

BEI YU

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RESEARCH INTERESTS

Machine learning & combinatorial algorithms in electronic design automation (EDA) and computer vision.

EXPERIENCE

Professor, CSE Department	Aug. 2025 – present
Associate Professor, CSE Department	Aug. 2021 – Jul. 2025
Assistant Professor, CSE Department	Aug. 2015 – Aug. 2021
The Chinese University of Hong Kong, Hong Kong SAR	
Postdoctoral Researcher, ECE Department	Aug. 2014 – July 2015
University of Texas at Austin, TX, USA	

EDUCATION

University of Texas at Austin, TX, USA	Aug. 2010 – Aug. 2014
Ph.D., Department of Electrical and Computer Engineering	
Tsinghua University, Beijing, P.R. China	Sep. 2007 – Jul. 2010
M.S., Department of Computer Science and Technology	
UESTC, Chengdu, P.R. China	Sep. 2003 – Jul. 2007
B.S., Information and Compute Science	

SELECTED AWARDS AND HONORS

Best Paper Award	ICCAD	2024
Best Paper Award	IEEE TSM	2022
Best Paper Award	DATE	2022
Best Paper Award	ICCAD	2021
Best Paper Award	ASPDAC	2021
Best Paper Award	Integration, VLSI Journal	2018
Best Paper Award	ISPD	2017
Best Paper Award	ICCAD	2013
Best Paper Award	ASPDAC	2012
Best Student Paper Award	ICTAI	2019
Best Student Paper Award	SPIE	2016
Best Paper Award Nomination	ISPD	2025
Best Paper Award Nomination	ICCAD	2024
Best Paper Award Nomination	ISPD	2024
Best Paper Award Nomination	ASPDAC	2023
Best Paper Award Nomination	MLCAD	2022
Best Paper Award Nomination	DATE	2021
Best Paper Award Nomination	ASPDAC	2019
Best Paper Award Nomination	DAC	2014
Best Paper Award Nomination	ASPDAC	2013
Best Paper Award Nomination	ICCAD	2011
Research Fellow Scheme (RFS) Award	RGC	2024
Under-40 Innovator Award	DAC	2024
Distinguished Lecturer	IEEE CEDA	2024
Mid-Career Award	IEEE TCSDM	2022
Ernest S. Kuh Early Career Award	IEEE CEDA	2022
Meritorious Service Award	ACM SIGDA	2021
Outstanding Dissertation Award	EDAA	2014
Outstanding Students Abroad Award	China Scholarship Council	2014
SPIE Scholarship	SPIE	2013
IBM Ph.D. Scholarship	IBM	2012
1st Place Award in CAD Contest	ICCAD	2015

2nd Place Award in CAD Contest	ICCAD	2024
2nd Place Award in CAD Contest	ICCAD	2018
2nd Place Award in CAD Contest	ICCAD	2013
2nd Place Award in CAD Contest	ICCAD	2012
3rd Place Award in CAD Contest	ICCAD	2022
3rd Place Award in ISPD Contest	ISPD	2020
3rd Place Award in ISPD Contest	ISPD	2017
2nd Place Award in ICDAR Competition	ICDAR	2021

PUBLICATIONS

Summary: IEEE TCAD (**92**), DAC (**62**), ICCAD (**51**), etc.

Journal Papers

- [J158] Siyuan Liang, Zhen Zhuang, Kai-Yuan Chao, Bei Yu, Tsung-Yi Ho, “Multi-Layer Package Power/Ground Planes Synthesis with Balanced DC IR Drops: A Game-Theoretic Optimization Approach”, accepted by IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**).
- [J157] Yang Bai, Mingjun Li, Wendong Xu, Bei Yu, “A Learned Performance Model with Transfer Learning Across GPUs on Tensorized Instructions”, accepted by IEEE Transactions on Parallel and Distributed Systems (**TPDS**).
- [J156] Weiran Chen, Zaitian Chen, Bei Yu, Song Chen, Yi Kang, Qi Xu, “Real-Time Compensation Framework for Large-Scale ReRAM-Based Sparse LU Factorization”, accepted by IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**).
- [J155] Peng Xu, Su Zheng, Mingzi Wang, Ziyang Yu, Shixin Chen, Tinghuan Chen, Keren Zhu, Tsung-Yi Ho, Bei Yu, “Rank-DSE: Neural Pareto Comparator of Microarchitecture Design Space Exploration”, accepted by ACM Transactions on Design Automation of Electronic Systems (**TODAES**).
- [J154] Mingjun Cheng, Shihan Zhang, Xin Zheng, Xian Lin, Huaie Gao, Shuting Cai, Xiaoming Xiong, Bei Yu, “Efficient Design Space Exploration for the BOOM Using SAC-Based Reinforcement Learning”, accepted by IEEE Transactions on Very Large Scale Integration Systems (**TVLSI**).
- [J153] Ziyi Wang, Siting Liu, Yuan Pu, Song Chen, Tsung-Yi Ho, Bei Yu, “[PRO-TIME: Pre-routing Optimization-aware Timing Prediction via Multimodal Learning](#)”, accepted by IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**).
- [J152] Yuan Pu, Zhuolun He, Yuqi Jiang, Tairu Qiu, Haoyuan Wu, Qi Sun, Cheng Zhuo, Bei Yu, “[Customized Retrieval Augmented Generation and Benchmarking for EDA Tool Documentation QA](#)”, accepted by IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**).
- [J151] Zhuolun He, Yuan Pu, Haoyuan Wu, Tairu Qiu, Bei Yu, “[Large Language Models for EDA: Future or Mirage?](#)”, accepted by ACM Transactions on Design Automation of Electronic Systems (**TODAES**).
- [J150] Zixiao Wang, Wenqian Zhao, Yunheng Shen, Yang Bai, Guojin Chen, Farzan Farnia, Bei Yu, “[DiffPattern-Flex: Efficient Layout Pattern Generation via Discrete Diffusion](#)”, accepted by IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**).
- [J149] Wan-Luan Lee, Dian-Lun Lin, Shui Jiang, Cheng-Hsiang Chiu, Yibo Lin, Bei Yu, Tsung-Yi Ho, Tsung-Wei Huang, “[G-kway: Multilevel GPU-Accelerated k-way Graph Partitioner using Task Graph Parallelism](#)”, accepted by ACM Transactions on Design Automation of Electronic Systems (**TODAES**).
- [J148] Xufeng Yao, Wenqian Zhao, Qi Sun, Cheng Zhuo, Bei Yu, “High-level Synthesis Directives Design Optimization via Large Language Model”, accepted by ACM Transactions on Design Automation of Electronic Systems (**TODAES**).
- [J147] Su Zheng, Wenqian Zhao, Shuyuan Sun, Fan Yang, Bei Yu, Martin D.F. Wong, “[Streamlining Computational Lithography with Efficient Pattern Database](#)”, accepted by IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**).
- [J146] Wenqian Zhao, Lancheng Zou, Zixiao Wang, Xufeng Yao, Bei Yu, “HAPE: Hardware-Aware LLM Pruning For Efficient On-Device Inference Optimization”, accepted by ACM Transactions on Design Automation of Electronic Systems (**TODAES**).
- [J145] Shuyuan Sun, Fan Yang, Bei Yu, Li Shang, Xuan Zeng, “[Adaptive ILT via Multi-level Lithography Simulation](#)”, accepted by IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**).

- [J144] Haoyang Xu, Xing Huang, Zhen Zhuang, Zhiwen Yu, Bin Guo, Kai-Yuan Chao, Bei Yu, Tsung-Yi Ho, Martin D.F. Wong, “[Hierarchical Partitioning-Based Inter-Chip Redistribution Layer Routing for Fan-Out Wafer-Level Packaging](#)”, accepted by IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**).
- [J143] Binwu Zhu, Su Zheng, Yuzhe Ma, Bei Yu, Martin Wong, “[Bridging Hotspot Detection and Mask Optimization via Domain-Crossing Masked Layout Modeling](#)”, accepted by ACM Transactions on Design Automation of Electronic Systems (**TODAES**).
- [J142] Peng Xu, Jindong Tu, Guojin Chen, Keren Zhu, Tinghuan Chen, Tsung-Yi Ho, Bei Yu, “[PARoute2: Enhanced Analog Routing via Performance-Drive Guidance Generation](#)”, accepted by IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**).
- [J141] Jindong Tu, Yapeng Li, Pengjia Li, Peng Xu, Qianru Zhang, Sanping Wan, Yongsheng Sun, Bei Yu, Tinghuan Chen, “[SMART: Graph Learning-Boosted Subcircuit Matching for Large-scale Analog Circuits](#)”, accepted by IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**).
- [J140] Xufeng Yao, Haoyang Li, Tsz Ho Chan, Wenyi Xiao, Mingxuan Yuan, Yu Huang, Lei Chen, Bei Yu, “[HDLdebugger: Streamlining HDL debugging with Large Language Models](#)”, accepted by ACM Transactions on Design Automation of Electronic Systems (**TODAES**).
- [J139] Weiguo Li, Zhipeng Huang, Bei Yu, Wenxing Zhu, Jian Chen, Zhixue He, Xingquan Li, “[iCTS: Iterative and Hierarchical Clock Tree Synthesis with Skew-Latency-Load Tree](#)”, accepted by IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**).
- [J138] Jiahao Xu, Zhuolun He, Shuo Yin, Yuan Pu, Wenjian Yu, Bei Yu, “[EasyMRC: Efficient Mask Rule Checking via Representative Edge Sampling](#)”, accepted by ACM Transactions on Design Automation of Electronic Systems (**TODAES**).
- [J137] Yuntao Lu, Chen Bai, Yuxuan Zhao, Ziyue Zheng, Yangdi Lyu, Mingyu Liu, Bei Yu, “[DeepVerifier: Learning to Update Test Sequences for Coverage-Guided Verification](#)”, accepted by ACM Transactions on Design Automation of Electronic Systems (**TODAES**).
- [J136] Siting Liu, Jieya Zhou, Jiayi Jiang, Zhuolun He, Ziyi Wang, Yibo Lin, Bei Yu, Martin Wong, “[Routing-aware Legal Hybrid Bonding Terminal Assignment for 3D Face-to-Face Stacked ICs](#)”, accepted by ACM Transactions on Design Automation of Electronic Systems (**TODAES**).
- [J135] Zhe Xiao, Xu He, Haoying Wu, Bei Yu, Yang Guo, “[EDA-Copilot: A RAG-Powered Intelligent Assistant for EDA Tools](#)”, accepted by ACM Transactions on Design Automation of Electronic Systems (**TODAES**).
- [J134] Yuan Pu, Tinghuan Chen, Zhuolun He, Jiajun Qin, Chen Bai, Haisheng Zheng, Yibo Lin, Bei Yu, “[IncreMacro: Incremental Macro Placement Refinement](#)”, accepted by IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**).
- [J133] Rongliang Fu, Chao Wang, Bei Yu, Tsung-Yi Ho, “[TeMACLE: A Technology Mapping-Aware Area-Efficient Standard Cell Library Extension Framework](#)”, accepted by IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**).
- [J132] Lancheng Zou, Su Zheng, Peng Xu, Siting Liu, Bei Yu, Martin D.F. Wong, “[Lay-Net: Grafting Netlist Knowledge on Layout-Based Congestion Prediction](#)”, accepted by IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**).
- [J131] Xinyun Zhang, Binwu Zhu, Fangzhou Liu, Jiayi Jiang, Ziyi Wang, Peng Xu, Hong Xu, Bei Yu, “[Pre-Routing Timing Prediction Across Different Technology Nodes](#)”, accepted by IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**).
- [J130] Zhuolun He, Yuan Pu, Haoyuan Wu, Yuhan Qin, Tairu Qiu, Bei Yu, “[Large Language Models for EDA: From Assistants to Agents](#)”, Foundations and Trends in Electronic Design Automation, vol. 14, no. 4, pp. 295–314, 2025.
- [J129] 1927 Siting Liu, Ziyi Wang, Fangzhou Liu, Yibo Lin, Bei Yu, Martin D.F. Wong, “[Sign-off Timing Considerations via Concurrent Routing Topology Optimization](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**), vol. 44, no. 05, pp. 1942–1953, 2025.
- [J128] Hongxi Wu, Xingquan Li, Liang Chen, Bei Yu, Wenxing Zhu, “[Delay-Driven Rectilinear Steiner Tree Construction](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**), vol. 44, no. 05, pp. 1928–1941, 2025.

- [J127] Ziyang Yu, Su Zheng, Wenqian Zhao, Shuo Yin, Xiaoxiao Liang, Guojin Chen, Yuzhe Ma, Bei Yu, Martin D.F. Wong, “[RuleLearner: OPC Rule Extraction from Inverse Lithography Technique Engine](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**), vol. 44, no. 05, pp. 1915–1927, 2025.
- [J126] Yuyang Ye, Peng Xu, Lizheng Ren, Tinghuan Chen, Hao Yan, Bei Yu, Longxing Shi, “[Learning-driven Physically-aware Large-scale Circuit Gate Sizing](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**), vol. 44, no. 05, pp. 1901–1914, 2025.
- [J125] Wenqian Zhao, Shuo Yin, Chen Bai, Zixiao Wang, Bei Yu, “[BAQE: Backend-Adaptive DNN Deployment via Synchronous Bayesian Quantization and Hardware Configuration Exploration](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**), vol. 44, no. 04, pp. 1394–1405, 2025.
- [J124] Hongduo Liu, Peiyu Liao, Mengchuan Zou, Bowen Pang, Xijun Li, Mingxuan Yuan, Tsung-Yi Ho, Bei Yu, “[Layout Decomposition via Boolean Satisfiability](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**), vol. 44, no. 03, pp. 1112–1125, 2025.
- [J123] Rongliang Fu, Mengmeng Wang, Yirong Kan, Olivia Chen, Nobuyuki Yoshikawa, Bei Yu, Tsung-Yi Ho, “[Buffer and Splitter Insertion for Adiabatic Quantum-Flux-Parametron Circuits](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**), vol. 44, no. 03, pp. 1180–1192, 2025.
- [J122] Ziyi Wang, Wenqian Zhao, Yuan Pu, Lei Chen, Wilson Wang Kit Thong, Weihua Sheng, Tsung-Yi Ho, Bei Yu, “[ParSGCN: Bridging the Gap Between Emulation Partitioning and Scheduling](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**), vol. 44, no. 03, pp. 1180–1192, 2025.
- [J121] Chen Bai, Xuechao Wei, Youwei Zhuo, Yi Cai, Hongzhong Zheng, Bei Yu, Yuan Xie, “[Klotski v2: Improved DNN Model Orchestration Framework for Dataflow Architecture Accelerators](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**), vol. 44, no. 03, pp. 1045–1058, 2025.
- [J120] Yuxuan Zhao, Peiyu Liao, Siting Liu, Jiayi Jiang, Yibo Lin, Bei Yu, “[Analytical Heterogeneous Die-to-Die 3D Placement with Macros](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**), vol. 44, no. 02, pp. 402–415, 2025.
- [J119] Ziyi Wang, Chen Bai, Zhuolun He, Guangliang Zhang, Qiang Xu, Tsung-Yi Ho, Yu Huang, Bei Yu, “[FGNN2: A Powerful Pre-training Framework for Learning the Logic Functionality of Circuits](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**), vol. 44, no. 01, pp. 227–240, 2025.
- [J118] Zehua Pei, Xufeng Yao, Wenqian Zhao, Bei Yu, “[Quantization via Distillation and Contrastive Learning](#)”, IEEE Transactions on Neural Networks and Learning Systems (**TNNLS**), vol. 35, no. 12, pp. 17164–17176, 2024.
- [J117] Jiequan Cui, Zhisheng Zhong, Zhuotao Tian, Shu Liu, Bei Yu, Jiaya Jia, “[Generalized Parametric Contrastive Learning](#)”, IEEE Transactions on Pattern Analysis and Machine Intelligence (**TPAMI**), vol. 46, no. 12, pp. 7463–7474, 2024.
- [J116] Lei Chen et al., “[Large circuit models: opportunities and challenges](#)”, Science China Information Sciences (**SCIS**), vol. 67, no. 10, 200402, 2024.
- [J115] Haoyuan Wu, Zhuolun He, Xinyun Zhang, Xufeng Yao, Su Zheng, Haisheng Zheng, Bei Yu, “[ChatEDA: A Large Language Model Powered Autonomous Agent for EDA](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**), vol. 43, no. 10, pp. 3184–3197, 2024.
- [J114] Peng Xu, Siyuan Xu, Tinghuan Chen, Guojin Chen, Tsung-Yi Ho, Bei Yu, “[DeepOTF: Learning Equations-constrained Prediction for Electromagnetic Behavior](#)”, ACM Transactions on Design Automation of Electronic Systems (**TODAES**), vol. 29, no. 05, pp. 80:1–80:22, 2024.
- [J113] Wenqian Zhao, Xufeng Yao, Shuo Yin, Yang Bai, Ziyang Yu, Yuzhe Ma, Bei Yu, Martin D.F. Wong, “[AdaOPC 2.0: Enhanced Adaptive Mask Optimization Framework for Via Layers](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**), vol. 43, no. 09, pp. 2674–2686, 2024.
- [J112] Yuyang Ye, Tinghuan Chen, Yifei Gao, Hao Yan, Bei Yu, Longxing Shi, “[Timing-driven Technology Mapping Approximation Based on Reinforcement Learning](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**), vol. 43, no. 09, pp. 2755–2768, 2024.

- [J111] Tinghuan Chen, Hao Geng, Qi Sun, Sanping Wan, Yongsheng Sun, Huatao Yu, Bei Yu, “[Wages: The Worst Transistor Aging Analysis for Large-scale Analog Integrated Circuits via Domain Generalization](#)”, ACM Transactions on Design Automation of Electronic Systems (**TODAES**), vol. 29, no. 05, pp. 73:1–73:23, 2024.
- [J110] Hongduo Liu, Yijian Qian, Youqiang Liang, Bin Zhang, Zhaohan Liu, Tao He, Wenqian Zhao, Jiangbo Lu, Bei Yu, “[A High-Performance Accelerator for Real-Time Super-Resolution on Edge FPGAs](#)”, ACM Transactions on Design Automation of Electronic Systems (**TODAES**), vol. 29, no. 03, pp. 53:1–53:25, 2024.
- [J109] Guojin Chen, Zixiao Wang, Bei Yu, David Z. Pan, Martin D.F. Wong, “[Ultra-Fast Source Mask Optimization via Conditional Discrete Diffusion](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**), vol. 43, no. 07, pp. 2140–2150, 2024.
- [J108] Jianwang Zhai, Zichao Ling, Chen Bai, Kang Zhao, Bei Yu, “[Machine Learning for Microarchitecture Power Modeling and Design Space Exploration: A Survey](#)”, Journal of Computer Research and Development (J-CRAD), vol. 61, no. 06, pp. 1–19, 2024. (in Chinese)
- [J107] Shixin Chen, Shanyi Li, Zhen Zhuang, Su Zheng, Zheng Liang, Tsung-Yi Ho, Bei Yu, Alberto L. Sangiovanni-Vincentelli, “[Floorplet: Performance-aware Floorplan Framework for Chiplet Integration](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**), vol. 43, no. 06, pp. 1638–1649, 2024.
- [J106] Peiyu Liao, Yuxuan Zhao, Dawei Guo, Yibo Lin, Bei Yu, “[Analytical Die-to-Die 3D Placement with Bistratal Wirelength Model and GPU Acceleration](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**), vol. 43, no. 06, pp. 1624–1637, 2024.
- [J105] Bo Yang, Qi Xu, Hao Geng, Song Chen, Bei Yu, Yi Kang, “[Floorplanning with Edge-Aware Graph Attention Network and Hindsight Experience Replay](#)”, ACM Transactions on Design Automation of Electronic Systems (**TODAES**), vol. 29, no. 03, pp. 56:1–56:17, 2024.
- [J104] Yuzhe Ma, Xufeng Yao, Ran Chen, Ruiyu Li, Xiaoyong Shen, Bei Yu, “[Small is Beautiful: Compressing Deep Neural Networks for Partial Domain Adaptation](#)”, IEEE Transactions on Neural Networks and Learning Systems (**TNNLS**), vol. 35, no. 03, pp. 3575–3585, 2024.
- [J103] Binwu Zhu, Su Zheng, Ziyang Yu, Guojin Chen, Yuzhe Ma, Fan Yang, Bei Yu, Martin Wong, “[L2O-ILT: Learning to Optimize Inverse Lithography Techniques](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**), vol. 43, no. 03, pp. 944–955, 2024.
- [J102] Xiaoliu Luo, Zhuotao Tian, Taiping Zhang, Bei Yu, Yuan Yan Tang, Jiaya Jia, “[PFENet: Boosting Few-shot Semantic Segmentation with the Noise-filtered Context-aware Prior Mask](#)”, IEEE Transactions on Pattern Analysis and Machine Intelligence (**TPAMI**), vol. 46, no. 02, pp. 1273–1289, 2024.
- [J101] Zhaoting Chen, Junzhe Cai, Changhao Yan, Zhaori Bi, Yuzhe Ma, Bei Yu, Dian Zhou, Xuan Zeng, “[pNeurFill: Enhanced Neural Network Model-Based Dummy Filling Synthesis with Perimeter Adjustment](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**), vol. 43, no. 02, pp. 667–680, 2024.
- [J100] Yang Bai, Xufeng Yao, Qi Sun, Wenqian Zhao, Shixin Chen, Zixiao Wang, Bei Yu, “[GTCO: Graph and Tensor Co-Design for Transformer-based Image Recognition on Tensor Cores](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**), vol. 43, no. 02, pp. 586–599, 2024.
- [J99] Yuyang Ye, Tinghuan Chen, Zicheng Wang, Hao Yan, Bei Yu, Longxing Shi, “[Fast and Accurate Aging-aware Cell Timing Model via Graph Learning](#)”, IEEE Transactions on Circuits and Systems II (**TCASII**), vol. 71, no. 01, pp. 156–160, 2024.
- [J98] Chen Bai, Qi Sun, Jianwang Zhai, Yuzhe Ma, Bei Yu, Martin D.F. Wong, “[BOOM-Explorer: RISC-V BOOM Microarchitecture Design Space Exploration](#)”, ACM Transactions on Design Automation of Electronic Systems (**TODAES**), vol. 29, no. 01, pp. 1–23, 2024.
- [J97] Xiaoxiao Liang, Yikang Ouyang, Haoyu Yang, Bei Yu, Yuzhe Ma, “[RL-OPC: Mask Optimization with Deep Reinforcement Learning](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**), vol. 43, no. 01, pp. 340–351, 2024.
- [J96] Guojin Chen, Ziyang Yu, Hongduo Liu, Yuzhe Ma, Bei Yu, “[DevelSet: Deep Neural Level Set for Instant Mask Optimization](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**), vol. 42, no. 12, pp. 5020–5033, 2023.

- [J95] Yuyang Ye, Tinghuan Chen, Yifei Gao, Hao Yan, Bei Yu, Longxing Shi, “[Aging-aware Critical Path Selection via Graph Attention Networks](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**), vol. 42, no. 10, pp. 5006–5019, 2023.
- [J94] Tinghuan Chen, Silu Xiong, Huan He, Bei Yu, “[TRouter: Thermal-driven PCB Routing via Non-Local Crisscross Attention Networks](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**), vol. 42, no. 10, pp. 3388–3401, 2023.
- [J93] Wenqian Zhao, Yang Bai, Qi Sun, Wenbo Li, Haisheng Zheng, Nianjuan Jiang, Jiangbo Lu, Bei Yu, Martin D.F. Wong, “[A High-Performance Accelerator for Super-Resolution Processing on Embedded GPU](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**), vol. 42, no. 10, pp. 3210–3223, 2023.
- [J92] Peiyu Liao, Dawei Guo, Zizheng Guo, Siting Liu, Yibo Lin, Bei Yu, “[DREAMPlace 4.0: Timing-driven Placement with Momentum-based Net Weighting and Lagrangian-based Refinement](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**), vol. 42, no. 10, pp. 3374–3387, 2023.
- [J91] Ziyang Yu, Peiyu Liao, Yuzhe Ma, Bei Yu, Martin D.F. Wong, “[CTM-SRAF: Continuous Transmission Mask-based Constraint-aware Sub Resolution Assist Feature Generation](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**), vol. 42, no. 10, pp. 3402–3411, 2023.
- [J90] Su Zheng, Hao Geng, Chen Bai, Bei Yu, Martin Wong, “[Boosting VLSI Design Flow Parameter Tuning with Random Embedding and Multi-objective Trust-region Bayesian Optimization](#)”, ACM Transactions on Design Automation of Electronic Systems (**TODAES**), vol. 28, no. 05, pp. 1–23, 2023.
- [J89] Binwu Zhu, Xinyun Zhang, Yibo Lin, Bei Yu, Martin Wong, “[DRC-SG 2.0: Efficient Design Rule Checking Script Generation via Key Information Extraction](#)”, ACM Transactions on Design Automation of Electronic Systems (**TODAES**), vol. 28, no. 05, pp. 1–18, 2023.
- [J88] Xiaogang Xu, Yi Wang, Liwei Wang, Bei Yu, Jiaya Jia, “[Conditional Temporal Variational AutoEncoder for Action Video Prediction](#)”, International Journal of Computer Vision (**IJCV**), vol. 131, no. 10, pp. 2699–2722, 2023.
- [J87] Ziyi Wang, Zhuolun He, Chen Bai, Haoyu Yang, Bei Yu, “[Efficient Arithmetic Block Identification with Graph Learning and Network-flow](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**), vol. 42, no. 08, pp. 2591–2603, 2023.
- [J86] Siting Liu, Yuan Pu, Peiyu Liao, Hongzhong Wu, Rui Zhang, Zhitang Chen, Wenlong Lv, Yibo Lin, Bei Yu, “[FastGR: Global Routing on CPU-GPU with Heterogeneous Task Graph Scheduler](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**), vol. 42, no. 07, pp. 2317–2330, 2023.
- [J85] Yilun Chen, Shijia Huang, Shu Liu, Bei Yu, Jiaya Jia, “[DSGN++: Exploiting Visual-Spatial Relation for Stereo-based 3D Detectors](#)”, IEEE Transactions on Pattern Analysis and Machine Intelligence (**TPAMI**), vol. 45, no. 4, pp. 4416–4429, 2023.
- [J84] Zhuotao Tian, Pengguang Chen, Xin Lai, Li Jiang, Shu Liu, Hengshuang Zhao, Bei Yu, Ming-Chang Yang, Jiaya Jia, “[Adaptive Perspective Distillation for Semantic Segmentation](#)”, IEEE Transactions on Pattern Analysis and Machine Intelligence (**TPAMI**), vol. 45, no. 2, pp. 1372–1387, 2023.
- [J83] Ran Chen, Shoubo Hu, Zhitang Chen, Shengyu Zhu, Bei Yu, Pengyun Li, Cheng Chen, Yu Huang, Jianye Hao, “[A Unified Framework for Layout Pattern Analysis with Deep Causal Estimation](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**), vol. 42, no. 04, pp. 1199–1211, 2023.
- [J82] Tinghuan Chen, Grace Li Zhang, Bei Yu, Bing Li, Ulf Schlichtmann, “[Machine Learning in Advanced IC Design: A Methodological Survey](#)”, IEEE Design & Test, vol. 40, no. 01, pp. 17–33, 2023. (**Invited Paper**)
- [J81] Ulf Schlichtmann, Bing Li, Bei Yu, Raviv Gal, “[Guest Editors’ Introduction: Special Issue on Machine Learning for CAD/EDA](#)”, IEEE Design & Test, vol. 40, no. 01, pp. 5–7, 2023.
- [J80] Ziyang Yu, Guojin Chen, Yuzhe Ma, Bei Yu, “[A GPU-enabled Level Set Method for Mask Optimization](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**), vol. 42, no. 02, pp. 594–605, 2023.
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- [C153] Jianwang Zhai, Yici Cai, Bei Yu, “[Microarchitecture Power Modeling via Artificial Neural Network and Transfer Learning](#)”, IEEE/ACM Asian and South Pacific Design Automation Conference (**ASPDAC**), Tokyo Odaiba Miraikan, Jan. 16–19, 2023. (**Best Paper Award Nomination**)
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- [C122] Chen Bai, Qi Sun, Jianwang Zhai, Yuzhe Ma, Bei Yu, Martin D.F. Wong, “[BOOM-Explorer: RISC-V BOOM Microarchitecture Design Space Exploration Framework](#)”, IEEE/ACM International Conference on Computer-Aided Design (**ICCAD**), Nov. 1–4, 2021. **(William J. McCalla Best Paper Award)**
- [C121] Jianwang Zhai, Chen Bai, Binwu Zhu, Yici Cai, Qiang Zhou, Bei Yu, “[McPAT-Calib: A Microarchitecture Power Modeling Framework for Modern CPUs](#)”, IEEE/ACM International Conference on Computer-Aided Design (**ICCAD**), Nov. 1–4, 2021.
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- [C115] Ziyang Yu, Guojin Chen, Yuzhe Ma, Bei Yu, “[A GPU-enabled Level-Set Method for Mask Optimization](#)”, IEEE/ACM Proceedings Design, Automation and Test in Europe (**DATE**), Feb. 01–05, 2021.
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- [C113] Qi Sun, Chen Bai, Hao Geng, Bei Yu, “[Deep Neural Network Hardware Deployment Optimization via Advanced Active Learning](#)”, IEEE/ACM Proceedings Design, Automation and Test in Europe (**DATE**), Feb. 01–05, 2021.
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- [C109] Wei Li, Yuxiao Qu, Gengjie Chen, Yuzhe Ma, Bei Yu, “[TreeNet: Deep Point Cloud Embedding for Routing Tree Construction](#)”, IEEE/ACM Asian and South Pacific Design Automation Conference (**ASPDAC**), Jan. 18–21, 2021. (**Best Paper Award**)
- [C108] Tinghuan Chen, Qi Sun, Canhui Zhan, Changze Liu, Huatao Yu, Bei Yu, “[Analog IC Aging-induced Degradation Estimation via Heterogeneous Graph Convolutional Networks](#)”, IEEE/ACM Asian and South Pacific Design Automation Conference (**ASPDAC**), Jan. 18–21, 2021.
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- [C106] Hao Geng, Haoyu Yang, Lu Zhang, Jin Miao, Fan Yang, Xuan Zeng, Bei Yu, “[Hotspot Detection via Attention-based Deep Layout Metric Learning](#)”, IEEE/ACM International Conference on Computer-Aided Design (**ICCAD**), Nov. 2–5, 2020.
- [C105] Qi Sun, Arjun Ashok Rao, Xufeng Yao, Bei Yu, Shiyan Hu, “[Counteracting Adversarial Attack in Autonomous Driving](#)”, IEEE/ACM International Conference on Computer-Aided Design (**ICCAD**), Nov. 2–5, 2020. (**Invited Paper**)
- [C104] Guojin Chen, wanli chen, Yuzhe Ma, Haoyu Yang, Bei Yu, “[DAMO: Deep Agile Mask Optimization for Full Chip Scale](#)”, IEEE/ACM International Conference on Computer-Aided Design (**ICCAD**), Nov. 2–5, 2020.
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- [C101] Zhuolun He, Yuzhe Ma, Lu Zhang, Peiyu Liao, Ngai Wong, Bei Yu, Martin D. F. Wong, “[Learn to Floorplan through Acquisition of Effective Local Search Heuristics](#)”, IEEE International Conference on Computer Design (**ICCD**), Oct. 18–21, 2020.
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- [C99] Ran Chen, Yong Liu, Mengdan Zhang, Shu Liu, Bei Yu, Yu-Wing Tai, “[Dive Deeper Into Box for Object Detection](#)”, European Conference on Computer Vision (**ECCV**), August 23–28, 2020.
- [C98] Wei Li, Jialu Xia, Yuzhe Ma, Jialu Li, Yibo Lin, Bei Yu, “[Adaptive Layout Decomposition with Graph Embedding Neural Networks](#)”, ACM/IEEE Design Automation Conference (**DAC**), San Francisco, July 19–23, 2020.
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- [C94] Yuzhe Ma, Zhuolun He, Wei Li, Tinghuan Chen, Lu Zhang, Bei Yu, “[Understanding Graphs in EDA: From Shallow to Deep Learning](#)”, ACM International Symposium on Physical Design (**ISPD**), Taipei, Mar. 25–Apr. 01, 2020. (**Invited Paper**)
- [C93] Haoyu Yang, Wei Zhong, Yuzhe Ma, Hao Geng, Ran Chen, Wanli Chen, Bei Yu, “[VLSI Mask Optimization: From Shallow To Deep Learning](#)”, IEEE/ACM Asian and South Pacific Design Automation Conference (**ASPDAC**), Beijing, Jan. 13–16, 2020. (**Invited Paper**)
- [C92] Qi Sun, Tinghuan Chen, Jin Miao, Bei Yu, “[Power-Driven DNN Dataflow Optimization on FPGA](#)”, IEEE/ACM International Conference on Computer-Aided Design (**ICCAD**), Westminster, Nov. 4–7, 2019. (**Invited Paper**)

- [C91] Yuzhe Ma, Ran Chen, Wei Li, Fanhua Shang, Wenjian Yu, Minsik Cho, Bei Yu, “[A Unified Approximation Framework for Compressing and Accelerating Deep Neural Networks](#)”, IEEE International Conference on Tools with Artificial Intelligence (ICTAI), Portland, OR, Nov. 4–6, 2019. **(Best Student Paper Award)**
- [C90] Wei Li, Yuzhe Ma, Qi Sun, Yibo Lin, Iris Hui-Ru Jiang, Bei Yu, David Z. Pan, “[OpenMPL: An Open Source Layout Decomposer](#)”, IEEE International Conference on ASIC (ASICON), Chongqing, China, Oct. 29–Nov. 1, 2019. **(Invited Paper)**
- [C89] Yuzhe Ma, Ziyang Yu, Bei Yu, “[CAD Tool Design Space Exploration via Bayesian Optimization](#)”, ACM/IEEE Workshop on Machine Learning for CAD (**MLCAD**), Alberta, Canada, Sep. 3–4, 2019.
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- [C81] Haocheng Li, Satwik Patnaik, Abhrajit Sengupta, Haoyu Yang, Johann Knechtel, Bei Yu, Evangeline F. Y. Young, Ozgur Sinanoglu, “[Attacking Split Manufacturing from a Deep Learning Perspective](#)”, ACM/IEEE Design Automation Conference (**DAC**), pp. 135:1–135:6, Las Vegas, June 2–6, 2019.
- [C80] Bentian Jiang, Xiaopeng Zhang, Ran Chen, Gengjie Chen, Peishan Tu, Wei Li, Evangeline F. Y. Young, Bei Yu, “[FIT: Fill Insertion Considering Timing](#)”, ACM/IEEE Design Automation Conference (**DAC**), pp. 221:1–221:6, Las Vegas, June 2–6, 2019.
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- [C78] Haoyu Yang, Piyush Pathak, Frank Gennari, Ya-Chieh Lai, Bei Yu, “[Detecting Multi-Layer Layout Hotspots with Adaptive Squish Patterns](#)”, IEEE/ACM Asian and South Pacific Design Automation Conference (**ASPDAC**), pp. 299–304, Tokyo, Jan. 21–24, 2019. **(Invited Paper)**
- [C77] Xingquan Li, Bei Yu, Jianli Chen, Wenxing Zhu, “[A Local Optimal Method on DSA Guiding Template Assignment with Redundant Dummy Via Insertion](#)”, IEEE/ACM Asian and South Pacific Design Automation Conference (**ASPDAC**), pp. 305–310, Tokyo, Jan. 21–24, 2019. **(Invited Paper)**
- [C76] Hao Geng, Haoyu Yang, Yuzhe Ma, Joydeep Mitra, Bei Yu, “[SRAF Insertion via Supervised Dictionary Learning](#)”, IEEE/ACM Asian and South Pacific Design Automation Conference (**ASPDAC**), pp. 406–411, Tokyo, Jan. 21–24, 2019. **(Best Paper Award Nomination)**
- [C75] Zheng Zhao, Derong Liu, Meng Li, Zhoufeng Ying, Biying Xu, Lu Zhang, Bei Yu, Ray T. Chen, David Z. Pan, “[Hardware-software Co-design of Slimmed Optical Neural Networks](#)”, IEEE/ACM Asian and South Pacific Design Automation Conference (**ASPDAC**), pp. 705–710, Tokyo, Jan. 21–24, 2019.
- [C74] Hao Geng, Haoyu Yang, Bei Yu, Xingquan Li, Xuan Zeng, “[Sparse VLSI Layout Feature Extraction: A Dictionary Learning Approach](#)”, IEEE Computer Society Annual Symposium on VLSI (ISVLSI), pp. 488–493, Hong Kong, July 9–11, 2018. **(Invited Paper)**

- [C73] Haoyu Yang, Shuhe Li, Yuzhe Ma, Bei Yu, Evangeline F. Y. Young, “[GAN-OPC: Mask Optimization with Lithography-guided Generative Adversarial Nets](#)”, ACM/IEEE Design Automation Conference (**DAC**), pp. 136:1–136:6, San Francisco, June 24–28, 2018.
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- [C69] Wei Ye, Meng Li, Kai Zhong, Bei Yu, David Z. Pan, “[Power Grid Reduction by Sparse Convex Optimization](#)”, ACM International Symposium on Physical Design (**ISPD**), pp. 60–67, Monterey, Mar. 25–28, 2018.
- [C68] Grace Li Zhang, Bing Li, Bei Yu, David Z. Pan, Ulf Schlichtmann, “[TimingCamouflage: Improving Circuit Security against Counterfeiting by Unconventional Timing](#)”, IEEE/ACM Proceedings Design, Automation and Test in Europe (DATE), pp. 91–96, Dresden, Mar. 19–23, 2018.
- [C67] Meng Li, Bei Yu, Yibo Lin, Xiaoqing Xu, Wuxi Li, David Z. Pan, “[A Practical Split Manufacturing Framework for Trojan Prevention via Simultaneous Wire Lifting and Cell Insertion](#)”, IEEE/ACM Asian and South Pacific Design Automation Conference (**ASPDAC**), pp. 265–270, Jeju Island, Jan. 22–25, 2018.
- [C66] Chak-Wa Pui, Gengjie Chen, Yuzhe Ma, Evangeline F. Y. Young, Bei Yu, “[Clock-Aware UltraScale FPGA Placement with Machine Learning Routability Prediction](#)”, IEEE/ACM International Conference on Computer-Aided Design (**ICCAD**), pp. 929–936, Irvine, Nov. 13–16, 2017. (**Invited Paper**)
- [C65] Yuzhe Ma, Jih-Rong Gao, Jian Kuang, Jin Miao, Bei Yu, “[A Unified Framework for Simultaneous Layout Decomposition and Mask Optimization](#)”, IEEE/ACM International Conference on Computer-Aided Design (**ICCAD**), pp. 81–88, Irvine, Nov. 13–16, 2017.
- [C64] Yuzhe Ma, Xuan Zeng, Bei Yu, “[Methodologies for Layout Decomposition and Mask Optimization: A Systematic Review](#)”, IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC), Abu Dhabi, UAE, Oct. 23–25, 2017. (**Invited Paper**)
- [C63] Cheng Zhuo, Bei Yu, Di Gao, “[Accelerating Chip Design with Machine Learning: From Pre-Silicon to Post-Silicon](#)”, IEEE International System-on-Chip Conference (SOCC), pp. 227–232, Munich, Germany, September 5–8, 2017. (**Invited Paper**)
- [C62] Haoyu Yang, Yajun Lin, Bei Yu, Evangeline F. Y. Young, “[Lithography Hotspot Detection: From Shallow To Deep Learning](#)”, IEEE International System-on-Chip Conference (SOCC), pp. 233–238, Munich, Germany, September 5–8, 2017. (**Invited Paper**)
- [C61] Subhendu Roy, Yuzhe Ma, Jin Miao, Bei Yu, “[A Learning Bridge from Architectural Synthesis to Physical Design for Exploring Power Efficient High-Performance Adders](#)”, IEEE International Symposium on Low Power Electronics and Design (ISLPED), Taipei, July 24–26, 2017.
- [C60] Haoyu Yang, Jing Su, Yi Zou, Bei Yu, Evangeline F. Y. Young, “[Layout Hotspot Detection with Feature Tensor Generation and Deep Biased Learning](#)”, ACM/IEEE Design Automation Conference (**DAC**), pp. 62:1–62:6, Austin, June 18–22, 2017.
- [C59] Gengjie Chen, Jian Kuang, Zhiliang Zeng, Hang Zhang, Evangeline F. Y. Young, Bei Yu, “[Minimizing Thermal Gradient and Pumping Power in 3D IC Liquid Cooling Network Design](#)”, ACM/IEEE Design Automation Conference (**DAC**), pp. 70:1–70:6, Austin, June 18–22, 2017.
- [C58] Soumi Chattopadhyay, Ansuman Banerjee, Bei Yu, “[A Utility-Driven Data Transmission Optimization Strategy in Large Scale Cyber-Physical Systems](#)”, IEEE/ACM Proceedings Design, Automation and Test in Europe (DATE), pp. 1619–1622, Lausanne, Mar. 27–31, 2017.
- [C57] Hang Zhang, Fengyuan Zhu, Haocheng Li, Evangeline F. Y. Young, Bei Yu, “[Bilinear Lithography Hotspot Detection](#)”, ACM International Symposium on Physical Design (**ISPD**), pp. 7–14, Portland, Mar. 19–22, 2017. (**Best Paper Award**)

- [C56] Jiaojiao Ou, Bei Yu, Xiaoqing Xu, Joydeep Mitra, Yibo Lin, David Z. Pan, “[DSAR: DSA aware Routing with Simultaneous DSA Guiding Pattern and Double Patterning Assignment](#)”, ACM International Symposium on Physical Design (**ISPD**), pp. 91–98, Portland, Mar. 19–22, 2017.
- [C55] Haoyu Yang, Luyang Luo, Jing Su, Chenxi Lin, Bei Yu, “[Imbalance Aware Lithography Hotspot Detection: A Deep Learning Approach](#)”, SPIE Intl. Symp. Advanced Lithography Conference, San Jose, CA, Feb. 26—Mar. 2, 2017.
- [C54] Chak-Wa Pui, Gengjie Chen, Wing-Kai Chow, Jian Kuang, Ka-Chun Lam, Peishan Tu, Hang Zhang, Evangeline F. Y. Young, Bei Yu, “[RippleFPGA: A Routability-Driven Placement for Large-Scale Heterogeneous FPGAs](#)”, IEEE/ACM International Conference on Computer-Aided Design (**ICCAD**), pp. 67:1–67:8, Austin, Nov. 7–10, 2016. (**Invited Paper**)
- [C53] Jian Kuang, Evangeline F. Y. Young, Bei Yu, “[Incorporating Cut Redistribution with Mask Assignment to Enable 1D Gridded Design](#)”, IEEE/ACM International Conference on Computer-Aided Design (**ICCAD**), pp. 48:1–48:8, Austin, Nov. 7–10, 2016.
- [C52] Hang Zhang, Bei Yu, Evangeline F. Y. Young, “[Enabling Online Learning in Lithography Hotspot Detection with Information-Theoretic Feature Optimization](#)”, IEEE/ACM International Conference on Computer-Aided Design (**ICCAD**), pp. 47:1–47:8, Austin, Nov. 7–10, 2016.
- [C51] Jin Miao, Meng Li, Subhendu Roy, Bei Yu, “[LRR-DPUF: Learning Resilient and Reliable Digital Physical Unclonable Function](#)”, IEEE/ACM International Conference on Computer-Aided Design (**ICCAD**), pp. 46:1–46:8, Austin, Nov. 7–10, 2016.
- [C50] Meng Li, Kaveh Shamsi, Travis Meade, Zheng Zhao, Bei Yu, Yier Jin, David Z. Pan, “[Provably Secure Camouflaging Strategy for IC Protection](#)”, IEEE/ACM International Conference on Computer-Aided Design (**ICCAD**), pp. 28:1–28:8, Austin, Nov. 7–10, 2016.
- [C49] Yibo Lin, Bei Yu, Xiaoqing Xu, Jih-Rong Gao, Natarajan Viswanathan, Wen-Hao Liu, Zhuo Li, Charles J. Alpert, David Z. Pan, “[MrDP: Multiple-row Detailed Placement of Heterogeneous-sized Cells for Advanced Nodes](#)”, IEEE/ACM International Conference on Computer-Aided Design (**ICCAD**), pp. 7:1–7:8, Austin, Nov. 7–10, 2016.
- [C48] Yibo Lin, Bei Yu, David Z. Pan, “[Detailed Placement In Advanced Technology Nodes: A Survey](#)”, IEEE International Conference on Solid -State and Integrated Circuit Technology (ICSICT), Hangzhou, Oct. 25–28, 2016. (**Invited Paper**)
- [C47] Hang Zhang, Haoyu Yang, Bei Yu, Evangeline F. Y. Young, “[VLSI Layout Hotspot Detection Based on Discriminative Feature Extraction](#)”, IEEE Asia Pacific Conference on Circuits and Systems (APCCAS), Jeju, Oct. 25–28, 2016. (**Invited Paper**)
- [C46] Derong Liu, Bei Yu, Salim Chowdhury, David Z. Pan, “[Incremental Layer Assignment for Critical Path Timing](#)”, ACM/IEEE Design Automation Conference (**DAC**), pp. 85:1–85:6, Austin, June 5–9, 2016.
- [C45] Xiaotao Jia, Qiang Zhou, Yici Cai, Bei Yu, “[MCFRoute 2.0: A Redundant Via Insertion Enhanced Concurrent Detailed Router](#)”, ACM Great Lakes Symposium on VLSI (GLSVLSI), pp. 87–92, Boston, MA, May 18–20, 2016.
- [C44] Jiaojiao Ou, Bei Yu, David Z. Pan, “[Concurrent Guiding Template Assignment and Redundant Via Insertion for DSA-MP Hybrid Lithography](#)”, ACM International Symposium on Physical Design (**ISPD**), pp. 39–46, Sonoma, April 3–6, 2016.
- [C43] Yibo Lin, Xiaoqing Xu, Bei Yu, Ross Baldick, David Z. Pan, “[Triple/Quadruple Patterning Layout Decomposition via Novel Linear Programming and Iterative Rounding](#)”, SPIE Intl. Symp. Advanced Lithography Conference, San Jose, CA, Feb. 21–25, 2016. (**Best Student Paper Award**)
- [C42] Tetsuaki Matsunawa, Bei Yu, David Z. Pan, “[Laplacian Eigenmaps and Bayesian Clustering Based Layout Pattern Sampling and Its Applications to Hotspot Detection and OPC](#)”, IEEE/ACM Asian and South Pacific Design Automation Conference (**ASPDAC**), pp. 679–684, Macau, Jan. 25–28, 2016.
- [C41] Yibo Lin, Bei Yu, Yi Zou, Zhuo Li, Charles J. Alpert, David Z. Pan, “[Stitch Aware Detailed Placement for Multiple E-Beam Lithography](#)”, IEEE/ACM Asian and South Pacific Design Automation Conference (**ASPDAC**), pp. 186–191, Macau, Jan. 25–28, 2016.
- [C40] Bei Yu, Derong Liu, Salim Chowdhury, David Z. Pan, “[TILA: Timing-Driven Incremental Layer Assignment](#)”, IEEE/ACM International Conference on Computer-Aided Design (**ICCAD**), pp. 110–117, Austin, Nov. 2–6, 2015.

- [C39] Yibo Lin, Bei Yu, Biying Xu, David Z. Pan, “[Triple Patterning Aware Detailed Placement Toward Zero Cross-Row Middle-of-Line Conflict](#)”, IEEE/ACM International Conference on Computer-Aided Design (**ICCAD**), pp. 396–403, Austin, Nov.2–6, 2015.
- [C38] David Z. Pan, Lars Liebmann, Bei Yu, Xiaoqing Xu, Yibo Lin, “[Pushing Multiple Patterning in Sub-10nm: Are We Ready?](#)”, ACM/IEEE Design Automation Conference (**DAC**), pp. 197:1–197:6, San Francisco, June 7–11, 2015. (**Invited Paper**)
- [C37] Xiaoqing Xu, Bei Yu, Jhih-Rong Gao, Che-Lun Hsu, David Z. Pan, “[PARR: Pin Access Planning and Regular Routing for Self-Aligned Double Patterning](#)”, ACM/IEEE Design Automation Conference (**DAC**), pp. 28:1–28:6, San Francisco, June 7–11, 2015.
- [C36] Yibo Lin, Bei Yu, David Z. Pan, “[High Performance Dummy Fill Insertion with Coupling and Uniformity Constraints](#)”, ACM/IEEE Design Automation Conference (**DAC**), pp. 71:1–71:6, San Francisco, June 7–11, 2015.
- [C35] Wei Ye, Bei Yu, Yong-Chan Ban, Lars Liebmann, David Z. Pan, “[Standard Cell Layout Regularity and Pin Access Optimization Considering Middle-of-Line](#)”, ACM Great Lakes Symposium on VLSI (GLSVLSI), pp. 289–294, Pittsburgh, PA, May 20–22, 2015.
- [C34] Jiaojiao Ou, Bei Yu, Jhih-Rong Gao, Moshe Preil, Azat Latypov, David Z. Pan, “[Directed Self-Assembly Based Cut Mask Optimization for Unidirectional Design](#)”, ACM Great Lakes Symposium on VLSI (GLSVLSI), pp. 83–86, Pittsburgh, PA, May 20–22, 2015.
- [C33] Tetsuaki Matsunawa, Bei Yu, David Z. Pan, “[Optical proximity correction with hierarchical Bayes model](#)”, SPIE Intl. Symp. Advanced Lithography - Optical Microlithography XXVIII, San Jose, CA, Feb. 22–26, 2015.
- [C32] Tetsuaki Matsunawa, Jhih-Rong Gao, Bei Yu, David Z. Pan, “[A new lithography hotspot detection framework based on AdaBoost classifier and simplified feature extraction](#)”, SPIE Intl. Symp. Advanced Lithography - Design-Process-Technology Co-optimization for Manufacturability IX, San Jose, CA, Feb. 22–26, 2015.
- [C31] Xiaoqing Xu, Brian Cline, Greg Yeric, Bei Yu, David Z. Pan, “[A systematic framework for evaluating standard cell middle-of-line \(MOL\) robustness for multiple patterning](#)”, SPIE Intl. Symp. Advanced Lithography - Design-Process-Technology Co-optimization for Manufacturability IX, San Jose, CA, Feb. 22–26, 2015.
- [C30] Bei Yu, David Z. Pan, Tetsuaki Matsunawa, Xuan Zeng, “[Machine Learning and Pattern Matching in Physical Design](#)”, IEEE/ACM Asian and South Pacific Design Automation Conference (**ASPDAC**), pp. 286–293, Japan, Jan. 19–22, 2015. (**Invited Paper**)
- [C29] Jiwoo Pak, Bei Yu, David Z. Pan, “[Electromigration-aware Redundant Via Insertion](#)”, IEEE/ACM Asian and South Pacific Design Automation Conference (**ASPDAC**), pp. 544–549, Japan, Jan. 19–22, 2015.
- [C28] Bei Yu, Gilda Garreton, David Z. Pan, “[Layout Compliance for Triple Patterning Lithography: An Iterative Approach](#)”, SPIE/BACUS Photomask Symposium, Monterey, CA, Sept. 16–18, 2014. (**Invited Paper**)
- [C27] Bei Yu, David Z. Pan, “[Layout Decomposition for Quadruple Patterning Lithography and Beyond](#)”, SRC Techcon Conference, Austin, TX, Sept. 7–9, 2014.
- [C26] Jhih-Rong Gao, Xiaoqing Xu, Bei Yu, David Z. Pan, “[MOSAIC: Mask Optimizing Solution With Process Window Aware Inverse Correction](#)”, ACM/IEEE Design Automation Conference (**DAC**), pp. 52:1–52:6, San Francisco, June 1–5, 2014. (**Best Paper Award Nomination**)
- [C25] Bei Yu, David Z. Pan, “[Layout Decomposition for Quadruple Patterning Lithography and Beyond](#)”, ACM/IEEE Design Automation Conference (**DAC**), pp. 53:1–53:6, San Francisco, June 1–5, 2014.
- [C24] Xiaoqing Xu, Brian Cline, Greg Yeric, Bei Yu, David Z. Pan, “[Self-Aligned Double Patterning Aware Pin Access and Standard Cell Layout Co-Optimization](#)”, ACM International Symposium on Physical Design (**ISPD**), pp. 101–108, Petaluma, March 30–April 2, 2014.
- [C23] Jhih-Rong Gao, Bei Yu, Duo Ding, David Z. Pan, “[Accurate lithography hotspot detection based on PCA-SVM classifier with hierarchical data clustering](#)”, SPIE Intl. Symp. Advanced Lithography - Design-Process-Technology Co-optimization for Manufacturability VIII, San Jose, CA, Feb. 23–27, 2014.
- [C22] Bei Yu, Jhih-Rong Gao, Xiaoqing Xu, David Z. Pan, “[Bridging the Gap from Mask to Physical Design for Multiple Patterning Lithography](#)”, SPIE Intl. Symp. Advanced Lithography - Design-Process-

- Technology Co-optimization for Manufacturability VIII, San Jose, CA, Feb. 23–27, 2014. (**Invited Paper**)
- [C21] Jhih-Rong Gao, Bei Yu, David Z. Pan, “[Self-Aligned Double Patterning Layout Decomposition with Complementary E-Beam Lithography](#)”, IEEE/ACM Asian and South Pacific Design Automation Conference (**ASPDAC**), pp. 143–148, Singapore, Jan. 20–23, 2014.
 - [C20] Bei Yu, Xiaoqing Xu, Jhih-Rong Gao, David Z. Pan, “[Methodology for Standard Cell Compliance and Detailed Placement for Triple Patterning Lithography](#)”, IEEE/ACM International Conference on Computer-Aided Design (**ICCAD**), pp. 349–356, San Jose, Nov. 18–21, 2013. (**William J. McCalla Best Paper Award**)
 - [C19] Bei Yu, Yen-Hung Lin, Gerard Luk-Pat, Duo Ding, Kevin Lucas, David Z. Pan, “[A High-Performance Triple Patterning Layout Decomposer with Balanced Density](#)”, IEEE/ACM International Conference on Computer-Aided Design (**ICCAD**), pp. 163–169, San Jose, Nov. 18–21, 2013.
 - [C18] Jhih-Rong Gao, Bei Yu, Duo Ding, David Z. Pan, “[Lithography Hotspot Detection and Mitigation in Nanometer VLSI](#)”, IEEE International Conference on ASIC (ASICON), pp. 1–4, Shenzhen, China, Oct. 28–31, 2013. (**Invited Paper**)
 - [C17] Bei Yu, Kun Yuan, Jhih-Rong Gao, David Z. Pan, “[E-BLOW: E-Beam Lithography Overlapping aware Stencil Planning for MCC System](#)”, ACM/IEEE Design Automation Conference (**DAC**), pp. 70:1–70:7, Austin, June 2–6, 2013.
 - [C16] Bei Yu, Jhih-Rong Gao, David Z. Pan, “[Triple-patterning lithography \(TPL\) layout decomposition using end-cutting](#)”, SPIE Intl. Symp. Advanced Lithography, San Jose, CA, Feb. 24–28, 2013.
 - [C15] Jhih-Rong Gao, Bei Yu, Ru Huang, David Z. Pan, “[Self-aligned Double Patterning Friendly Configuration for Standard Cell Library Considering Placement](#)”, SPIE Intl. Symp. Advanced Lithography, San Jose, CA, Feb. 24–28, 2013.
 - [C14] Bei Yu, Jhih-Rong Gao, David Z. Pan, “[L-Shape based Layout Fracturing for E-Beam Lithography](#)”, IEEE/ACM Asia and South Pacific Design Automation Conference (**ASPDAC**), pp. 249–254, Japan, Jan. 22–25, 2013. (**Best Paper Award Nomination**)
 - [C13] Bei Yu, Jhih-Rong Gao, Duo Ding, Yongchan Ban, Jae-Seok Yang, Kun Yuan, Minsik Cho, David Z. Pan, “[Dealing with IC Manufacturability in Extreme Scaling](#)”, IEEE/ACM International Conference on Computer-Aided Design (**ICCAD**), pp. 240–242, San Jose, Nov. 5–8, 2012. (**Embedded Tutorial paper**)
 - [C12] Yen-Hung Lin, Bei Yu, David Z. Pan, Yih-Lang Li, “[TRIAD: A Triple Patterning Lithography Aware Detailed Router](#)”, IEEE/ACM International Conference on Computer-Aided Design (**ICCAD**), pp. 123–129, San Jose, Nov. 5–8, 2012.
 - [C11] David Z. Pan, Jhih-Rong Gao, Bei Yu, “[VLSI CAD for Emerging Nanolithography](#)”, International Symposium on VLSI Design, Automation and Test (VLSI-DAT), pp. 1–4, 2012. (**Invited Paper**)
 - [C10] Kevin Lucas, Chris Cork, Bei Yu, Gerry Luk-Pat, Ben Painter, David Z. Pan, “[Implications of triple patterning for 14 nm node design and patterning](#)”, SPIE Advanced Lithography Symposium Design for Manufacturability through Design-Process Integration VI (Conference 8327), Feb. 2012. (**Keynote Paper**)
 - [C9] Duo Ding, Bei Yu, Joydeep Ghosh, David Z. Pan, “[EPIC: Efficient Prediction of IC Manufacturing Hotspots With A Unified Meta-Classification Formulatio](#)”, IEEE/ACM Asia and South Pacific Design Automation Conference (**ASPDAC**), pp. 263–270, Sydney, Jan. 30–Feb. 3, 2012. (**Best Paper Award**)
 - [C8] Duo Ding, Bei Yu, David Z. Pan, “[GLOW: A Global Router for Low-Power Thermal-reliable Interconnect Synthesis using Photonic Wavelength Multiplexing](#)”, IEEE/ACM Asia and South Pacific Design Automation Conference (**ASPDAC**), pp. 621–626, Sydney, Jan. 30–Feb. 3, 2012.
 - [C7] Bei Yu, Kun Yuan, Boyang Zhang, Duo Ding, David Z. Pan, “[Triple Patterning Lithography Layout Decomposition](#)”, IEEE/ACM International Conference on Computer-Aided Design (**ICCAD**), pp. 1–8, San Jose, Nov. 2011. (**William J. McCalla Best Paper Award Nomination**)
 - [C6] Bei Yu, Sheqin Dong, Yuchun Ma, Tao Lin, Yu Wang, Song Chen, Satoshi Goto, “[Network Flow-based Simultaneous Retiming and Slack Budgeting for Low Power Design](#)”, IEEE/ACM Asia and South Pacific Design Automation Conference (**ASPDAC**), pp. 473–478, Japan, Jan. 2011.
 - [C5] Wei Zhong, Bei Yu, Song Chen, Takeshi Yoshimura, Sheqin Dong, Satoshi Goto, “[Application-Specific Network-on-Chip Synthesis: Cluster Generation and Network Component Insertion](#)”, IEEE International Symposium on Quality Electronic Design (ISQED), pp. 144–149, Santa Clara, CA, March 14–16, 2011.

- [C4] Bei Yu, Sheqin Dong, Song Chen, Satoshi Goto, “[Floorplanning and Topology Generation for Application-Specific Network-on-Chip](#)”, IEEE/ACM Asia and South Pacific Design Automation Conference (**ASPDAC**), pp. 535–540, Taipei, Jan. 2010.
- [C3] Tao Lin, Sheqin Dong, Song Chen, Bei Yu, Satoshi Goto, “[A Revisit to Voltage Partitioning Problem](#)”, ACM Great Lakes Symposium on VLSI (GLSVLSI), pp. 115–118, Providence, RI, May 16–18, 2010.
- [C2] Bei Yu, Sheqin Dong, Satoshi Goto, “[Multi-Voltage and Level-Shifter Assignment Driven Floorplanning](#)”, IEEE International Conference on ASIC (ASICON), pp. 1264–1267, Changsha, Oct. 20–23, 2009.
- [C1] Bei Yu, Sheqin Dong, Song Chen, Satoshi Goto, “[Voltage-Island Driven Floorplanning Considering Level-Shifter Positions](#)”, ACM Great Lakes Symposium on VLSI (GLSVLSI), pp. 51–56, Boston, MA, May 10–12, 2009.

Books / Book Chapters

- [B4] Haoyu Yang, Yibo Lin, Bei Yu, “Machine Learning for Mask Synthesis and Verification”, in Machine Learning Applications in Electronic Design Automation, Mark Ren eds., Springer, 2022.
- [B3] Shiyan Hu, Bei Yu, “[Big Data Analytics for Cyber-Physical Systems](#)”, Springer, 2020.
- [B2] Bei Yu, David Z. Pan, “[Design for Manufacturability with Advanced Lithography](#)”, Springer, 2016.
- [B1] Bei Yu, David Z. Pan, “[Layout Decomposition for Triple Patterning](#)”, in Encyclopedia of Algorithms, M.-Y. Kao eds., Springer, 2015.

Dissertation

- [PHD] Bei Yu, “[Design for Manufacturing with Advanced Lithography](#)”, University of Texas at Austin, August 2014. (**EDAA Outstanding Dissertation Award**)

ADVISING AND SUPERVISORSHIP

Current Students:

Yuxuan Zhao	Ph.D	Fall 2021 – Present
Ziyi Wang	Ph.D	Fall 2021 – Present
Hongduo Liu	Ph.D	Fall 2021 – Present
Xufeng Yao	Ph.D	Fall 2021 – Present
Xinyun Zhang	Ph.D	Fall 2021 – Present
Guojin Chen	Ph.D	Fall 2021 – Present
Ziyang Yu	Ph.D	Fall 2021 – Present
Zixiao Wang	Ph.D	Fall 2022 – Present
Peng Xu	Ph.D	Fall 2022 – Present
Shixin Chen	Ph.D	Fall 2022 – Present
Su Zheng	Ph.D	Fall 2022 – Present
Yu Zhang	Ph.D	Fall 2022 – Present
Shuo Yin	Ph.D	Fall 2022 – Present
Fangzhou Liu	Ph.D	Fall 2023 – Present
Lancheng Zou	Ph.D	Fall 2023 – Present
Zehua Pei	Ph.D	Fall 2023 – Present
Yuan Pu	Ph.D	Fall 2023 – Present
Jiaxi Jiang	Ph.D	Fall 2023 – Present
Mingjun Li	Ph.D	Fall 2023 – Present
Yuntao Lu	Ph.D	Fall 2023 – Present
Yuhao Ji	Ph.D	Fall 2024 – Present
Haoyuan Wu	Ph.D	Fall 2024 – Present
Yifan Shi	Ph.D	Fall 2024 – Present
Mengjia Dai	Ph.D	Fall 2024 – Present
Jiahao Xu	Ph.D	Fall 2024 – Present
Feng Gu	Ph.D	Fall 2025 – Present
Peiyi Han	Ph.D	Fall 2025 – Present
Zhiyuan Liu	Ph.D	Fall 2025 – Present
Jiajun Qin	Ph.D	Fall 2025 – Present
Yuhan Qin	Ph.D	Fall 2025 – Present
Mingjun Wang	Ph.D	Fall 2025 – Present
Mingzi Wang	Ph.D	Fall 2025 – Present
Siying Yu	Ph.D	Fall 2025 – Present
Zhijie Zhang	Ph.D	Fall 2025 – Present

Co-supervised:

Shaoteng Liu	Ph.D	Fall 2021 – Present
Chengyao Wang	Ph.D	Fall 2022 – Present
Wendong Xu	Ph.D @HKU	Fall 2023 – Present
Mingkang Zhu	Ph.D	Fall 2023 – Present
Sitong Wu	Ph.D	Fall 2023 – Present
Bin Xia	Ph.D	Fall 2023 – Present
Zhongshen Zeng	Ph.D	Fall 2023 – Present
Senqiao Yang	Ph.D	Fall 2024 – Present
Ruiyan Wang	Ph.D	Fall 2024 – Present
Tianyuan Qu	Ph.D	Fall 2024 – Present
Zheng Zhu	Ph.D	Fall 2024 – Present
Yuqi Liu	Ph.D	Fall 2024 – Present

Supervisions Completed:

Binwu Zhu	PhD 2024	Associate Professor @Southeast Univ
Yang Bai	PhD 2024	Postdoc @CUHK
Chen Bai	PhD 2024	Postdoc @HKUST
Siting Liu	PhD 2024	Huawei
Wenqian Zhao	PhD 2024	Huawei Noah
Peiyu Liao	PhD 2024	Huawei Noah
Wanli Chen	PhD 2024	point72
Zhuolun He	PhD 2023	Postdoc @CUHK
Lu Zhang	MPhil 2023	
Qi Sun	PhD 2022	Postdoc @Cornell → ZJU100 Young Professor @Zhejiang Univ
Ran Chen	PhD 2022	Huawei Noah
Hao Geng	PhD 2021	Postdoc @CUHK → Assistant Professor @ShanghaiTech
Tinghuan Chen	PhD 2021	Postdoc @CUHK → Assistant Professor @CUHK(SZ)
Wei Li	MPhil 2021	PhD @CMU
Yuzhe Ma	PhD 2020	Huawei → Assistant Professor @HKUST(GZ)
Haoyu Yang	PhD 2020	Postdoc @CUHK → Cadence → nVIDIA

Post-Doc Supervisions:

Tianshu Hou	2025/04 –
Yuyang Ye	2024/10 –
Yang Bai	2024/09 –
Zhuolun He	2023/09 –
Tinghuan Chen	2021/09 – 2022/12 now Faculty @CUHK-SZ
Hao Geng	2021/09 – 2022/03 now Faculty @ShanghaiTech
Haoyu Yang	2020/08 – 2021/03 now Research Scientist@nVIDIA

PROFESSIONAL SERVICE**University Committee Assignments**

- Chair, Internship and Industry Liaison, 2023–present.
- Member, CUHK CSE Department Graduate Panel, 2016–2023.
- Member, CUHK CSE Department Curriculum Committee, 2015–present.

Editorial Board

- **Editor**, Technical Committee on Cyber-Physical Systems (TC-CPS) Newsletter, 2019–present.
- Associate Editor, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2024–present.
- Associate Editor, ACM Transactions on Design Automation of Electronic Systems (TODAES), 2020–present.
- Associate Editor, Integration, the VLSI Journal, 2016–present.
- Associate Editor, IET Cyber-Physical Systems: Theory & Applications, 2016–2023.

Guest Editor

- IEEE Consumer Electronics Magazine Special Issue on ISVLSI
- IEEE Design & Test Special Issue on Machine Learning for CAD / EDA
- IEEE Transactions on Sustainable Computing (TSUSC) Special Issue on Sustainable Cyber-Physical Systems
- Integration, the VLSI Journal Special Issue on Emerging Technologies for System Level Design and Interconnects.
- Integration, the VLSI Journal Special Issue on ASP-DAC 2017.
- Journal of Parallel and Distributed Computing (JPDC) Special Issue on Scalable Cyber-Physical Systems

Selected Organizers

- **Chair**, IEEE Technical Committee on Secure and Dependable Measurement (TC-SDM), 2021–Present.
- **Chair**, ACM Student Research Competition at ICCAD, 2018, 2019.
- **Chair**, EDATHON, 2022.
- Assistant Vice President Publicity, IEEE CEDA, 2024–Present.
- Organizing Committee, ACM International Symposium on Physical Design (ISPD), 2026–.
- Organizing Committee, IEEE CEDA Hong Kong Chapter, 2017–2024.
- Organizing Committee, International System Design Contest at DAC, 2018, 2019.
- Organizing Committee, EDATHON, 2017, 2018, 2019, 2020, 2021.

Selected PC Member

- **TPC Co-Chair**, International Symposium of EDA (ISED), 2025.
- **TPC Co-Chair**, ACM/IEEE Workshop on Machine Learning for CAD (MLCAD), 2019.
- AAAI Conference on Artificial Intelligence (AAAI), 2023, 2024, 2025.
- ACM/IEEE Workshop on Machine Learning for CAD (MLCAD), 2019, 2020, 2021.
- ACM/IEEE Design Automation Conference (DAC), 2016, 2017, 2018.
- ACM International Symposium on Physical Design (ISPD), 2017, 2018, 2019, 2020, 2023, 2024, 2025.
- ACM Great Lakes Symposium on VLSI (GLSVLSI), 2016, 2017, 2018 (CAD Track Chair).
- IEEE/ACM International Conference On Computer Aided Design (ICCAD), 2016, 2017, 2018, 2024.
- IEEE/ACM Proceedings Design, Automation and Test in Europe (DATE), 2020, 2021.
- IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), 2018, 2019, 2020, 2021, 2022 (DFM track chair), 2024 (DFM track chair), 2025 (DFM track chair), 2026 (DFM track chair).
- IEEE International Conference on Computer Design (ICCD), 2021, 2022.
- IEEE International Conference on LLM-Aided Design (LAD), 2024, 2025.
- International Joint Conference on Artificial Intelligence (IJCAI), 2020.