Performance-driven Analog Routing via Heterogeneous 3DGNN and Potential Relaxation

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Analog Routing Problem

Analog circuit routing is critical to optimal performance, but obtaining a decent circuit layout requires significant time and expertise.

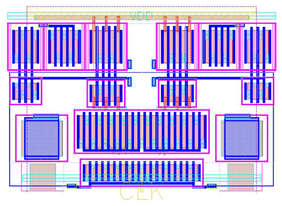


Figure 1. The placed comparator.

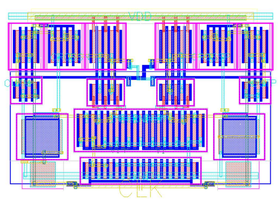


Figure 2. The routing solution.

Existing Heuristic Constraint-based Methods

Ou et al. propose different levels of geometrical matching constraints [4].

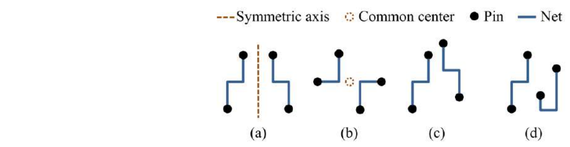


Figure 3. (a) Symmetric constraint. (b) Common-centroid constraint. (c) Topology-matching constraint. (d) Length-matching constraint.

Other works optimize power routing [3] and propose shielding critical nets [2].

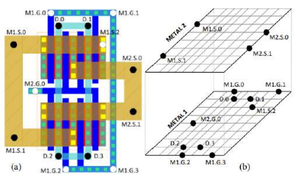


Figure 4. Optimize power routing.

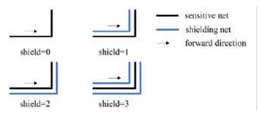
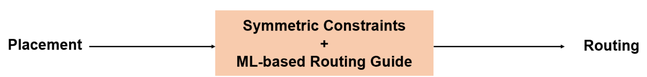


Figure 5. Shielding critical nets.

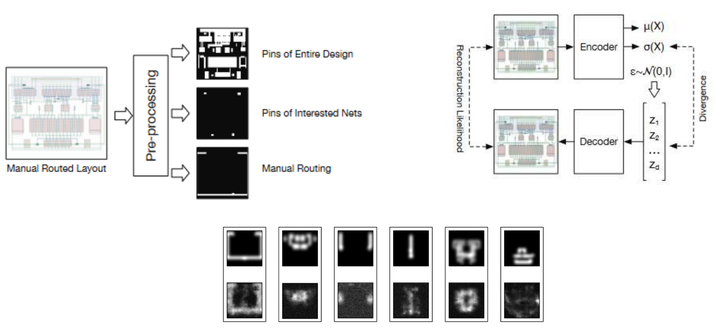
A ML-Guided Analog Routing Problem

Can we automatically summarize the human layout intelligence leveraging ML? [5]

Heuristic constraints Use a set of detailed heuristics as routing constraints.



Routing guidance Routing strategies learned from human



- Extract training data where the human would likely route the nets.
- Predict a 2D probability map of the routing likelihoods.
- Leveraging variational autoencoder (VAE) to reconstruct the routing solutions.

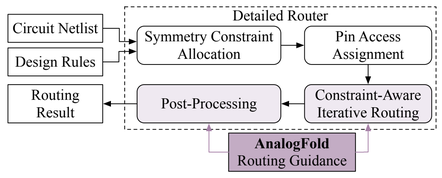
Existing Problems

- Problem #1 The human experts' layout data is **pretty scarce**.
- Problem #2 Fail to deal with **designs of different sizes or aspect ratios** and **resource competition** between different pins close to each other.
- Problem #3 The generative model makes it hard to guarantee a **performance boost**.

Methodology

- We introduce a **performance-driven analog routing** approach.
- A non-uniform routing guidance is proposed to address sparsity issues by assigning routing guidance to different nets.
- A a customized **AnalogFold** framework is proposed to enable accurate modeling of the performance potential of routing guidance.

Problem #1: Performance-Driven Analog Routing



- We introduce a performance-driven analog routing approach.
- Learn from the **automatically generated routing patterns** and their **simulation results**.

Problem #2: Non-uniform Routing Guidance

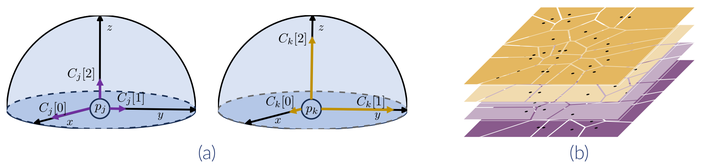
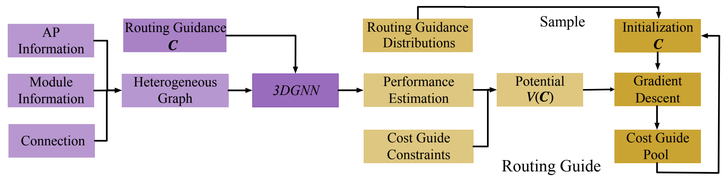


Figure 6. (a) Two examples of non-uniform routing guidance; (b) The 3D visualization.

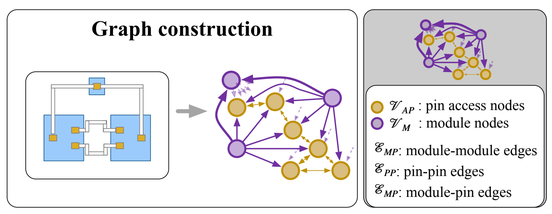
- We propose a non-uniform and adaptive routing guidance, which assigns different routing guidance $\vec{c}_i$ along different directions for each net n_i.
- Adapt the route guide distribution to areas with different densities and support a 3D cost map.

Problem #3: AnalogFold for Performance Relaxation



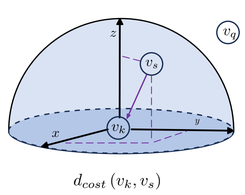
- AnalogFold contains a heterogeneous routing graph, a protein-inspired 3DGNN network, and a pool-aided potential relaxation process.

Heterogeneous Graph for Analog Routing We design a heterogeneous graph $\mathcal{G}_H =< \mathcal{V}_{AP}, \mathcal{V}_M, \mathcal{E}_{PP}, \mathcal{E}_{PM}, \mathcal{E}_{MM} >$ to represent the interactions between pin access points and modules.



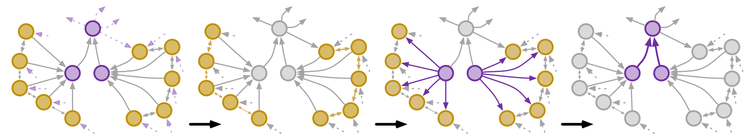
Cost-aware Distance Augmented Module We can define the distance honors routing cost as follows:

$$d_{cost}(v_k, v_s) = \sqrt{(\vec{c}[0] \cdot h_{ks})^2 + (\vec{c}[1] \cdot w_{ks})^2 + (\vec{c}[2] \cdot z_{ks})^2}. \quad (1)$$

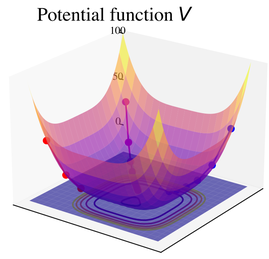


The distance between nodes is embedded to reflect the routing resource competition.

Protein-inspired 3DGNN for Analog Routing Especially, the 3D information in P is incorporated to update each message e_k.



Routing Guide Performance Potential Modeling and Relaxation



- We created a differentiable model using the 3DGNN to predict the post-layout performance of the routing guidance.
- We then apply a gradient-based optimization of routing guidance potential **multiple times with different initialization** to derive the top-N routing guidance results.

Dataset

- We use operational transconductance amplifiers (OTAs) as our main benchmark designs.

Table 1. Benchmark circuits information of the number of PMOS, number of NMOS, number of capacitors, number of resistors, number of standard cells, number of total modules.

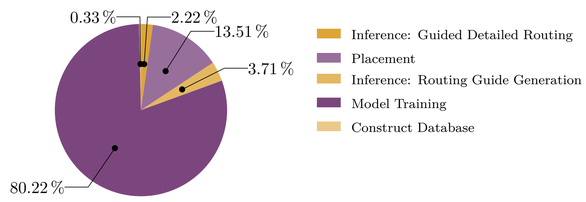
Benchmark	#PMOS	#NMOS	#Cap	#Res	#Total
OTA1	6	8	2	0	25
OTA2	6	8	2	0	25
OTA3	16	10	6	4	36
OTA4	16	10	6	4	36

Post-layout Performance Comparisons on OTA benchamarks

Table 2. The summarized comparisons between baseline methods and the proposed method on OTA{1-4}&{A-C}.

Circuits		Schematic	MagicalRoute [1]	GeniusRoute [5]	**PARoute (ours)**
Average	Offset Voltage(μV) ↓	-	1.000	10.426	**0.546**
	CMRR(dB) ↑	-	1.000	0.998	**1.163**
	BandWidth(MHz) ↑	-	1.000	1.002	**1.113**
	DC Gain(dB) ↑	-	1.000	0.999	**2.368**
	Noise(μV_{rms}) ↓	-	1.000	1.007	**0.787**
	Runtime(s) ↓	-	**1.000**	17.147	7.480

Runtime Breakdown



- Althogh the average runtime of our proposed approach is 7.48× slower than MagicalRoute [1], it is nearly 2.29× faster than GeniusRoute [5] due to the simplified 3D graph structure.

References

[1] Hao Chen, Keren Zhu, Mingjie Liu, Xiyuan Tang, Nan Sun, and David Z Pan. Toward silicon-proven detailed routing for analog and mixed-signal circuits. In *Proc. ICCAD*, pages 1–8, 2020.

[2] Qiang Gao, Yin Shen, Yici Cai, and Hailong Yao. Analog circuit shielding routing algorithm based on net classification. In *Proc. ISPD*, pages 123–128, 2010.

[3] Ricardo Martins, Nuno Lourenço, António Canelas, and Nuno Horta. Electromigration-aware and ir-drop avoidance routing in analog multiport terminal structures. In *Proc. DATE*, pages 1–6. IEEE, 2014.

[4] Hung-Chih Ou, Hsing-Chih Chang Chien, and Yao-Wen Chang. Non-uniform multilevel analog routing with matching constraints. In *Proc. DAC*, pages 549–554, 2012.

[5] Keren Zhu, Mingjie Liu, Yibo Lin, Biying Xu, Shaolan Li, Xiyuan Tang, Nan Sun, and David Z Pan. GeniusRoute: A new analog routing paradigm using generative neural network guidance. In *Proc. ICCAD*, pages 1–8, 2019.