

### RankTuner: When Design Tool Parameter Tuning Meets Preference Bayesian Optimization

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1 Introduction







Introduction

## Starting from EDA Tool Parameter Tuning





# High-dimensional Black-box Optimization





- High-dimensional: A lot of values of design parameters need to be determined or tuned (n<sub>Params</sub> ≥ 150)
- Multiple quality-of-result (QoR) metrics (e.g., area, power, and delay) to be optimized
- "Black-box" parameter-to-performance mappings: no explicit function expressions
- **Time-consuming** EDA tool evaluation, i.e., expensive data annotation

## EDA Tool Parameter Tuning



- EDA tools provide effective and complex optimization options
- Efficient Tool Parameter Tuning
  - XGBoost<sup>1</sup>
  - Neural Networks (NN)<sup>2</sup>
  - Gaussian process (GP)<sup>3</sup>
- These approaches typically view tool parameter tuning as a regression task!

<sup>3</sup>Hao Geng et al. (2022). "PTPT: physical design tool parameter tuning via multi-objective Bayesian optimization". In: *IEEE TCAD* 42.1, pp. 178–189.

<sup>&</sup>lt;sup>1</sup>E. Ustun et al. (2019). "LAMDA: Learning-Assisted Multi-stage Autotuning for FPGA Design Closure". In: *Proc. FCCM*, pp. 74–77.

<sup>&</sup>lt;sup>2</sup>Jihye Kwon, Matthew M. Ziegler, and Luca P. Carloni (2019). "A Learning-Based Recommender System for Autotuning Design Flows of Industrial High-Performance Processors". In: *Proc. DAC*.

## Motivation



- Existing methods focus on predicting the exact QoR values
  - The enormous options make it difficult to train an accurate model<sup>4</sup>
  - A lack of uncertainty modeling leads to inaccurate Pareto relationship<sup>5</sup>
- What do we need? Ranking-based tuning framework!
  - Preference Bayesian Optimization  $\rightarrow$  Pairwise GP + Duel-Thompson Sampling



<sup>4</sup>Hao Geng et al. (2022). "PTPT: physical design tool parameter tuning via multi-objective Bayesian optimization". In: *IEEE TCAD* 42.1, pp. 178–189.

<sup>5</sup>Qi Sun et al. (2022). "Correlated multi-objective multi-fidelity optimization for HLS directives design". In: *ACM Transactions on Design Automation of Electronic Systems (TODAES)* 27.4, pp. 1–27. Algorithm

### The Pairwise Gaussian Process





A pairwise likelihood function is defined as:

$$p_{\text{ideal}}(\boldsymbol{x}_{v} \succeq \boldsymbol{x}_{u} | f(\boldsymbol{x}_{v}), f(\boldsymbol{x}_{u})) = \begin{cases} 1 & \text{if } f(\boldsymbol{x}_{v}) \ge f(\boldsymbol{x}_{u}) \\ 0 & \text{otherwise.} \end{cases}$$
(1)

# The Dominating Uncertainty Region





Using a Gaussian noise to model the dominance uncertainty, the pairwise likelihood function could be formulated as:

$$\Phi(z_k) = p\left(\mathbf{x}_v \succeq \mathbf{x}_u \mid f\left(\mathbf{x}_v\right), f\left(\mathbf{x}_u\right)\right),$$

$$= \iint p_{\text{ideal}} \left(\mathbf{x}_v \succeq \mathbf{x}_k \mid f\left(\mathbf{x}_v\right) + \delta_v, f\left(\mathbf{x}_u\right) + \delta_u\right)$$

$$\mathcal{N}\left(\delta_v; 0, \sigma^2\right) \mathcal{N}\left(\delta_u; 0, \sigma^2\right) \, \mathrm{d}\delta_v \mathrm{d}\delta_u,$$
where  $z_k = \frac{f(\mathbf{x}_u) - f(\mathbf{x}_u)}{\sqrt{2\sigma}}$  and  $\Phi(z) = \int_{-\infty}^2 N(\gamma; 0, 1) \mathrm{d}\gamma.$ 
(2)

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# Acquisition Function for Pareto-dominance Comparison





#### • Exploration and Exploitation of Comparisons

- Searching across the entire search space of parameter tuning requires an effective balance between **exploration and exploitation**
- The key aspect is to select informative parameter pairs for comparison

### Pareto-Dominace Thompson Sampling





**1** Selecting x The first element of the new comparison,  $x_{next}$ , is selected as:

$$\boldsymbol{x}_{\text{next}} = \arg \max_{\boldsymbol{x} \in \mathcal{X}} \int_{\mathcal{X}} \pi_{\tilde{f}} \left( [\boldsymbol{x}, \boldsymbol{x}'] \right) d\boldsymbol{x}'.$$
(3)

**Selecting** x': The second element is selected as the parameter configuration that maximizes the variance of  $\sigma(f_*)$  in the direction of  $x_{next}$ ,

$$\boldsymbol{x}_{\text{next}}' = \arg \max_{\boldsymbol{x}_{\star}' \in \mathcal{X}} \mathbb{V}\left[\sigma\left(f_{\star}\right) \mid \left[\boldsymbol{x}_{\star}, \boldsymbol{x}_{\star}'\right], \boldsymbol{x}_{\star} = \boldsymbol{x}_{\text{next}}\right].$$
(4)  
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# The Overall Flow of Our RankTuner Framework



- 1 Random Embedding Generation
- 2 Trust-region Initialization
- **③** Informative Comparision Selection between Regions
- 4 Multi-fidelity Evaluation and Update



**Experiments** 

# **Experimental Setup**



- Benchmarks: RISC-V processors (RISCV321<sup>6</sup> and Rocket<sup>7</sup>), and BlackParrot<sup>8</sup> processors (BP).
- The QoR-related metrics are used to compare the parameter tuning methods as in<sup>9</sup>:
  - Hypervolume (HV)
  - Maximum performance improvement (MPI1), Maximum power improvement (MPI2), Maximum area improvement (MAI).
  - Maximum performance-power improvement (MPPI), and Maximum performance-area improvement (MPAI)

<sup>&</sup>lt;sup>6</sup>James E. Stine, Ryan Ridley, and Teodor-Dumitru Ene (2021). *OSU Datapath/Control RV32 Single-Cycle and Pipelined Architecture in SV*.

<sup>&</sup>lt;sup>7</sup>Krste Asanovic et al. (2016). "The rocket chip generator". In: *EECS Department, University of California, Berkeley, Tech. Rep. UCB/EECS-2016-17* 4.

<sup>&</sup>lt;sup>8</sup>Daniel Petrisko et al. (2020). "BlackParrot: An Agile Open-Source RISC-V Multicore for Accelerator SoCs". In: *Proc. MICRO* 40.4, pp. 93–102.

<sup>&</sup>lt;sup>9</sup>Su Zheng et al. (2023). "Boosting VLSI Design Flow Parameter Tuning with Random Embedding and Multi-objective Trust-region Bayesian Optimization". In: 28.5, pp. 1–23.

# Comparison Between Ours and Previous Methods



Method	FIST	DAC'19	MLCAD'19	ICCAD'21	PTPT	REMOTune	DATE'24	Ours
$HV(10^5)$	1.57	1.55	1.63	1.68	1.48	1.75	1.44	1.84
$HV_{0,1}$ (10 <sup>3</sup> )	2.85	2.72	3.00	2.95	2.70	3.05	2.63	3.44
$HV_{0,2}$ (10 <sup>3</sup> )	2.94	2.99	3.00	3.07	2.95	3.12	2.84	3.43
$HV_{1,2}$ (10 <sup>3</sup> )	2.97	2.97	3.00	3.14	2.79	3.23	2.77	3.00
MPI1(%)	3.16	2.54	5.00	3.81	3.56	4.38	2.08	13.64
MPI2(%)	3.90	2.12	5.12	5.23	0.85	6.27	0.68	5.04
MAI(%)	5.47	7.18	4.64	7.10	5.15	7.45	4.74	5.12
MPPI(%)	6.94	4.51	9.88	8.83	4.37	10.38	1.30	13.73
MPAI (%)	8.46	9.53	9.41	10.63	8.52	11.53	5.43	12.26

Table: Comparison of Parameter Tuning Methods on RISCV32I Benchmark.

- RankTuner consistently outperforms them across all benchmarks up to 40.34% improvement of hypervolume.
- RankTuner acquires 4.89% and 3.59% higher hypervolumes than the best baseline method, REMOTuner<sup>10</sup>, on RISCV321 and Rocket benchmarks.

<sup>&</sup>lt;sup>10</sup>Su Zheng et al. (2023). "Boosting VLSI Design Flow Parameter Tuning with Random Embedding and Multi-objective Trust-region Bayesian Optimization". In: 28.5, pp. 1–23.

### The Attained Hypervolume v.s. Iteration





The RankTuner framework also offers a notable advantage in constantly improving the explored Pareto front:

- The RankTuner framework offers a notable advantage in constantly improving the explored Pareto front.
- Although RankTuner has nearly the lowest initial HV value, it continuously improves during the exploration process and eventually surpasses all other methods at around 100 iterations.

## The Runtime Comparison & Breakdown

- RankTuner is nearly  $4.83 \times$  faster than PTPT<sup>11</sup> due to the parallel exploration
- The most consuming part is the EDA Physical Design part, which takes 75.5% of the total runtime. The initialization and optimization time only take about 1.25% in total.



<sup>&</sup>lt;sup>11</sup>Hao Geng et al. (2022). "PTPT: physical design tool parameter tuning via multi-objective Bayesian optimization". In: *IEEE TCAD* 42.1, pp. 178–189.

Conclusion





- We propose RankTuner, a ranking-based EDA tool parameter tuning framework.
- We introduce a pairwise Gaussian process and a Duel-Thompson sampling to sample informative comparisons.
- RankTuner outperforms state-of-the-art methods in terms of search quality in competitive runtime.

**THANK YOU!**