THE CHINESE UNIVERSITY OF HONG KONG
Department of Electronic Engineering
Seminar

Mixed-signal Processing for High-performance A/D Interfaces

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Date: **June 26, 2024 (Wednesday)**
Time: **11:30 a.m. – 12:45 p.m.**
Venue: **Room 222, 2/F, Ho Sin Hang Engineering Building, CUHK**

Abstract

A mixed-signal processing approach for high-performance analog-to-digital (A/D) interfaces, focusing on innovation at A/D and digital-to-analog (D/A) interfaces by utilizing signal feature extraction and algorithm-circuit co-design, is presented to improve the performance of mixed-signal integrated circuits (ICs) and systems. To demonstrate how significantly system performance is improved with the above idea, a high-channel count, high-density implantable single-cell resolution neural interface for future high-bandwidth brain-computer interfaces (BCI) will be introduced in detail. The IC features wired-OR lossy compression during digitization, thus preventing data deluge and massive data movement. By discarding unwanted baseline samples of the neural signals, the output data rate is reduced by 146× on average while allowing the reconstruction of spike samples. The recording array consists of pulse-position modulation (PPM)-based ADPs with a global single-slope (SS) analog-to-digital conversion scheme, which enables a low-power and compact pixel design with significantly simple routing and low array readout energy. The neural recording IC features 1024 channels with a pixel pitch of 36 μm that can be directly matched to a high-density MEA. The IC achieves the smallest area per channel ($36 \times 36\ \mu m^2$) and the highest energy efficiency among the state-of-the-art high density neural recording ICs published to date.

Biography

Moonhyung Jang (Member, IEEE) received the B.Sc. (*summa cum laude*) and Ph.D. degrees in electrical and electronic engineering from Yonsei University, Seoul, South Korea, in 2014 and 2021, respectively. His Ph.D. research was in the field of high-resolution power-efficient continuous-time delta–sigma A/D conversion. He is currently a Post-Doctoral Research Fellow with the Murmann Mixed-Signal Group, Stanford University, Stanford, CA, USA. His current research interests include low-power data converters, high-bandwidth single-cell resolution brain–machine interfaces (BMI), in-memory computing-based deep neural network (DNN) accelerators, and various high-performance mixed-signal integrated circuits and systems. Dr. Jang was a recipient of the 2020–2021 IEEE Solid-State Circuits Society Predoctoral Achievement Award, the 2020 Yonsei-Samsung Semi-Conductor Research Center Best Paper Award, the 2020 Samsung Human-Tech Paper Award Silver Prize in Circuit Design, and the 2018 Samsung Human-Tech Paper Award Bronze Prize in Circuit Design. He has served as a reviewer for the IEEE JOURNAL OF SOLID-STATE CIRCUITS and IEEE TRANSACTIONS ON VERY LARGE-SCALE INTEGRATION SYSTEMS.

***** ALL ARE WELCOME *****

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