THE CHIPS TO SYSTEMS CONFERENCE

SHAPING THE NEXT GENERATION OF ELECTRONICS

JUNE 23-27, 2024

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Performance-driven Analog Routing via Heterogeneous 3DGNN and Potential Relaxation

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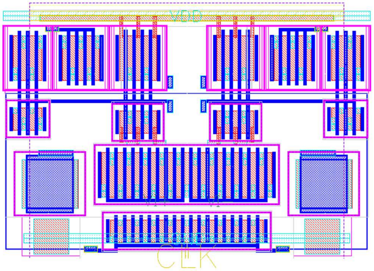
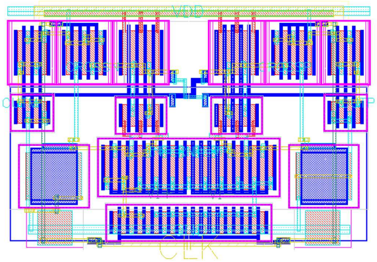
Outline

Backgroud Knowledge

Analog Routing Problem



A result of the placed comparator.

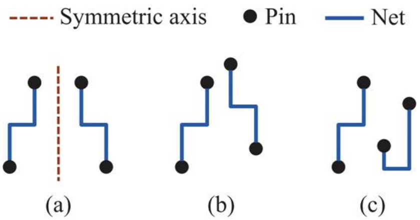


The routing solution.

Analog circuit routing is critical to optimal performance, but obtaining a decent circuit layout requires significant time and expertise.

Existing Methods: Heuristic Constraint-based Methods

Ou et al. propose different levels of geometrical matching constraints[1].

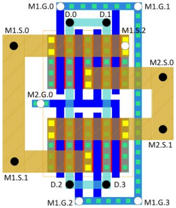


(a) Symmetric constraint. (b) Common-centroid constraint. (c) Topology-matching constraint.

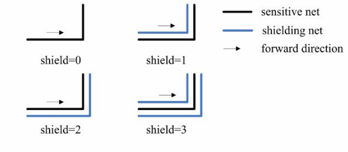
[1] H.-C. Ou *et al.*, "Non-uniform multilevel analog routing with matching constraints", in *Proceedings of the 49th Annual Design Automation Conference*, 2012, pp. 549–554.

Existing Methods: Heuristic Constraint-based Methods

There are other works that optimize power routing[2] and propose shielding critical nets[3].



Optimize power routing.



Shielding critical nets.

[2] R. Martins *et al.*, "Electromigration-aware and ir-drop avoidance routing in analog multiport terminal structures", in *2014 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, IEEE, 2014, pp. 1–6.

[3] Q. Gao *et al.*, "Analog circuit shielding routing algorithm based on net classification", in *Proceedings of the 16th ACM/IEEE international symposium on Low power electronics and design*, 2010, pp. 123–128.

A ML-Guided Analog Routing Problem

Can we automatically summarize the human layout intelligence leveraging ML?[4]

Placement → **Explicated Constraints** → Routing

Heuristic constraints

Use a set of detailed heuristics as routing constraints.

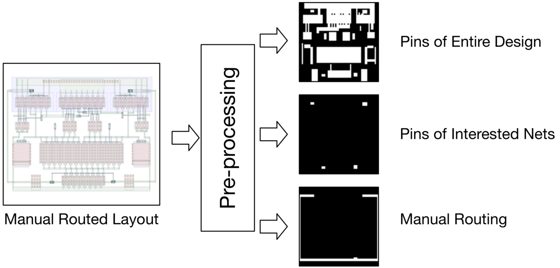
Placement → **Symmetric Constraints + ML-based Routing Guide** → Routing

Routing guidance

Routing strategies learned from human

[4] K. Zhu *et al.*, "Geniusroute: A new analog routing paradigm using generative neural network guidance", in *Proc. ICCAD*, 2019.

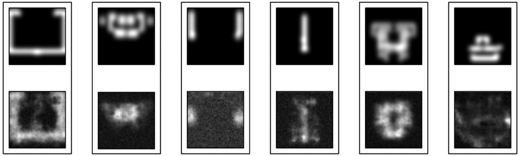
Automatically Learn Guidance from Human Layouts



Human Layout data

- Pre-process the GDS layouts into images
- Extract training data where the human would likely route the nets
- Problem #1 The human experts' layout data is **pretty scarce**.

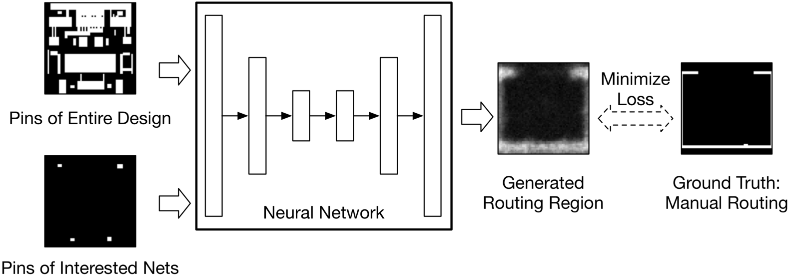
2D Uniform Routing Guidance



2D Uniform Routing Guidance

- Predict a 2D probability map of the routing likelihoods in each region.
- The 2D uniform routing guidance is honored via penalties in the cost function.
- Problem #2 Fail to deal with **designs of different sizes or aspect ratios** and **resource competition** between different pins close to each other.

VAE-based Generation

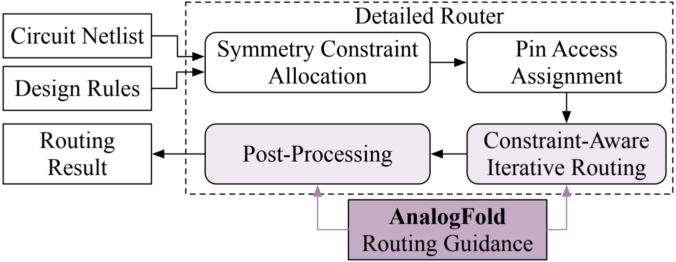


VAE-based Generation

- Leveraging variational autoencoder (VAE) to reconstruct the routing solutions.
- Minize the distance between ground truth and inferred output.
- Problem #3 The generative model makes it hard to guarantee a **performance boost**.

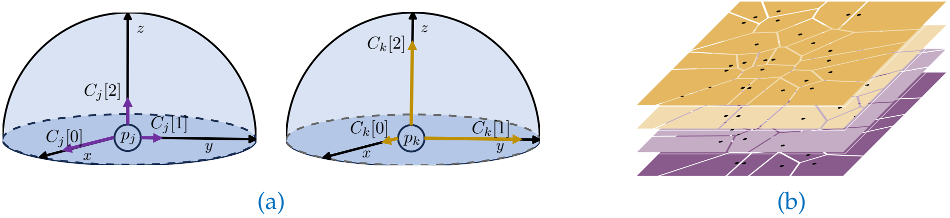
Proposed Method: PARoute

Problem #1: Performance-Driven Analog Routing



- We introduce a performance-driven analog routing approach.
- Learn from the **automatically generated routing patterns** and their **simulation results** without **human labeling effort**.

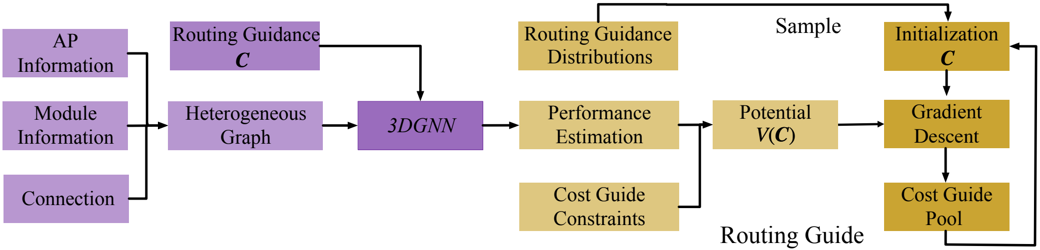
Problem #2: Non-uniform Routing Guidance



(a) Two examples of non-uniform routing guidance; (b) The 3D visualization.

- We propose a non-uniform and adaptive routing guidance, which assigns different routing guidance $\boldsymbol{c}_i$ along different directions for each net n_i.
- Adapt the route guide distribution to areas with different densities and support a 3D cost map.

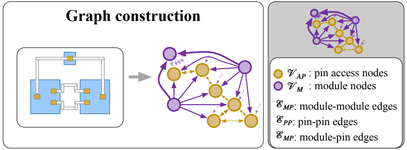
Problem #3: AnalogFold Framework for Performance Relaxation



- We proposed a customized AnalogFold framework to enable accurate modeling of the performance potential of routing guidance.
- AnalogFold contains a heterogeneous routing graph, a protein-inspired 3DGNN network, and a pool-aided potential relaxation process.

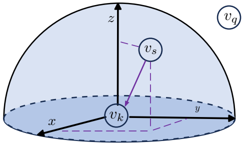
Heterogeneous Graph for Analog Routing

We design a heterogeneous graph $\mathcal{G}_H =< \mathcal{V}_{AP}, \mathcal{V}_M, \mathcal{E}_{PP}, \mathcal{E}_{PM}, \mathcal{E}_{MM} >$ to represent the interactions between pin access points and modules.



- The vertex sets $\mathcal{V}_{AP}$ and $\mathcal{V}_M$ correspond to the pin access points and modules.
- $\mathcal{E}_{PP}$ is designed to reflect the interactions between different pin access points.
- $\mathcal{E}_{MM}$ contains the edges that connect the modules according to the netlist.
- We add the edge $\mathcal{E}_{PM}$ to model the relationship between the pin access points and the modules.

Cost-aware Distance Augmented Module



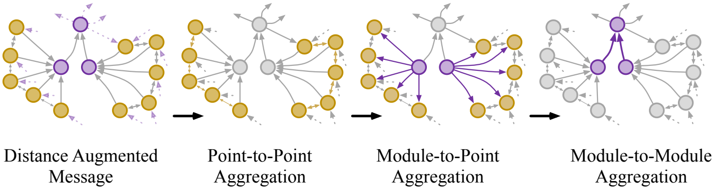
$d_{cost}(v_k, v_s)$

We can define the distance honors routing cost as follows:

$$d_{cost}(v_k, v_s) = \sqrt{(\boldsymbol{c}[0] \cdot h_{ks})^2 + (\boldsymbol{c}[1] \cdot w_{ks})^2 + (\boldsymbol{c}[2] \cdot z_{ks})^2}, \tag{1}$$

where $\boldsymbol{c}$ is the cost guide assigned for each access point, $h_{ks}/w_{ks}/z_{ks}$ is the distance between v_k and v_s along horizontal/vertical/Z-axis direction. **The distance between nodes is embedded to reflect the routing resource competition.**

Protein-inspired 3DGNN for Analog Routing

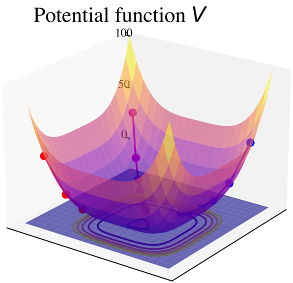


In 3D-GNN, the proposed cost-aware message passing can be defined as:

$$\begin{aligned} \mathbf{e}_k^l &= \phi^e\left(\mathbf{e}_k, v_{r_k}, v_{s_k}, \mathcal{E}_{s_k}, \rho^{p\to e}\left(\{\mathbf{r}_h\}_{h=r_k\cup s_k}\right)\right), \\ v_i^l &= \phi^v\left(v_i, \rho^{e\to v}\left(\mathcal{E}_i^l\right)\right), \mathbf{u}^l = \phi^u\left(\mathbf{u}, \rho^{v\to u}\left(\mathcal{V}^l\right)\right), \end{aligned} \tag{2}$$

where ϕ^e, ϕ^v, and ϕ^u are three information update functions on edges, pin access points/modules, and the whole graph, respectively. **Especially, the 3D information in P is incorporated to update each message e_k.**

Routing Guide Performance Potential Modeling and Relaxation



- We created a differentiable model using the 3DGNN to predict the post-layout performance of the routing guidance.
- We then apply a gradient-based optimization of routing guidance potential **multiple times with different initialization** to derive the top-N routing guidance results.

Experiment Results

Post-layout Performance Comparisons on OTA benchamarks

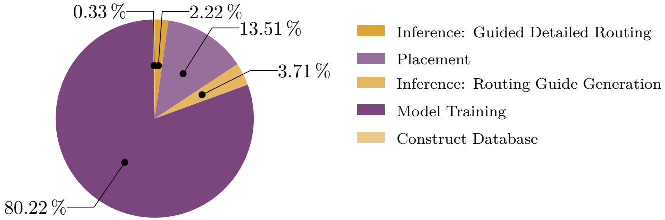
Table: The comparisons between baseline methods and the proposed method.

Circuits		Schematic	MagicalRoute[5]	GeniusRoute[6]	**PARoute (ours)**
Average	Offset Voltage(μV) ↓	-	1.000	10.426	**0.546**
	CMRR(dB) ↑	-	1.000	0.998	**1.163**
	BandWidth(MHz) ↑	-	1.000	1.002	**1.113**
	DC Gain(dB) ↑	-	1.000	0.999	**2.368**
	Noise(μV_{rms}) ↓	-	1.000	1.007	**0.787**
	Runtime(s) ↓	-	**1.000**	17.147	7.480

[5] H. Chen *et al.*, "Toward silicon-proven detailed routing for analog and mixed-signal circuits", in *Proc. ICCAD*, 2020, pp. 1–8.

[6] K. Zhu *et al.*, "Geniusroute: A new analog routing paradigm using generative neural network guidance", in *Proc. ICCAD*, 2019.

Runtime Breakdown



- Althogh the average runtime of our proposed approach is 7.48× slower than MagicalRoute[7], it is nearly 2.29× faster than GeniusRoute[8] due to the simplified 3D graph structure.
- The most consuming part is the model training part, which takes 80.22% of the total runtime and 3.71% of the total time for the routing cost generation.

[7]H. Chen *et al.*, "Toward silicon-proven detailed routing for analog and mixed-signal circuits", in *Proc. ICCAD*, 2020, pp. 1–8.

[8]K. Zhu *et al.*, "Geniusroute: A new analog routing paradigm using generative neural network guidance", in *Proc. ICCAD*, 2019.

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