ASP-DAC 2024
29th Asia and South Pacific Design Automation Conference

iPD: An Open-source intelligent Physical Design Toolchain

Xingquan Li, Simin Tao, Shijian Chen, Zhisheng Zeng, Zhipeng Huang, Hongxi Wu, Weiguo Li, Zengrong Huang, Liwei Ni, Xueyan Zhao, He Liu, Shuaiying Long, Ruizhi Liu, Xiaoze Lin, Bo Yang, Fuxing Huang, Zonglin Yang, Yihang Qiu, Zheqing Shao, Jikang Liu, Yuyao Liang, Biwei Xie, Yungang Bao, and **Bei Yu**

Jan. 23 2024

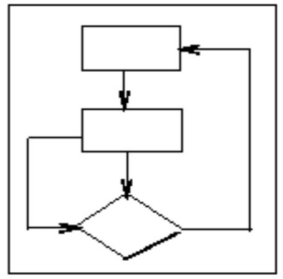
01 Introduction

02 iPD Design Mode

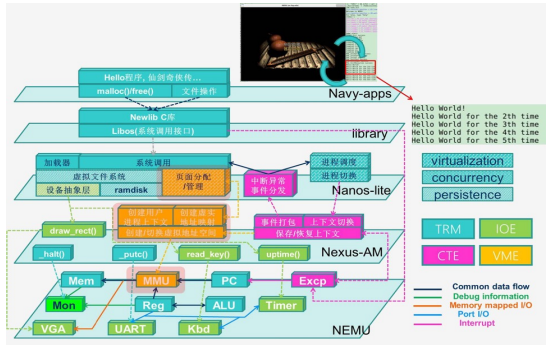
03 iPD Toolchain

Chip Design Flow

System Specifications



Architectural Design

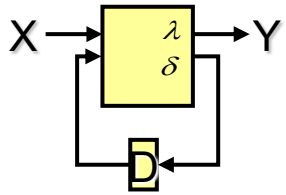


Functional Design

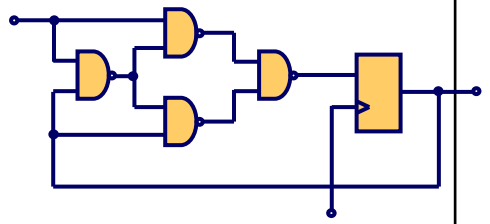
```
module conv;
reg [31:0] m[0:8192];
reg [12:0] pc;
reg [31:0] acc;
reg[15:0] ir;

always
  begin
    ir = m[pc];
    if(ir[15:13] == 3b' 000)
      pc = m[ir[12:0]];
    else if (ir[15:13] == 3' b010)
      acc = -m[ir[12:0]];
    ...
```

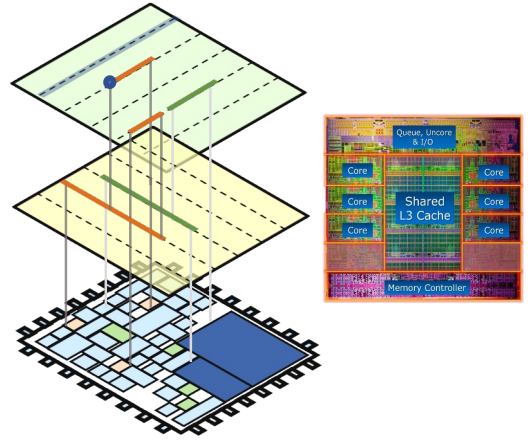
Logic Synthesis



Tech Mapping

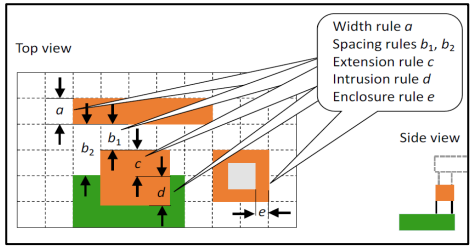


Physical Design

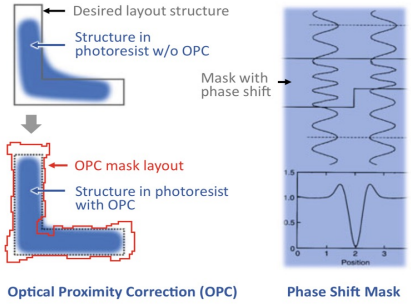


Sign-off Verification

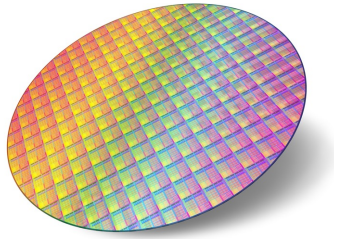
Timing, Power, DRC, ERC, LVS



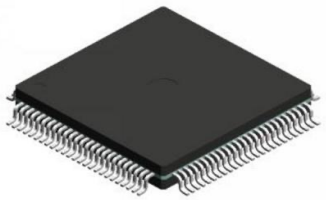
Layout Processing



Fabrication

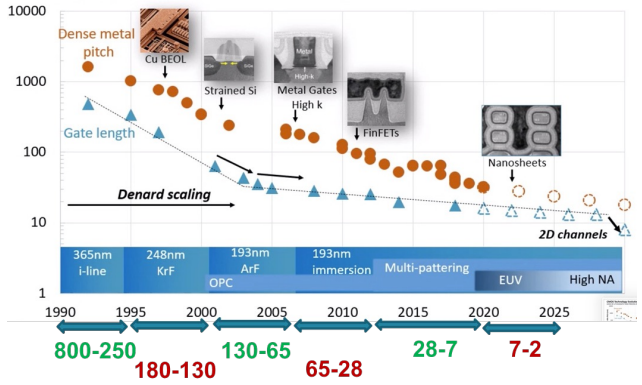


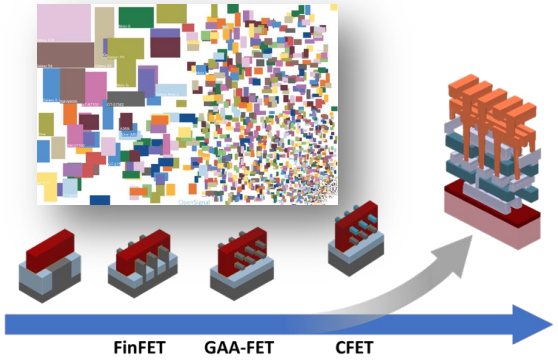
Package and Test



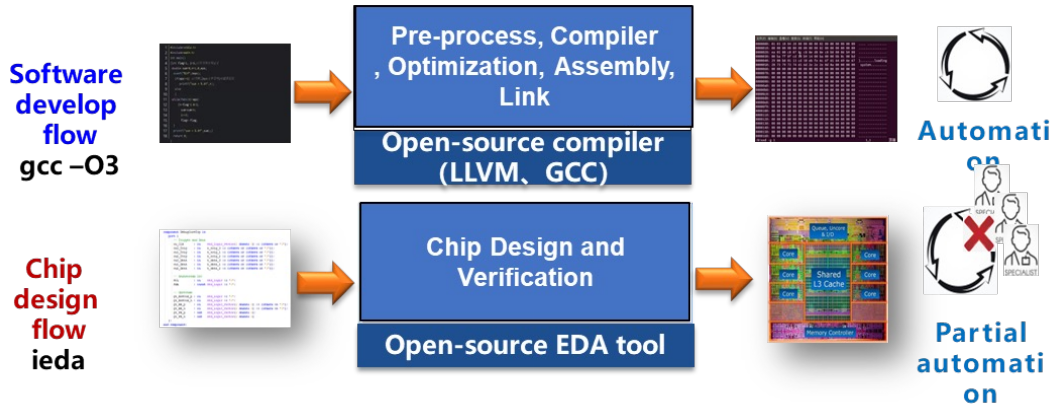
Challenges and Chances

- **Challenges**
  - Moore's Law
  - Gap between academic and industrial
  - Innovation more difficult
  - Design rules are evolving





- **Chances**



Open-source

AI

Open-source EDA Tools

Design Module	Design Step	Some Open-source Tools					iEDA
HLS	HLS	LegUp	GAUT	PandA	FCUDA	XLS	
Simulation Verification	Logic Simulation	Verilator/iVerilog	GHDL	FreeHDL	TkGate		
	Circuit Simulation	NGSpice	mixedsim	GnuCap	Qucs	XICE	
	Debug						
Logic Synthesis	Logic Synthesis	Yosys	ABC	EPFL-LS-Lib	LLDHL	UNIVR	iLS
	Tech Map	ABC					iMap
DFT	DFT	Fault					
Formal	Formal						
Physical Design	Partition	PartitionMgr	METIS	KaHyPar	MPPart		iNO
	Floorplan	OpenRoad TritonMacroPlacer	OpenRoad	Parquest			iFP
	PDN	OpenPDN					iPDN
	Placement	RePlace OpenDP	DreamPlace	Graywolf	Capo		iPL
	CTS	TritonCTS					iCTS
	Timing OPT	TritonSizer	Gate-Sizing				iTO
	Routing	FastRoute TritonRoute	CUGR Dr.CU	Qrouter	NTHU-Route	BoxRouter/FGR/ORGE	iRT
	ECO	OpenRoad-eco					iECO
Signoff	STA	OpenSTA	OpenTimer				iSTA
	RCX	OpenRCX	SPEF-Extractor				iRCX
	Power	OpenRoad-pp					iPA
	IR Drop	PDNSim	IREDGe				iIR
Physical Verification	DRC	Klayout	Magic				iDRC
	Antenna	OpenRoad-ant					
	LVS	Netgen					
Layout Synthesis	MPL						
	RET/ILT						
	Mask Generation						

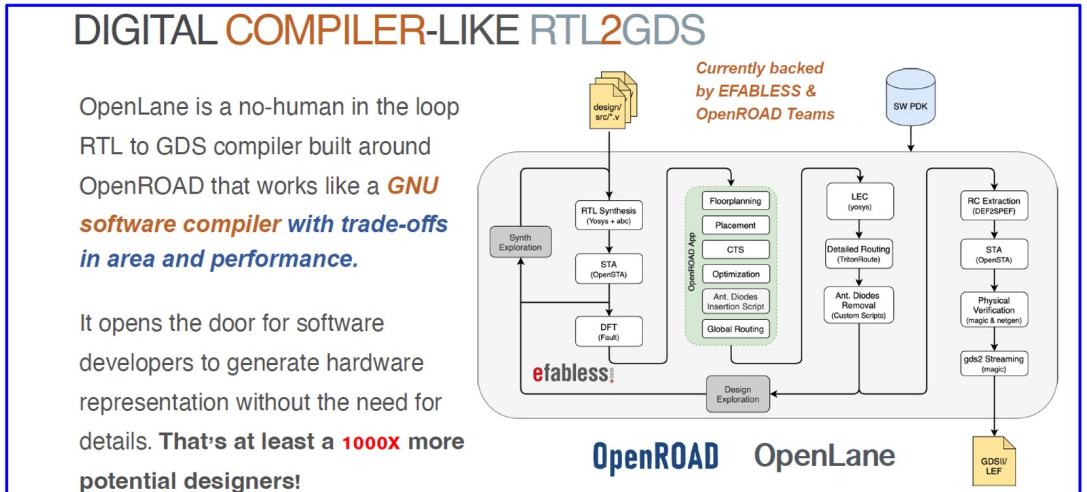
A Promising Open-source Precedent

- **OpenROAD: No Humans, 24 Hours**
- **Efabless-OpenLane: RTL2GDS Digital Flow**

OpenROAD: No Humans, 24 Hours

- **FOCUS: Ease of use and runtime**
- **Directly attack the crises of design and innovation**
  - **Schedule barrier: RTL-to-GDS in 24 hours**
  - **Expertise barrier: No-human-in-loop, tapeout GDS**
  - **Cost barrier: Open source (and, runs in 24 hours)**
- **Unleash system innovation and design innovation**
- **Enable tool customization to system, application needs**

Efabless: OpenLane



Mohamed Kassem, Efabless

From "Andrew B. Kahng, The OpenROAD Project: Today and Beyond, 2022"

Our Motivation

- Open-source EDA situation
  - Only support **one algorithmic** approach, but **no algorithm can perform best for any case**.
  - Challenges in **reliability**, **extendibility**, **ease-of-use**.
  - developed and maintained **by some professors and students.**

- The motivation of iPD
  - **Attract** diverse **academic disciplines**, and **bridge** the **gap** between industry and academia
  - **Support various algorithmic** solutions, and **provide long-term support**.
  - iPD is the set of **EDA tools** and **algorithm sets**
  - We aim to provide an EDA tool R&D platform.

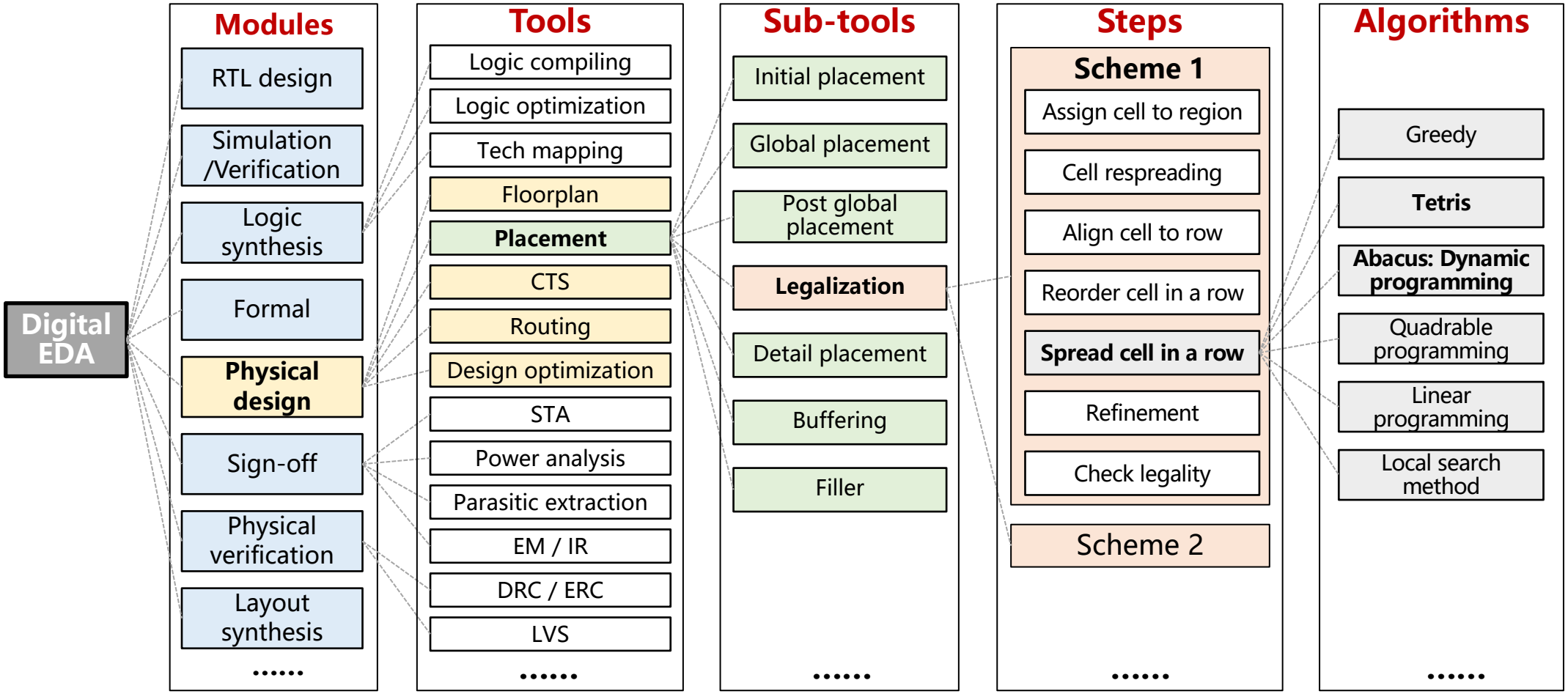
01 Introduction

02 iPD Design Mode

03 iPD Toolchain

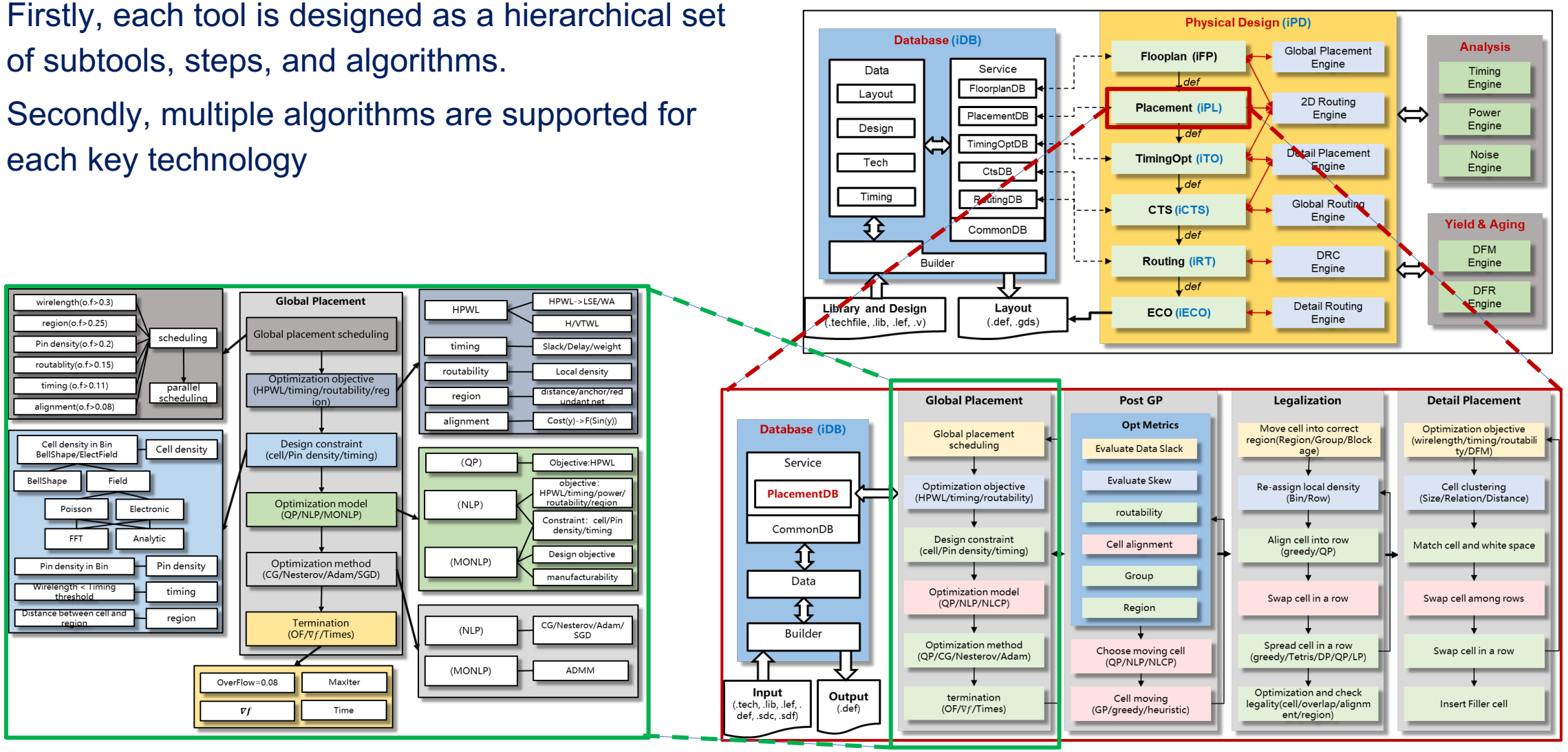
EDA Decomposition

- physical design -> multiple tools -> sub-tools -> steps -> algorithms



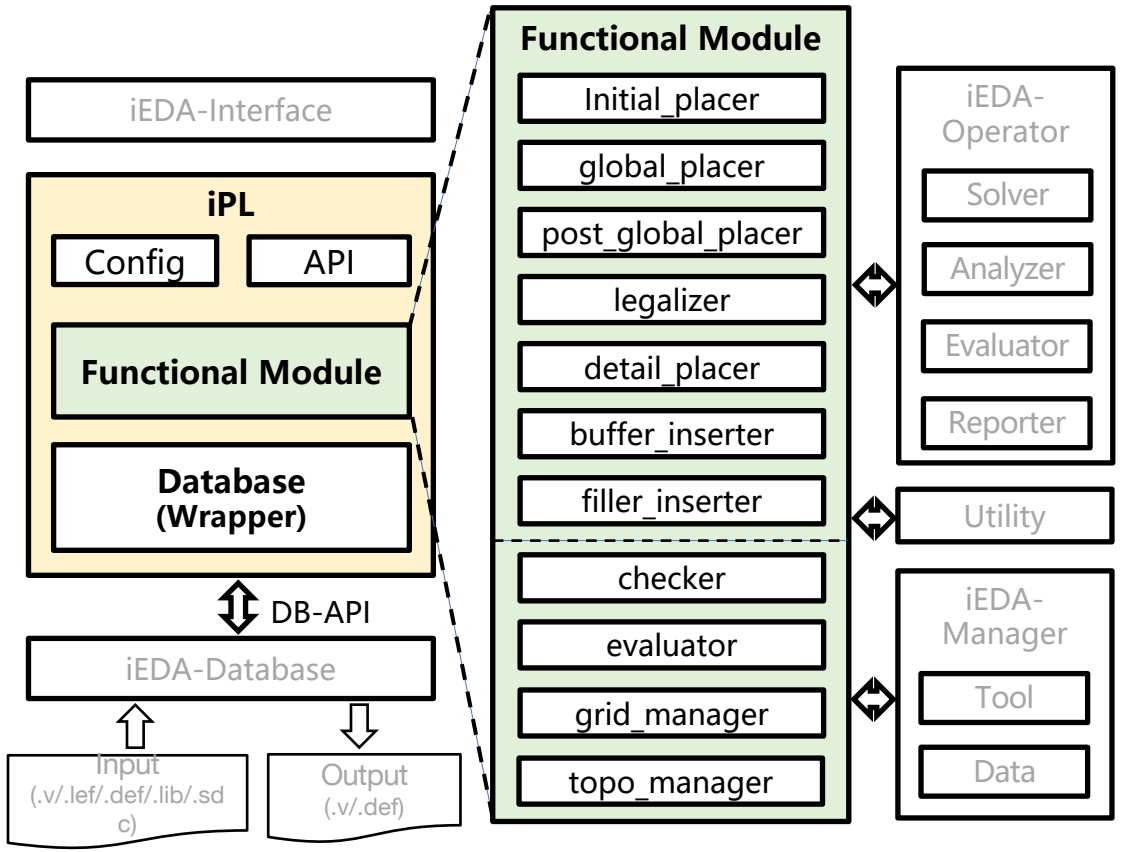
EDA Integration

- Firstly, each tool is designed as a hierarchical set of subtools, steps, and algorithms.
- Secondly, multiple algorithms are supported for each key technology



EDA Tool Software Structure

- A decoupled EDA tool structure:
  - To reduce development costs, iPD is based on the open-source EDA **infrastructure** "**iEDA**";
  - **Data and function** are separated;
  - EDA tool is a hierarchical **algorithm set**, with a plug-and-play mode;
  - All tools in iPD have the **same structure**.
- iPL (placement tool in iPD)
  - iPL utilizes iEDA's **database, operator, manager, and interface** to organize data and algorithms.
  - iPL mainly includes the iPL-**database** and **functional** modules.
  - Users can configure tool **functions** and **parameter** flows through the **config** files, and obtain outputs by **API**.

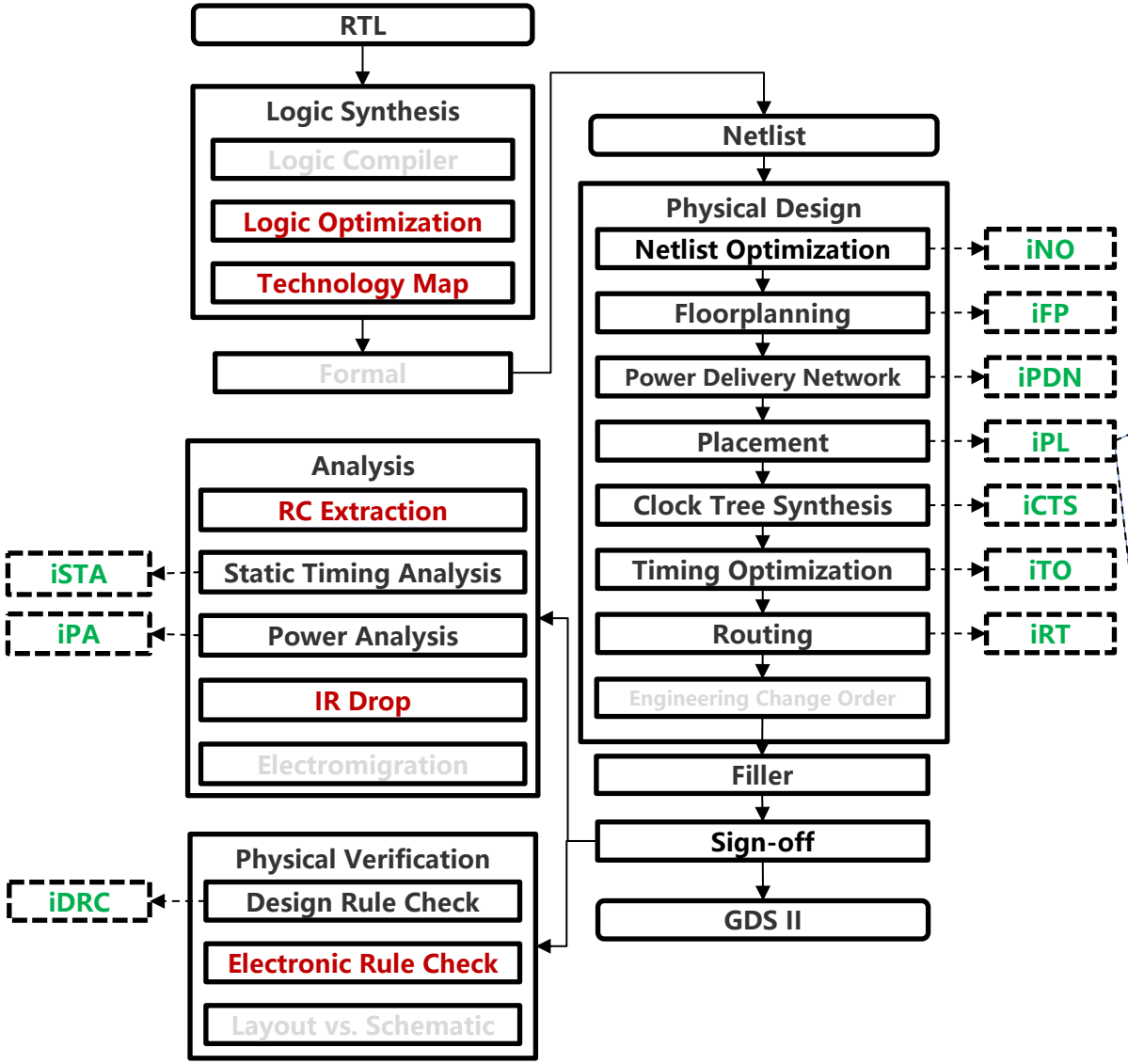


01 Introduction

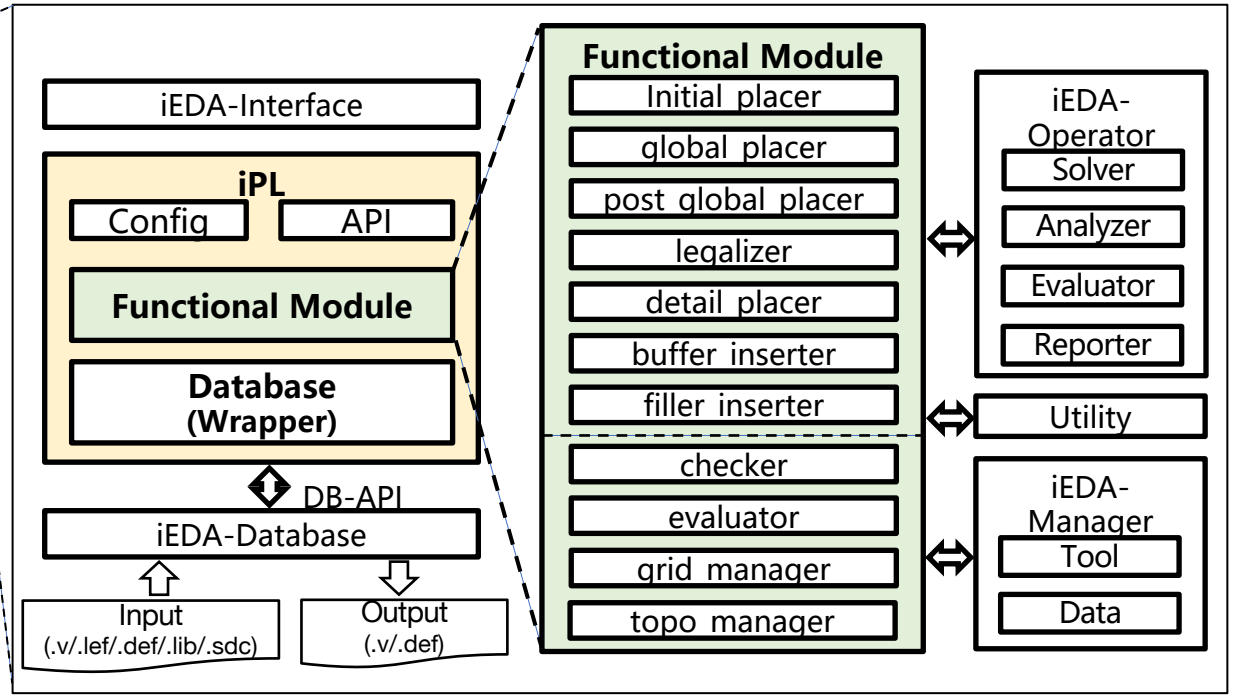
02 iPD Design Mode

03 iPD Toolchain

iPD Toolchain

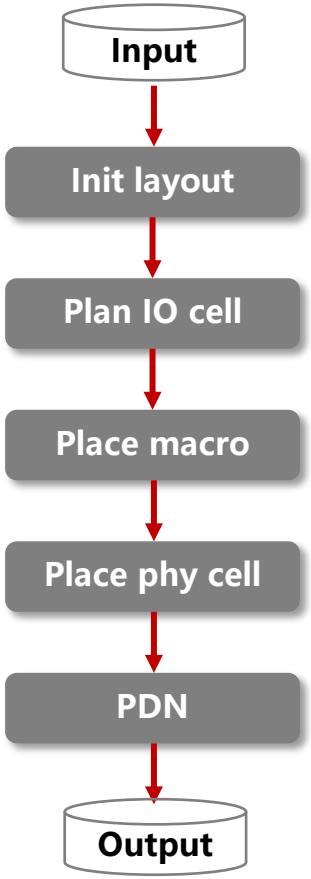


- **Netlist-to-GDS II**
  - **10 tools, and other 5 tools are R&Ding.**
  - **Design, Analysis, Verification**
- **Number of Codes**
  - **>0.3M lines (exclude 3rd party and history)**

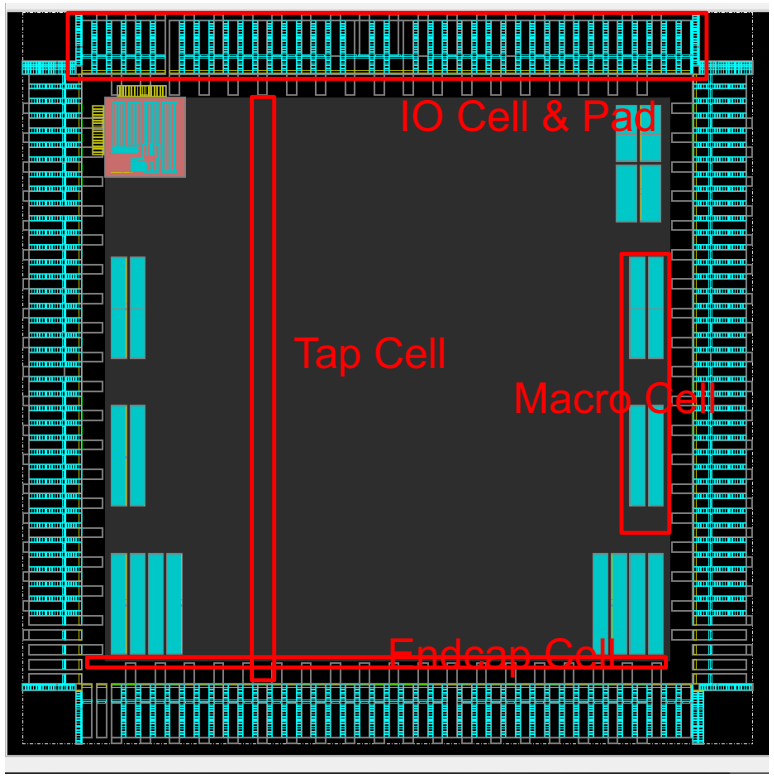


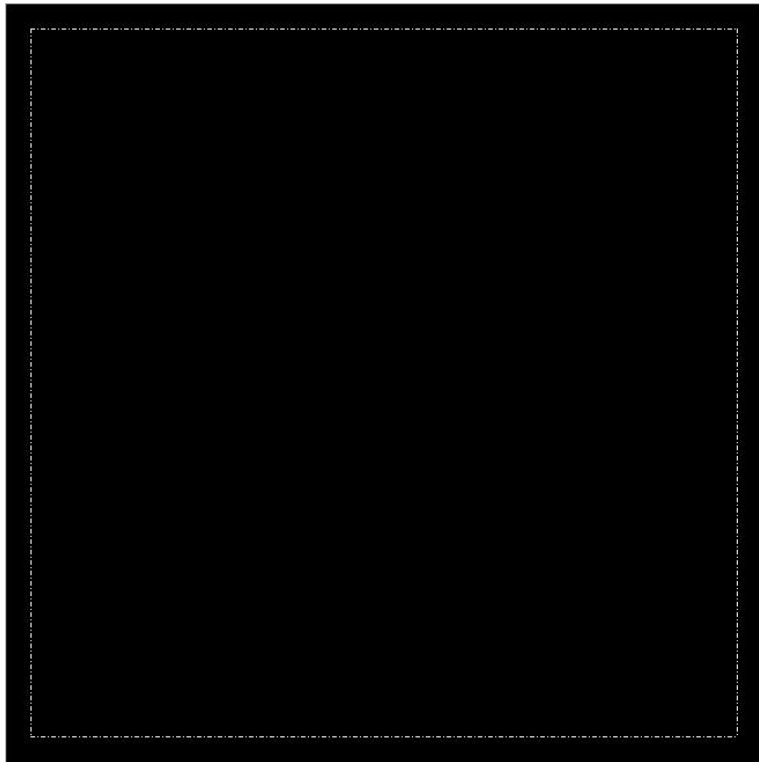
Floorplan (iFP) & Power Delivery Network (iPDN)

Flow



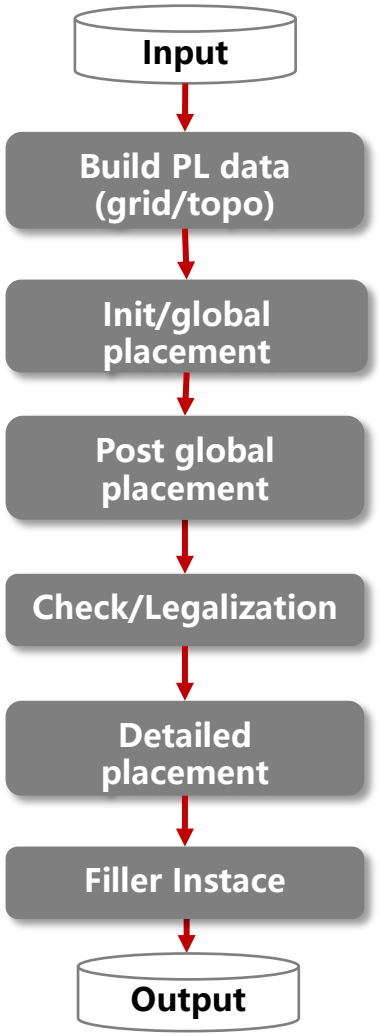
Key Metrics	Data
DIE Area	1.5 × 1.5 mm^2
DIE Utili	0.166554
Core Area	1.16 × 1.15 cm^2
Core Utili	0.279541
#IO Pin	110
#Instance	297504
#Net	311869
Pin	**pin（>= 32）= 2893**
PDN	M1、M2、M7、M8、M9、AP

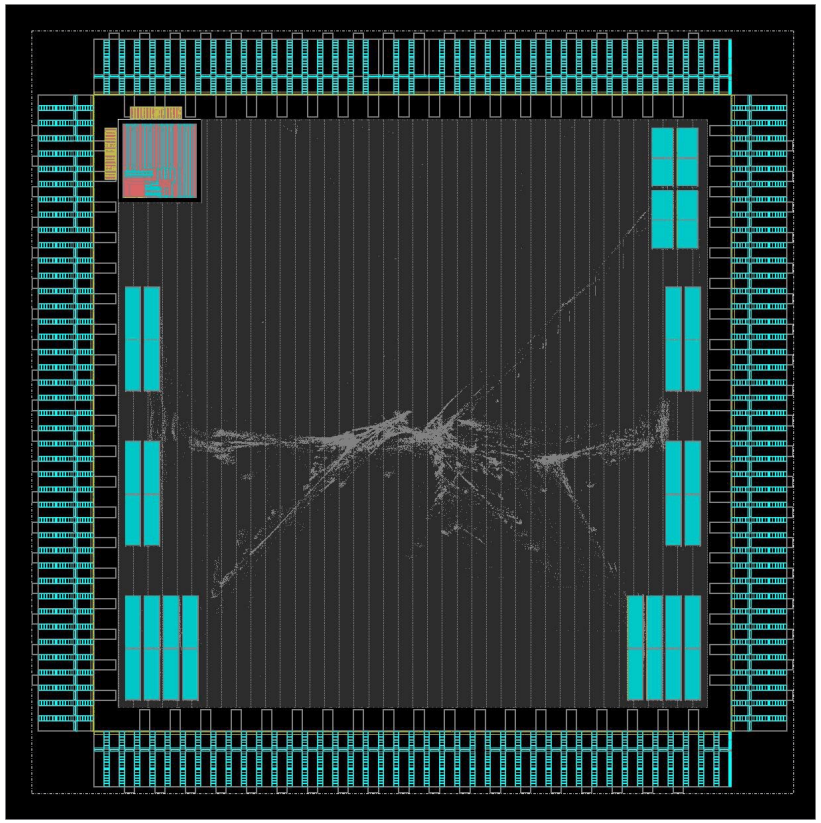




Placement (iPL)

Flow





■ Min Wirelength Model

$$\min_{\boldsymbol{v}} \quad W(\boldsymbol{v})$$
$$s.t. \quad \rho_b(\boldsymbol{v}) \le \rho_0, \qquad \forall b \in B$$

where v is cell location, $W(\boldsymbol{v})$ is wirelength, $\rho_b(\boldsymbol{v})$ is the area density in $b \in B$, ρ_0 is density thredhold.

$\boldsymbol{W(v)}$

$$HPWL_{ex}(\mathbf{v}) = \max_{i,j \in e} |x_i - x_j|$$

$$LSE_{ex} = \gamma\left(\ln\left(\sum_{i \in e}\exp\left(\frac{x_i}{\gamma}\right)\right) + \ln\left(\sum_{i \in e}\exp\left(\frac{-x_i}{\gamma}\right)\right)\right)$$

$\boldsymbol{\rho_b(v)}$

$$D(\boldsymbol{v}) = \frac{1}{2}\sum_{v \in V} D_i(x,y) = \frac{1}{2}\sum_{v \in V} q_i \psi_i(x,y)$$

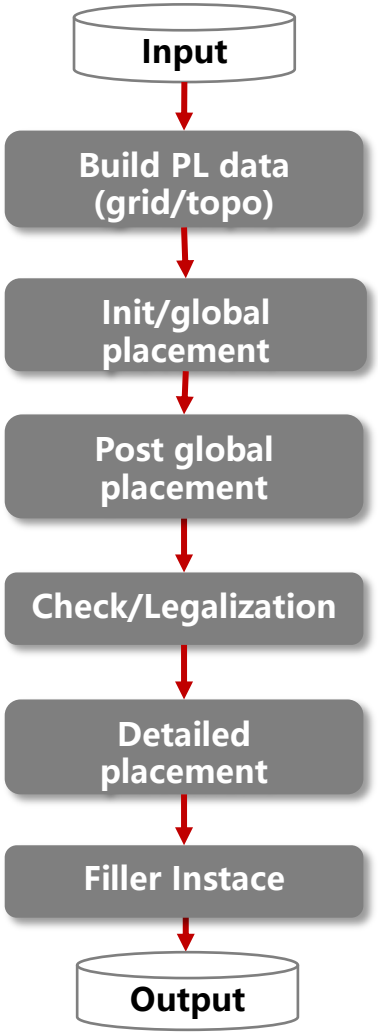
$$\begin{cases} \nabla \cdot \nabla\psi(x,y) = -\rho(x,y), \\ \hat{\boldsymbol{n}} \cdot \psi(x,y) = \mathbf{0}, \qquad (x,y) \in \partial R \\ \iint_R \rho(x,y) = \iint_R \psi(x,y) = 0. \end{cases}$$

$$\min_{\boldsymbol{v}} \quad f(v) = W(\boldsymbol{v}) + \lambda \sum_{\forall b \in B} \boldsymbol{\rho_b}(\boldsymbol{v})$$

- **Nesterov Method or** Conjugate Gradient

Placement (iPL)

Flow



Key parameter config	
Input	iFP.def, iFP.v
output	iPL_result.def, iPL.v
is_max_length_opt	Whether to enable max wirelength optimization
max_length_constraint	set max wirelength constraint
is_timing_aware_mode	Whether to enable timing opt
ignore_net_degree	ignore net whose pin number > k
num_threads	set number of CPU thread
[BUFFER] max_buffer_num	Set the number of using max buffer
[BUFFER] buffer_type	Set available buffer name
[GP-Wirelength] min_wirelength_force_bar	Control wirelength range
[GP-Density] target_density	Set target density
[GP-Density] bin_cnt_x	Set the number of horizontal Bin
[GP-Density] bin_cnt_y	Set the number of vertical Bin
[LG] global_right_padding	Set instance spacing (/site)
[DP] global_right_padding	Set instance spacing (/site)
[Filler] min_filler_width	Set min width of filler (/site)

Basic Summary

summary_report.txt

scripts > sky130 > result > pl > report > summary_report.txt

```
Generate the report at 2023-08-15T15:10:33
+-----------------------+----------+
| Base Info             | Value    |
+-----------------------+----------+
| Design                | gcd      |
| Utilization           | 0.098599 |
| Site Num              | 78 * 542 |
| Instances Count       | 795      |
| - Macro Count         | 0        |
| - StdCell Count       | 795      |
| -- FlipFlop Count     | 34       |
| -- Clock Buffer Count | 0        |
| -- Normal Logic Count | 761      |
| Nets Count            | 675      |
| - Signal Net Count    | 674      |
| - Clock Net Count     | 1        |
| - Reset Net Count     | 0        |
| - Other Net Count     | 0        |
+-----------------------+----------+

+-----------------------------------+-------+
| Violation Info                    | Value |
+-----------------------------------+-------+
| Core Range Violated Count         | 0     |
| Row/Site Alignment Violated Count | 0     |
| Power Alignment Violated Count    | 0     |
| Overlap Violated Count            | 0     |
+-----------------------------------+-------+

+-----------------------------------+----------+
| Wirelength Info                   | Value    |
+-----------------------------------+----------+
| Total HPWL                        | 14402289 |
| Max HPWL                          | 328905   |
| Total STWL                        | 15057480 |
| Max STWL                          | 512025   |
| LongNet HPWL (Exceed 1000000) Count | 0      |
+-----------------------------------+----------+

+------------------+----------+
| Bin Density Info | Value    |
+------------------+----------+
| Peak BinDensity  | 1.000000 |
+------------------+----------+

+------------------+-----------+-----------+-----------+-----------+
| Clock Timing Info | Early WNS | Early TNS | Late WNS  | Late TNS  |
+------------------+-----------+-----------+-----------+-----------+
| core_clock        | 0.000000  | 0.000000  | -0.194720 | -2.818471 |
+------------------+-----------+-----------+-----------+-----------+

+---------------------------+-----------+
| Congestion Info           |           |
+---------------------------+-----------+
| Average Congestion of Edges | 0.537355 |
| Total Overflow            | 53.000000 |
| Maximal Overflow          | 18.000000 |
+---------------------------+-----------+
```

Wirelength
wl_detail_report.txt

Instance density

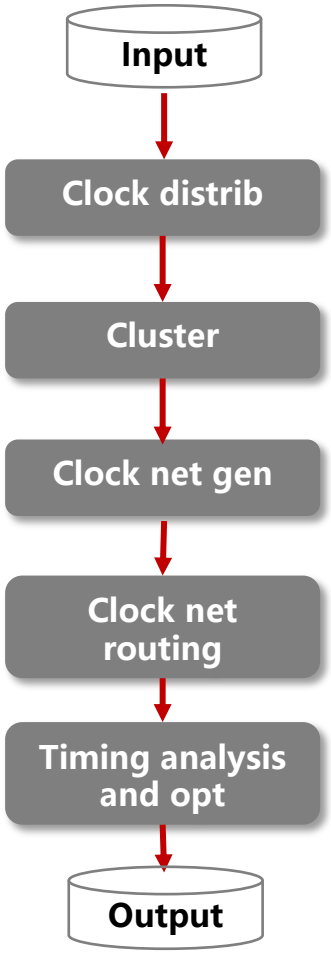
Timing

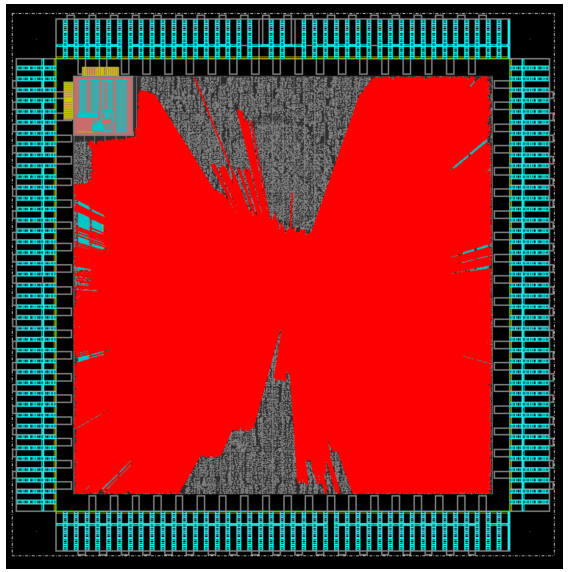
Congestion

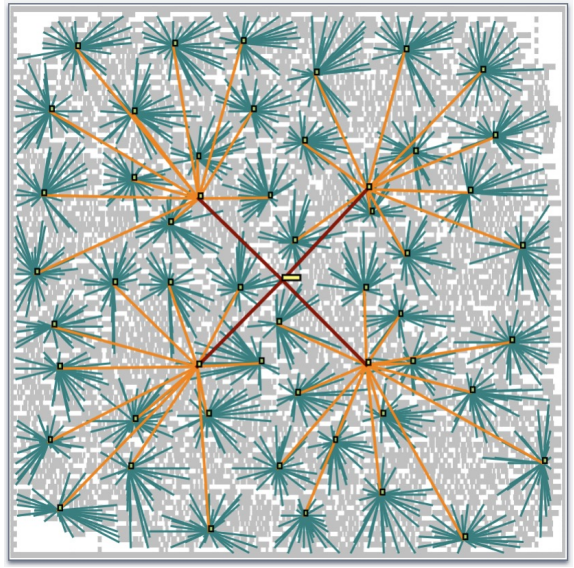
Design rule violation
violation_detail_report.txt

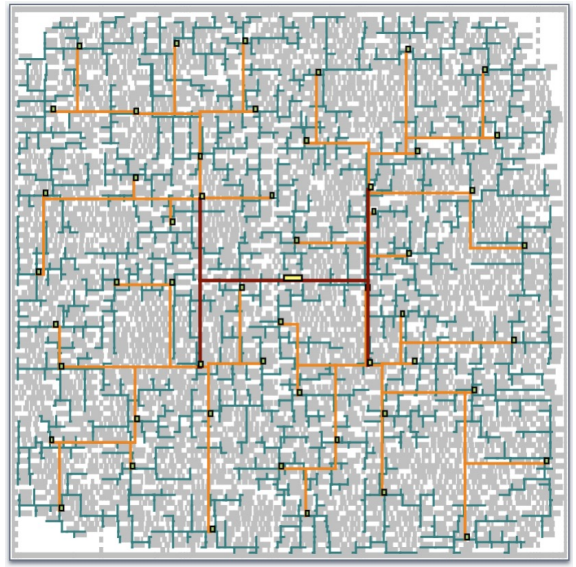
Clock Tree Synthesis (iCTS)

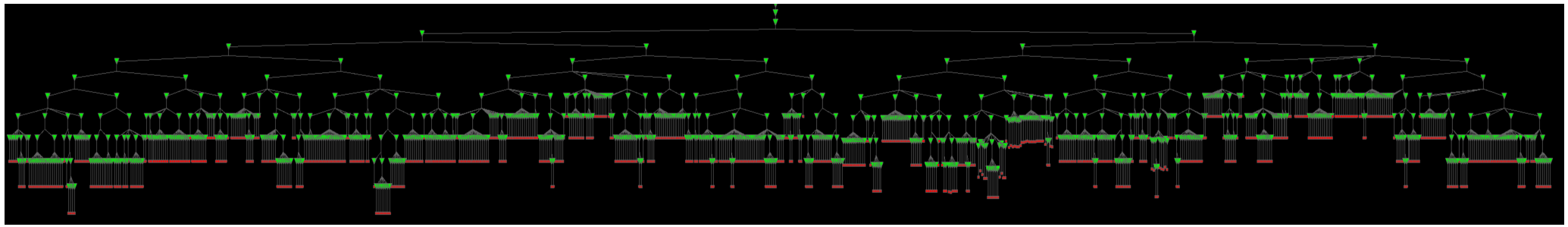
Flow





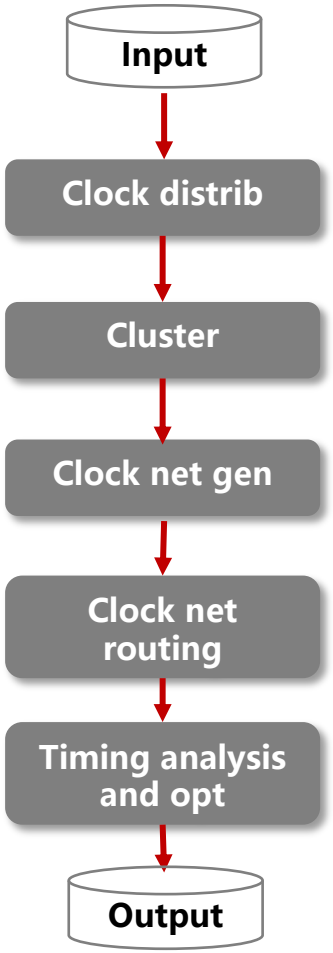






Clock Tree Synthesis (iCTS)

Flow



Timing

- Latency (max delay)
- Skew

Level	Inst Num	Min Skew	Max Skew	Avg Skew	Violation
1	1210	6.62388e-05	0.0145301	0.00105275	0
2	204	0.000406356	0.0278176	0.00972537	0
3	80	0.0042316	0.0411625	0.0190886	0
4	41	0.00690457	0.0566811	0.0323446	0
5	22	0.0261657	0.0760005	0.0524973	0
6	13	0.0261657	0.0799602	0.0623044	0
7	7	0.0261657	0.08	0.0669329	0
8	4	0.0603809	0.08	0.0743834	0
9	2	0.0799208	0.08	0.0799604	0
10	1	0.08	0.08	0.08	0

Level	Inst Num	Min Delay	Max Delay	Avg Delay	Violation
1	1210	0.000237424	0.0432362	0.00143337	None
2	204	0.0518461	0.0983796	0.0688073	None
3	80	0.119261	0.174637	0.145464	None
4	41	0.187633	0.255905	0.219663	None
5	22	0.250207	0.319777	0.294133	None
6	13	0.324988	0.400232	0.365337	None
7	7	0.405067	0.452041	0.435055	None
8	4	0.500763	0.549897	0.522962	None
9	2	0.573994	0.578742	0.576368	None
10	1	0.608399	0.608399	0.608399	None

Power

- Buffering
- Wirelength

Type	Wire Length
Top	161.021
Trunk	2255.200
Leaf	9267.600
Total	11683.821
Max net length	232.360

Type	HP Wire Length
Top	161.021
Trunk	1347.840
Leaf	3871.380
Total	5380.241
Max net length	161.021

Name	Type	Inst Count	Inst Area (um^2)
CKBD12BWP35P140	Buffer	45	96.39
CKBD16BWP35P140	Buffer	8	22.176
CKBD20BWP35P140	Buffer	12	40.824
CKBD24BWP35P140	Buffer	63	254.016
CKBD4BWP35P140	Buffer	1082	954.324
CKBD6BWP35P140	Buffer	1129	1280.29
CKBD8BWP35P140	Buffer	81	122.472

Violation

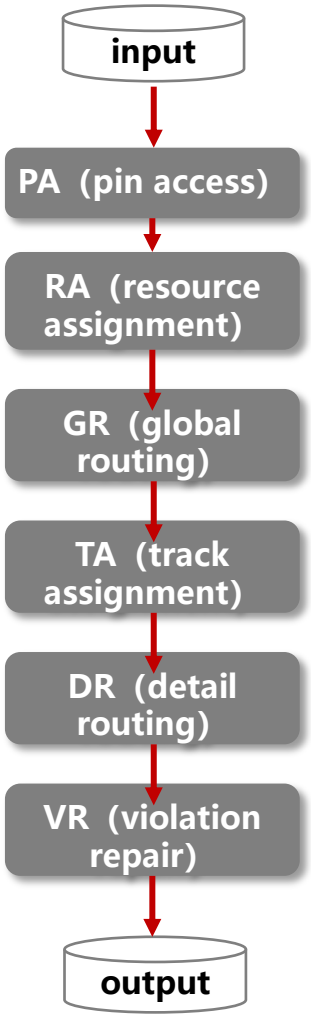
- Fanout
- Capacitance
- Slew (transition)

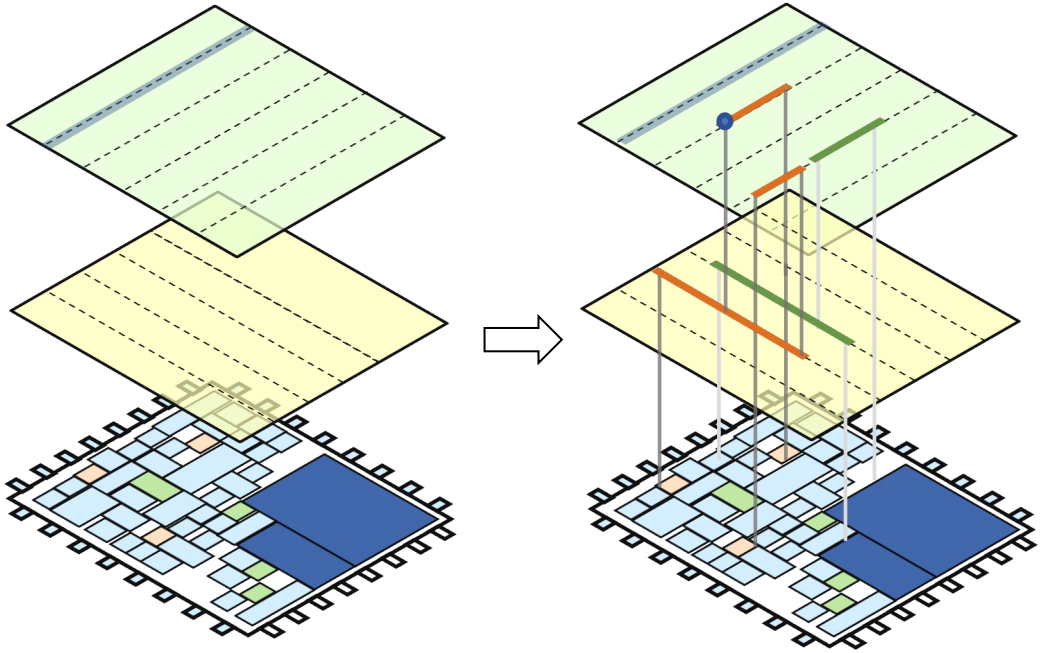
Level	Inst Num	Min Slew	Max Slew	Avg Slew	Violation
1	1210	0.0355823	0.0881141	0.0564704	970
2	204	0.0342527	0.0938317	0.0559007	134
3	80	0.0148774	0.103097	0.0581444	45
4	41	0.00736284	0.102664	0.0516092	20
5	22	0.0175251	0.103516	0.0535373	9
6	13	0.0116574	0.0884235	0.0402797	4
7	7	0.00706415	0.101609	0.0506611	3
8	4	0.015983	0.0220045	0.0188449	0
9	2	0.0259563	0.0286678	0.027312	0
10	1	0	2.22507e-308	0	0

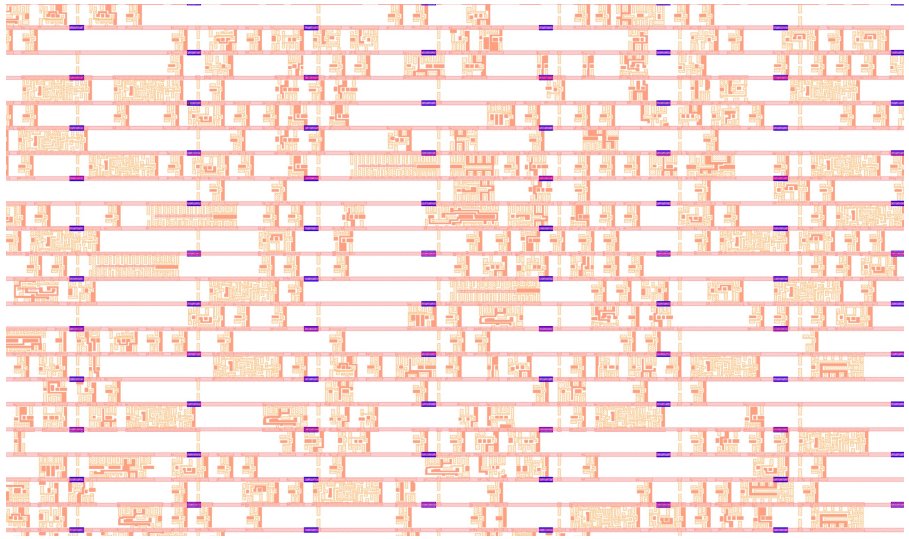
Net / InstPin	MaxTranTime	TranTime	TranSlack	CellPort	Remark
sdram_clk_o					
sdram_clk_o_15397_buf:I	0.800r/0.800f	1.583r/1.494f	-0.783r/-0.694f	CKBD24BWP35P140/I	R
sdram_clk_o					
u0_soc_top/u0_sdram_axi/u_core/U300:ZN	0.800r/0.800f	1.537r/1.446f	-0.737r/-0.646f	INVD1BWP40P140LVT/ZN	R
osc_25m_out_pad					
u0_clk:XOUT	5.000r/5.000f	5.704r/9.550f	-0.704r/-4.550f	PDXOEDG_V_G/XOUT	R
osc_100m_out_pad					
u1_clk:XOUT	5.000r/5.000f	5.704r/9.550f	-0.704r/-4.550f	PDXOEDG_V_G/XOUT	R
clk_hs_peri					
clk_hs_peri_11489_buf:I	0.800r/0.800f	0.850r/0.880f	-0.050r/-0.080f	CKBD24BWP35P140/I	R
u0_rcg/u0_pll_clk					
u0_rcg/u1_lvt_ckmux2hdv4:I1	0.267r/0.267f	0.189r/0.188f	0.078r/0.078f	CKMUX2D4BWP40P140LVT/I1	
u0_rcg/u0_pll_clk					
u0_rcg/u0_pll:FOUTPOSTDIV	0.267r/0.267f	0.000r/0.000f	0.267r/0.267f	PLLTS28HPMLAINT/FOUTPOSTDIV	
clk_core					
clk_core_1724_buf:I	0.800r/0.800f	0.522r/0.533f	0.278r/0.267f	CKBD4BWP35P140/I	
clk_hs_peri					
u0_soc_top/u0_sdram_axi/u_core/U300:I	0.800r/0.800f	0.519r/0.568f	0.281r/0.232f	INVD1BWP40P140LVT/I	
u0_soc_top/n495					
fanout_buf_40:I	0.437r/0.437f	0.098r/0.056f	0.339r/0.381f	BUFFD8BWP30P140LVT/I	

Routing (iRT)

Flow



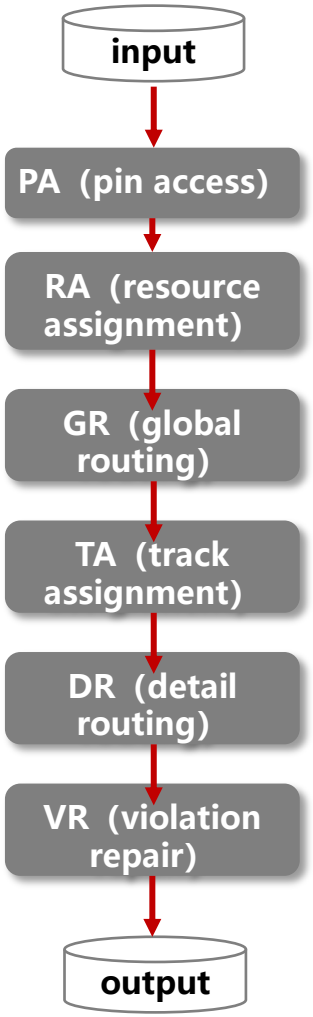


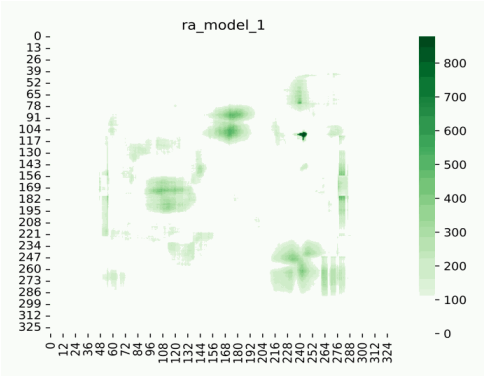


- **Optimization metrics:** wirelength, timing, congestion, DRC
- **Optimization operations:** Global routing: Track allocation: Detailed routing
- **Routing algorithms:** Pattern routing, A* routing, Steiner tree, Non-linear programming, Integer programming

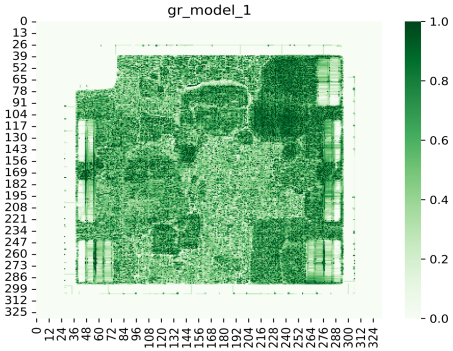
Routing (iRT)

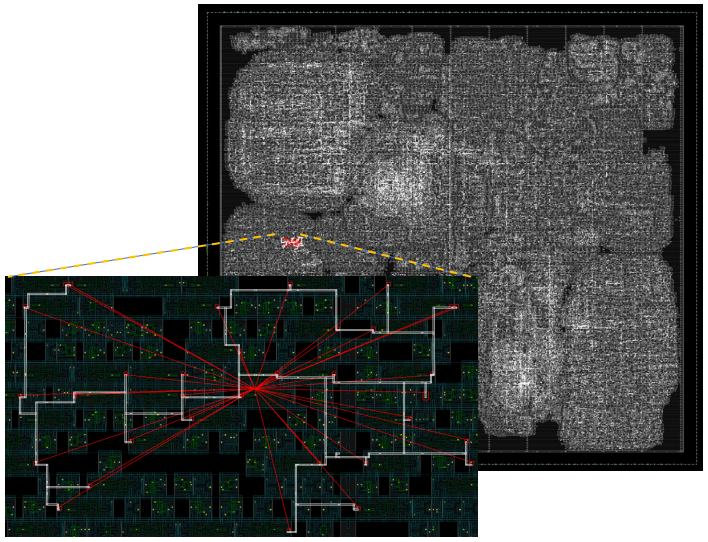
Flow



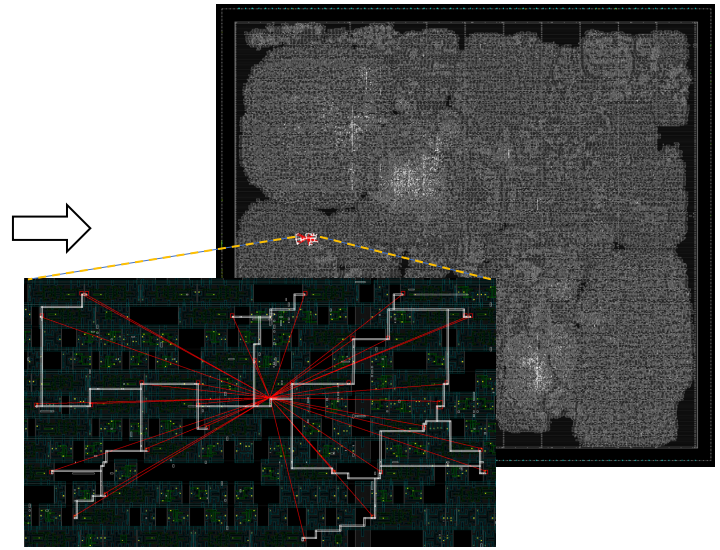


Layout resource/congestion





first iteration routing result



final routing result

Access Type	Pin Number
Track Grid	876856(75.2479%)
On Track	259825(22.297%)
On Shape	28608(2.45501%)
Total	1165289

Routing Layer	Port Number	Access Point Number
M1	806086(68.3279%)	799044(68.5705%)
M2	366214(31.0422%)	362248(31.0865%)
M3	7073(0.599543%)	3997(0.343005%)
M4	358(0.0303459%)	0(0%)
M5	0(0%)	0(0%)
M6	0(0%)	0(0%)
M7	0(0%)	0(0%)
M8	0(0%)	0(0%)
M9	0(0%)	0(0%)
AP	0(0%)	0(0%)
Total	1179731	1165289

Pin Access

Routing Layer	Wire Length / um
M1	9774(0.117785%)
M2	846292(10.1985%)
M3	1.98405e+06(23.9095%)
M4	1.78748e+06(21.5406%)
M5	1.29642e+06(15.6229%)
M6	1.41202e+06(17.016%)
M7	960890(11.5795%)
M8	539.92(0.00650648%)
M9	720(0.00867659%)
AP	0(0%)
Total	8.29819e+06

Cut Layer	Via Number
CO	0(0%)
VIA1	595417(30.6475%)
VIA2	682833(35.147%)
VIA3	400386(20.6088%)
VIA4	135600(6.97965%)
VIA5	89437(4.60353%)
VIA6	38709(1.99244%)
VIA7	262(0.0134857%)
VIA8	148(0.0076179%)
RV	0(0%)
Total	1942792

Resource Overflow	GCell Number
[0,0.1)	921387(83.1%)
[0.1,0.2)	57544(5.19%)
[0.2,0.3)	51492(4.64%)
[0.3,0.4)	40084(3.61%)
[0.4,0.5)	21944(1.98%)
[0.5,0.6)	10780(0.972%)
[0.6,0.7)	4140(0.373%)
[0.7,0.8)	1223(0.11%)
[0.8,0.9)	222(0.02%)
[0.9,1]	74(0.00667%)
Total	1108890

Access Overflow	GCell Number
[0,0.1)	1.78338e+06(80.4%)
[0.1,0.2)	108739(4.9%)
[0.2,0.3)	79939(3.6%)
[0.3,0.4)	90020(4.06%)
[0.4,0.5)	56112(2.53%)
[0.5,0.6)	36741(1.66%)
[0.6,0.7)	30046(1.35%)
[0.7,0.8)	12155(0.548%)
[0.8,0.9)	8771(0.395%)
[0.9,1]	11881(0.536%)
Total	2217780

Wirelength and via

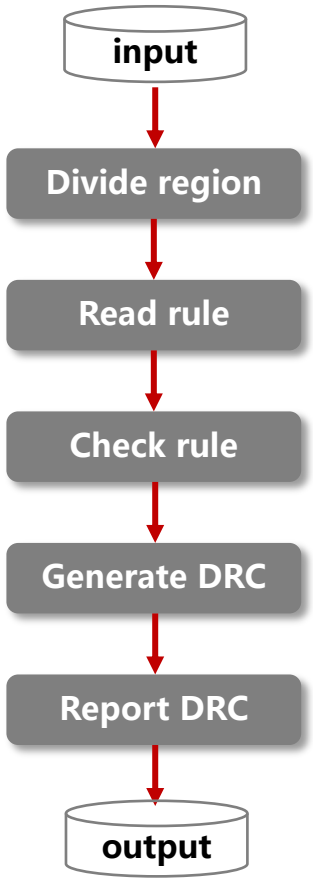
Drc Summary

DRC Type	Number
Cut Different Layer Spacing	433141
Cut EOL Spacing	197803
Cut Enclosure	152168
Cut EnclosureEdge	0
Cut Spacing	358281
Metal Corner Filling Spacing	10443
Metal EOL Spacing	869415
Metal JogToJog Spacing	0
Metal Notch Spacing	733497
Metal Parallel Run Length Spacing	864355
Metal Short	1745445
MinHole	1260
MinStep	670823
Minimal Area	1248072

Design rule check

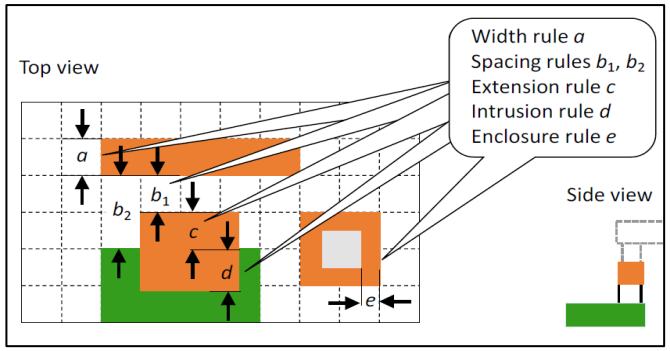
Design Rule Check (iDRC)

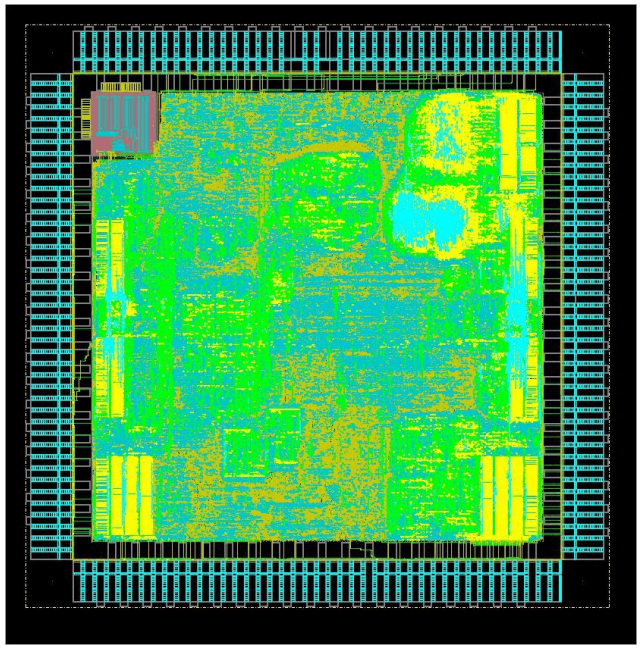
Flow

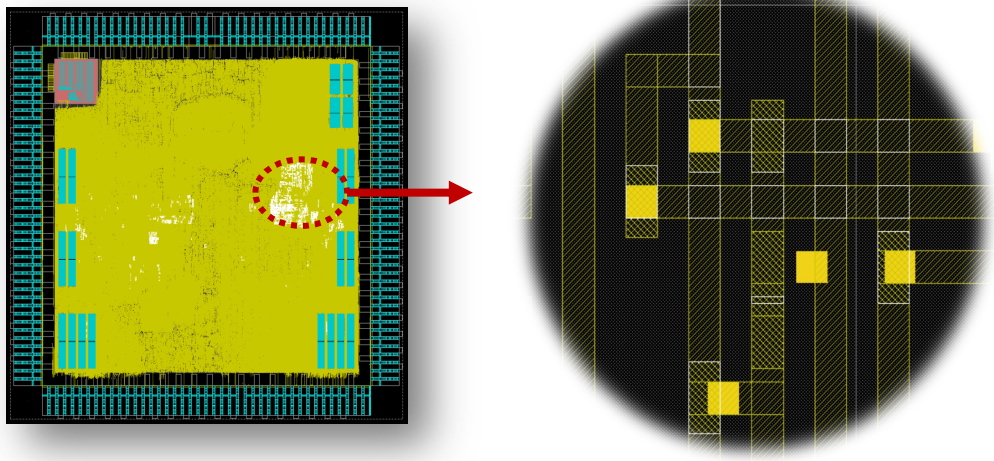


Support DRC Rules:

- Cut Different Layer Spacing
- Cut EOL Spacing
- Cut Enclosure
- Cut Enclosure Edge
- Cut Spacing
- Metal Corner Filling Spacing
- Metal EOL Spacing
- Metal JogToJog Spacing
- Metal Notch Spacing
- Metal Parallel Run Length Spacing
- Metal Short
- MinHole
- MinStep
- Minimal Area



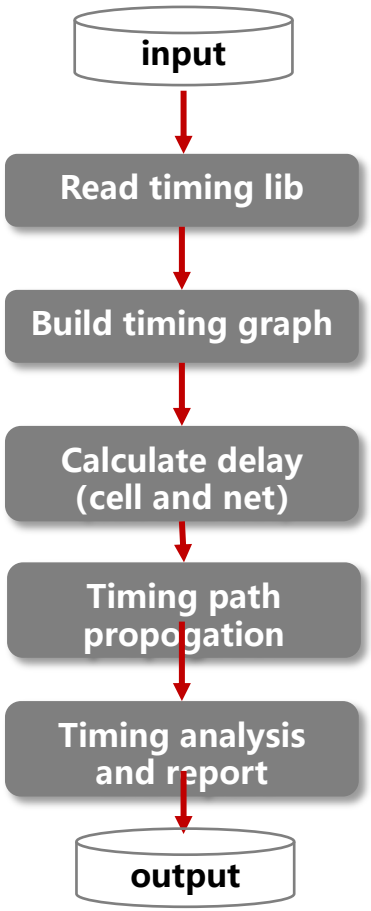


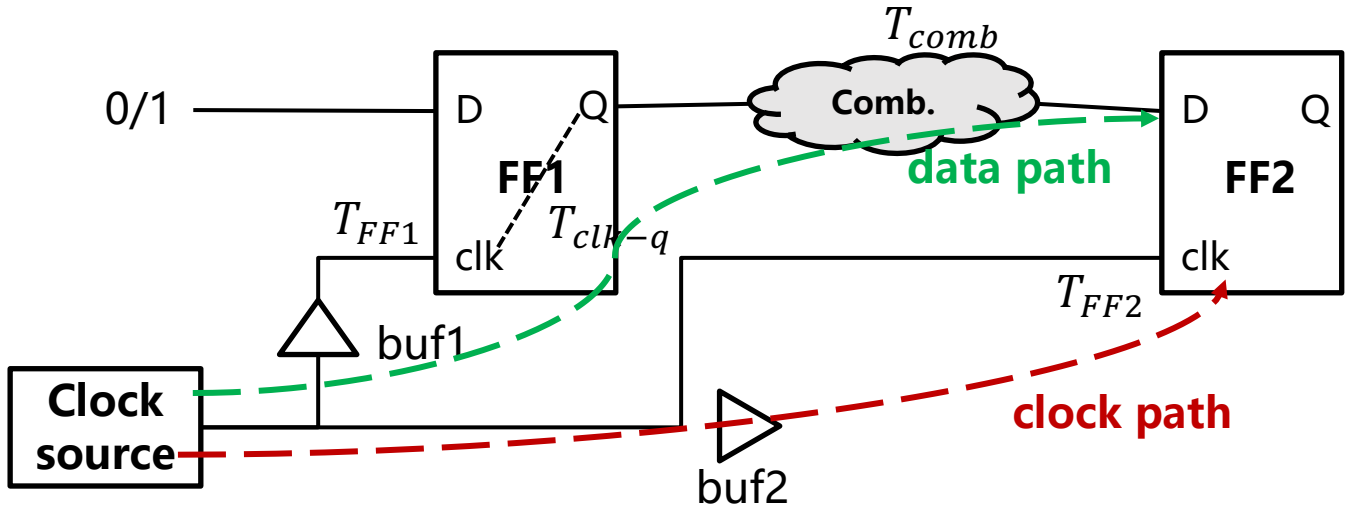


DRC Visulization

Static Timing Analysis (iSTA)

FLow



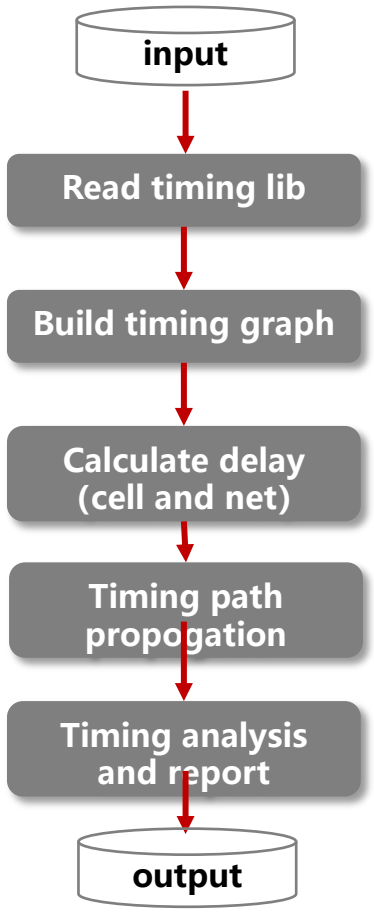


$$T_{FF1} + T_{clk-q} + T_{comb} + T_{setup} - T_{FF2} - T = T^{late}_{slack} \geq 0$$ **Setup Constraint**

$$T_{FF1} + T_{clk-q} + T_{comb} - T_{hold} - T_{FF2} = T^{early}_{slack} \geq 0$$ **Hold Constraint**

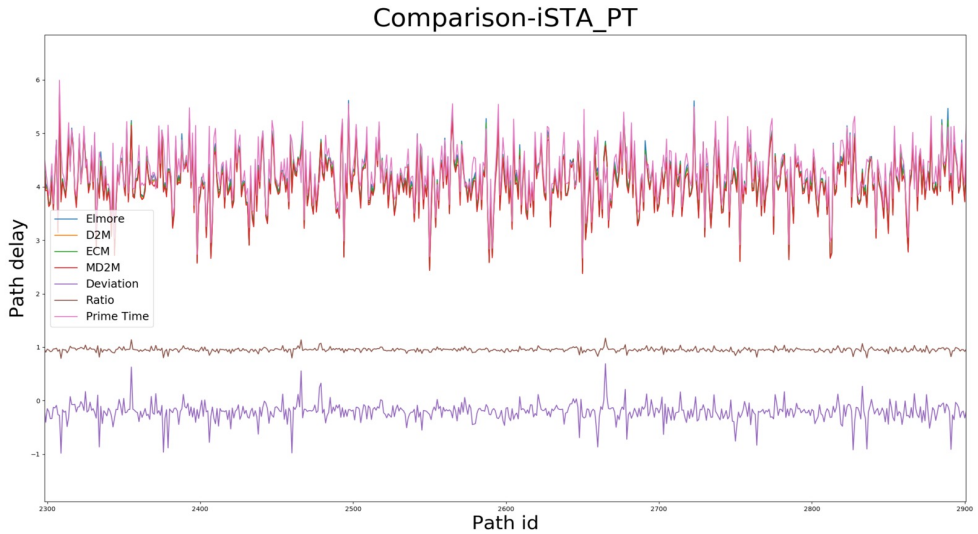
Static Timing Analysis (iSTA)

FLow



Feature
Support hierarchy netlist and def
Basic setup/hold analysis
Support NLDM/Elmore
Support CCS model
Support high-level net delay model
Support sdf mark
OCV
AOCV
POCV
Consider IRDrop analysis on multi-voltage domain
Hierarchy analysis
Crosstalk analysis
clock gate analysis
Latch analysis

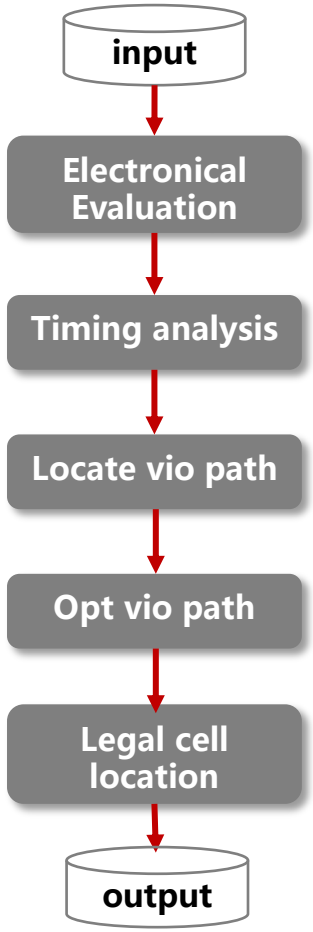
Point	Fanout	Capacitance	Resistance	Transition	Delta Delay	Derate	Incr	Path
u1_clk:XC (PDXOEDG_V_G)		0.002	0.000	0.000		1.000	0.000	0.000r
sys_clk_100m (clock net)	1				0.000			
u1_clk_xc_donottouch:I (CKBD12BWP40P140LVT)		0.002	0.000	0.000		1.000	0.000	0.000r
u1_clk_xc_donottouch:Z (CKBD12BWP40P140LVT)		0.002	0.000	0.006		0.885	0.011	0.011r
sys_clk_100m_buf (clock net)	2				0.000			
u0_rcg/u1_lvt_ckmux2hdv4:I0 (CKMUX2D4BWP40P140LVT)		0.001	0.000	0.006		1.000	0.000	0.011r
u0_rcg/u1_lvt_ckmux2hdv4:Z (CKMUX2D4BWP40P140LVT)		0.006	0.000	0.018		0.885	0.032	0.043r
u0_rcg/mux_core_clk (clock net)	5				0.000			
u0_rcg/mux_core_clk_0_buf:I (CKBD4BWP35P140)		0.001	0.000	0.018		1.000	0.000	0.043r
u0_rcg/mux_core_clk_0_buf:Z (CKBD4BWP35P140)		0.008	0.000	0.015		0.885	0.021	0.064r
u0_rcg/mux_core_clk_0 (clock net)	17				0.000			
u0_rcg/mux_core_clk_div3/gt_en1_reg:CP (DFSNQD1BWP40P140LVT)		0.000	0.000	0.015		1.000	0.000	0.064r
clock CLK_u1_clk_XC (rise edge)							0	0
clock network delay (propagated)							0.064	0.064
u0_rcg/mux_core_clk_div3/gt_en1_reg:CP (DFSNQD1BWP40P140LVT)		0.000	0.000	0.015		1.000	0.000	0.064r
u0_rcg/mux_core_clk_div3/gt_en1_reg:Q (DFSNQD1BWP40P140LVT)		0.001	0.000	0.009		0.820	0.045	0.109r
u0_rcg/mux_core_clk_div3/gt_en1 (net)	1				0.000			
u0_rcg/mux_core_clk_div3/U_GT1:E (CKLNQD4BWP40P140LVT)		0.001	0.000	0.009		1.000	0.000	0.109r
u1_clk:XC (PDXOEDG_V_G)		0.002	0.000	0.000		1.000	0.000	0.000r
sys_clk_100m (clock net)	1				0.000			
u1_clk_xc_donottouch:I (CKBD12BWP40P140LVT)		0.002	0.000	0.000		1.000	0.000	0.000r
u1_clk_xc_donottouch:Z (CKBD12BWP40P140LVT)		0.002	0.000	0.006		1.039	0.013	0.013r
sys_clk_100m_buf (clock net)	2				0.000			
u0_rcg/u1_lvt_ckmux2hdv4:I0 (CKMUX2D4BWP40P140LVT)		0.001	0.000	0.006		1.000	0.000	0.013r
u0_rcg/u1_lvt_ckmux2hdv4:Z (CKMUX2D4BWP40P140LVT)		0.006	0.000	0.018		1.039	0.038	0.051r
u0_rcg/mux_core_clk (clock net)	5				0.000			
u0_rcg/mux_core_clk_0_buf:I (CKBD4BWP35P140)		0.001	0.000	0.018		1.000	0.000	0.051r
u0_rcg/mux_core_clk_0_buf:Z (CKBD4BWP35P140)		0.008	0.000	0.015		1.039	0.025	0.076r
u0_rcg/mux_core_clk_0 (clock net)	17				NA			
u0_rcg/mux_core_clk_div3/U_GT1:CP (CKLNQD4BWP40P140LVT)		0.001	0.000	0.000		1.000	0.000	0.076r
clock CLK_u1_clk_XC (rise edge)							0	0
clock network delay (propagated)							0.076	0.076
u0_rcg/mux_core_clk_div3/U_GT1:CP (CKLNQD4BWP40P140LVT)								r
library hold time							0.000	0.076
clock reconvergence pessimism						-0.011	0.064	
data require time								0.064
data arrival time								0.109
slack (MET)								0.045



pt/ista ratio	value
mean	1.11
variance	0.00095
median	1.107
maximum	1.5404
minimum	0.9035

Timing Optimization (iTO)

Flow



Key parameter config	
Input	iPL.def, iCTS.def
output	iTO_setup_result.def, iTO_hold_reslut.def
setup_slack_margin	setup slack value
hold_slack_margin	hold slack value
max_buffer_percent	Area ratio of inserted buffer
max_utilization	Core utilization
DRV_insert_buffers	Available buffer for optimizing DRV
setup_insert_buffers	Available buffer for optimizing setup
hold_insert_buffers	Available buffer for optimizing hold
number_passes_allowed_decreasing_slack	The number of times that WNS is allowed continuously decrease when opt setup
rebuffer_max_fanout	For setup, a wire network is not optimized for buffer insertion when its fanout exceeds this value
split_load_min_fanout	For setup, fanout is reduced by inserting a buffer when fanout is greater than this value

DRV report

```
path
Worst Slack: -5.88383
Found 3 slew violations.
Found 11 capacitance violations.
Found 0 fanout violations.
Found 0 long wires.
Before ViolationFix | slew_vio: 3 cap_vio: 11 fanout_vio: 0 length_vio: 0
The 1th check
After ViolationFix | slew_vio: 3 cap_vio: 0 fanout_vio: 0 length_vio: 0
The 2th check
After ViolationFix | slew_vio: 0 cap_vio: 0 fanout_vio: 0 length_vio: 0
DRV_net_3
Inserted 11 buffers in 12 nets.
Resized 0 instances.
```

Setup report

```
Inserted 10 hold buffers.

Worst Hold Path Launch : u0_soc_top/u0_sdram_axi/u_core/sample_data0_q_reg_8_:CP
Worst Hold Path Capture: u0_soc_top/u0_sdram_axi/u_core/sample_data_q_reg_8_:CP

The 1-th timing check.
    worst hold slack: -1.28225
Unable to repair all hold violations. There are still 16 endpoints with hold violation.
Max utilization reached.
```

- Fix timing design rule violation
  - Max cap/Max slew/Max wirelength/Max fanout
- Fix hold time
- Fix setup time
- Cell sizing
- Buffer Insertion
- Load Insertion
- Buffer/load location

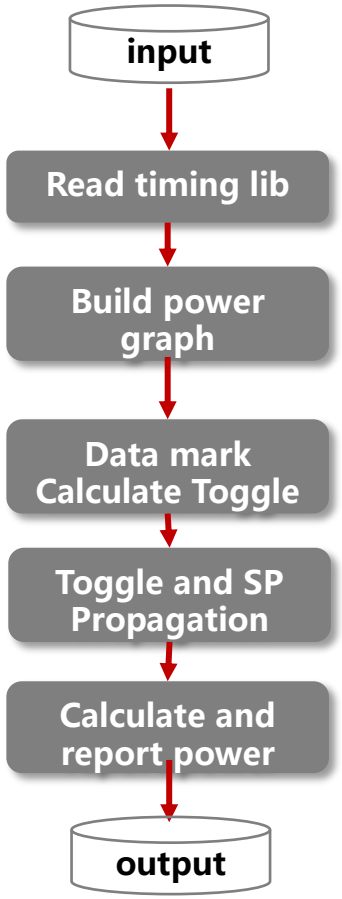
Clock Group	Hold TNS	Hold WNS
CLK_chiplink_tx_clk	0	0
CLK_clk_hs_peri	-185.768	-1.27825
CLK_div2_core	-2606.7	-0.106129
CLK_div2_hs_peri	-216.759	-0.028571
CLK_div3_hs_peri	-72.5124	-0.028571
CLK_div4_core	-1304.1	-0.106129
CLK_div4_hs_peri	-185.768	-1.27825
CLK_div4_peri	-231.408	-0.042802
CLK_sdram_clk_o	0	0
CLK_spi_clk	0	0
CLK_spi_clk_out	0	0
CLK_u0_chiplink_rx_clk_pad_PAD	-89.8732	-0.028408
CLK_u0_clk_XC	-2987.42	-0.106129
CLK_u0_pll_FOUTPOSTDIV	-8546.64	-0.106129
CLK_u1_clk_XC	-2755.16	-0.106129

Clock Group	Hold TNS	Hold WNS
CLK_chiplink_tx_clk	0	0
CLK_clk_hs_peri	0	0
CLK_div2_core	0	0
CLK_div2_hs_peri	0	0
CLK_div3_hs_peri	0	0
CLK_div4_core	0	0
CLK_div4_hs_peri	0	0
CLK_div4_peri	0	0
CLK_sdram_clk_o	0	0
CLK_spi_clk	0	0
CLK_spi_clk_out	0	0
CLK_u0_chiplink_rx_clk_pad_PAD	0	0
CLK_u0_clk_XC	0	0
CLK_u0_pll_FOUTPOSTDIV	0	0
CLK_u1_clk_XC	0	0

Hold report

Power Analysis (iPA)

Flow



API	Description
buildGraph	Build iPW graph data structure
readVCD	Parse the VCD file
buildSeqGraph	Build timing subgraph
checkPipelineLoop	Detect PipeLine loop
levelizeSeqGraph	Grade timing subgraph
propagateToggleSP	Propagate Toggle and SP data on the graph
calcLeakagePower	Calculate the leakage power
calcInternalPower	Calculate internal power
calcSwitchPower	Calculate switching power
analyzeGroupPower	Analyze power data
reportPower	Output power report

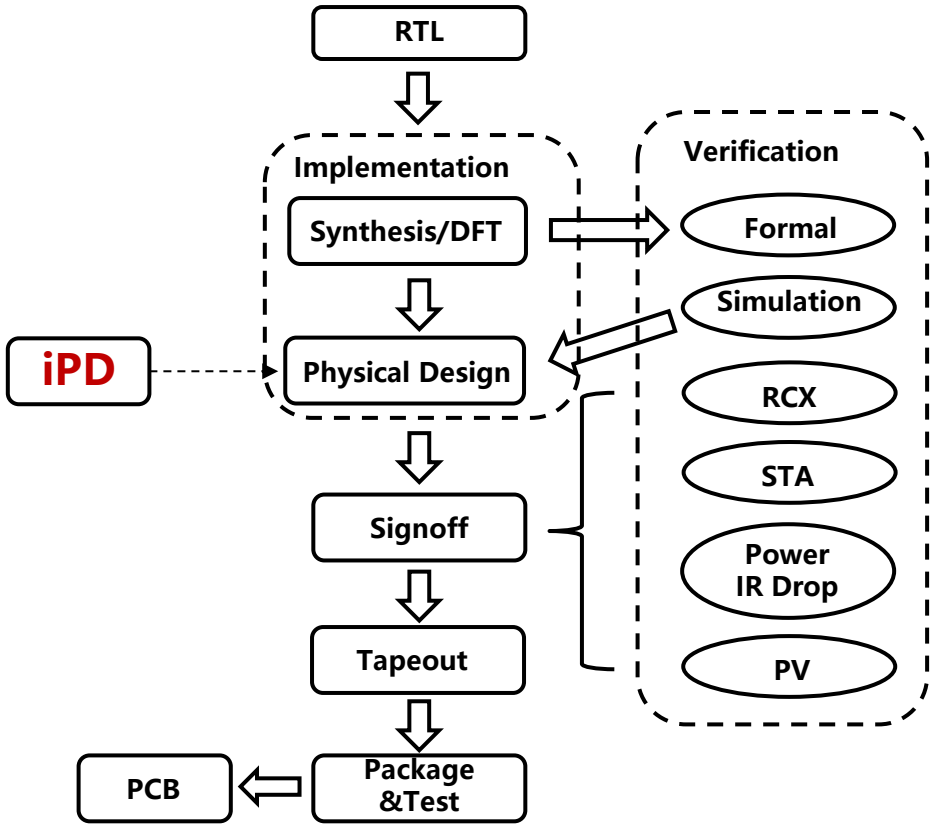
cases	iPA total power	Innovus total power	deviation
aes_cipher_top	22.22mW	23.74mW	6.4%
gcd	0.38mW	0.37mW	3.6%
uart	0.51mW	0.49mW	3.9%

```
Generate the report at 2023-05-06T09:54:06
Report : Averaged Power
+--------------+---------------+-------------+--------------+------------+-----------+
| Power Group  | Internal Power | Switch Power | Leakage Power | Total Power | (%)       |
+--------------+---------------+-------------+--------------+------------+-----------+
| combinational | 1.064e-07     | 5.063e-09    | 3.079e-08    | 1.422e-07  | (27.595%) |
| sequential    | 2.862e-07     | 7.337e-09    | 7.963e-08    | 3.732e-07  | (72.405%) |
+--------------+---------------+-------------+--------------+------------+-----------+
Net Switch Power  ==  1.240e-08 (2.406%)
Cell Internal Power  ==  3.926e-07 (76.173%)
Cell Leakage Power  ==  1.104e-07 (21.422%)
Total Power  ==  5.154e-07
```

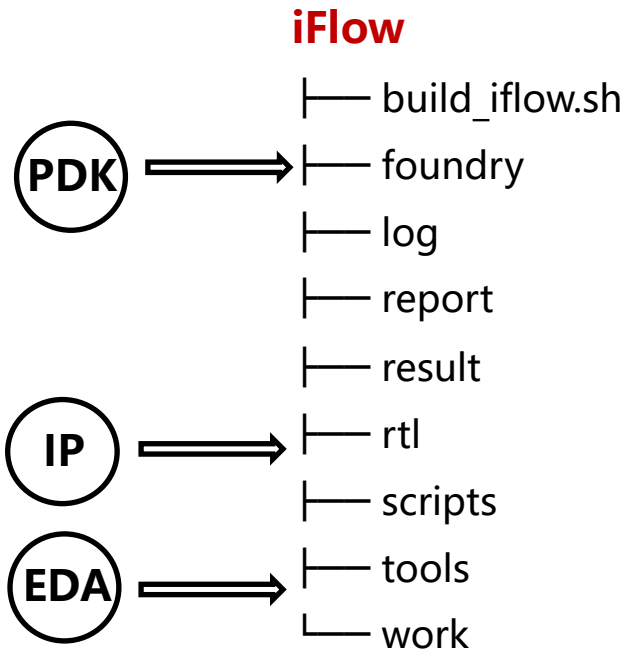
- Evaluate power before / during / after the physical design process
- Average model
- Timing window (coming soon)
- VCD parser
- Report/API

iFlow: A Chip Design Flow

- **iFlow: supporting different EDA tools, PDKs, designs**



Chip design flow

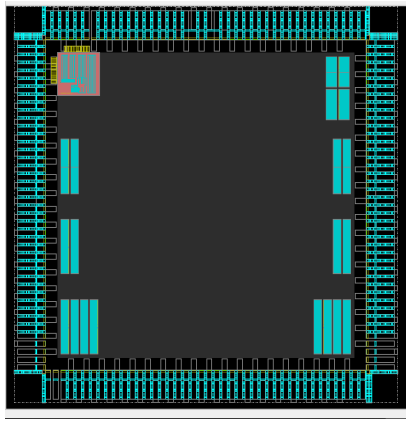


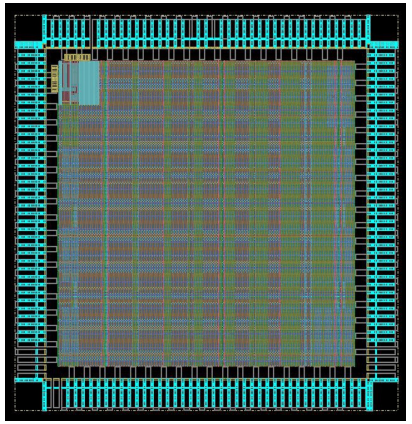
Example Design: ysyx-04-01

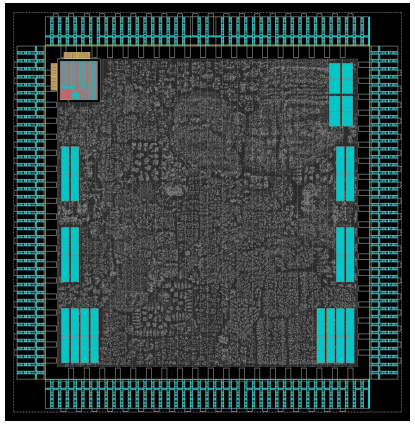
- RTL：ysyx(一生一芯)-04
- PDK：28nm
- Area：1.5mm × 1.5 mm
- Power：dynamic = 317mW，leakage = 29 mW
- Freq.：200MHz
- Scale：>1.5M Gates
- Features：11 pipelines with cache，IP：UART、VGA、PS/2、SPI、SDRAM、 2 PLLs，support Linux

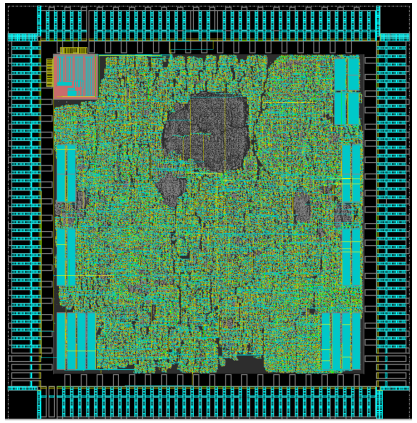
part metrics	iPL (place)	iCTS	iTO	iRT (route)
#inst	1043440	1057291	1057549	1057549
#net	1015532	1029383	1029641	1029641
utilization	0.563929	0.570644	0.570768	0.570768
HPWL	34108823398	35042653984	35044866877	50157263995*
STWL	46195026227	46580611921	46581568292	
frequency	245.245	238.226	241.386	224.254
#DRC	0	0	0	233335

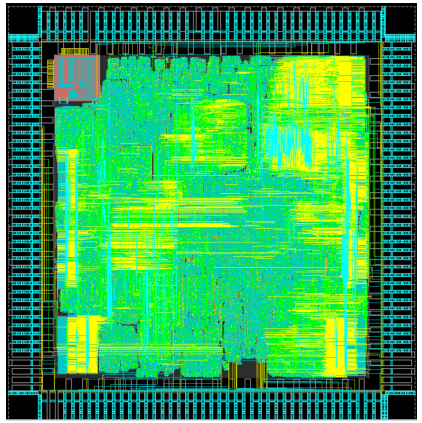
* Total wirelength after routing

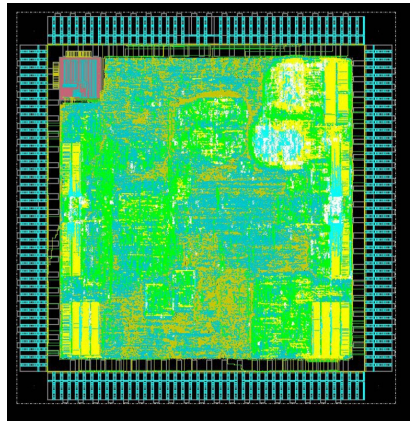

Floorplan


PDN


Placement

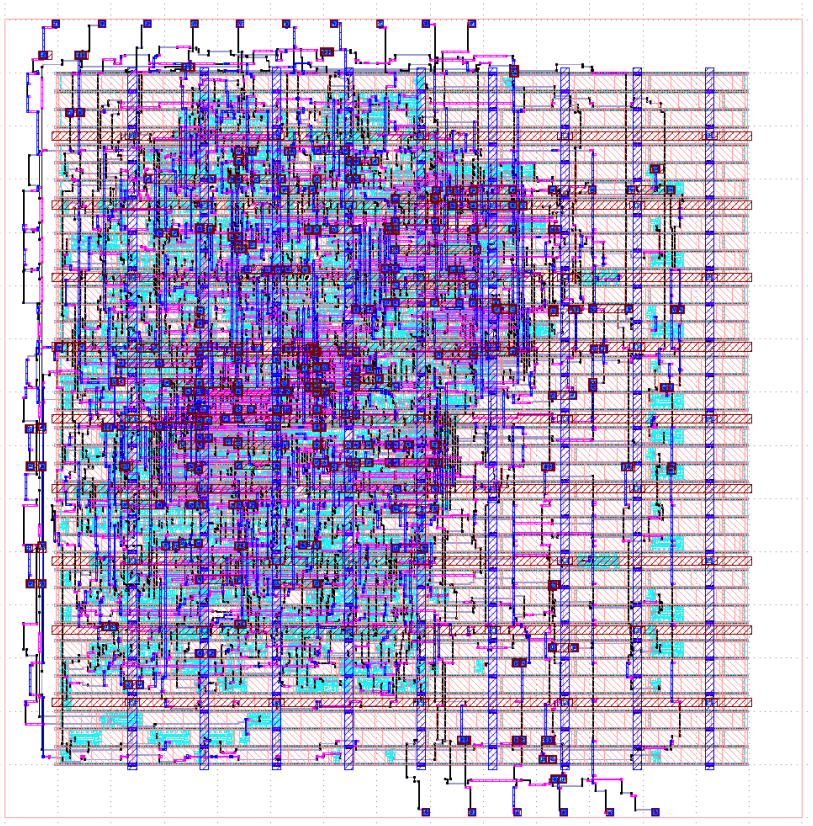

CTS


Routing

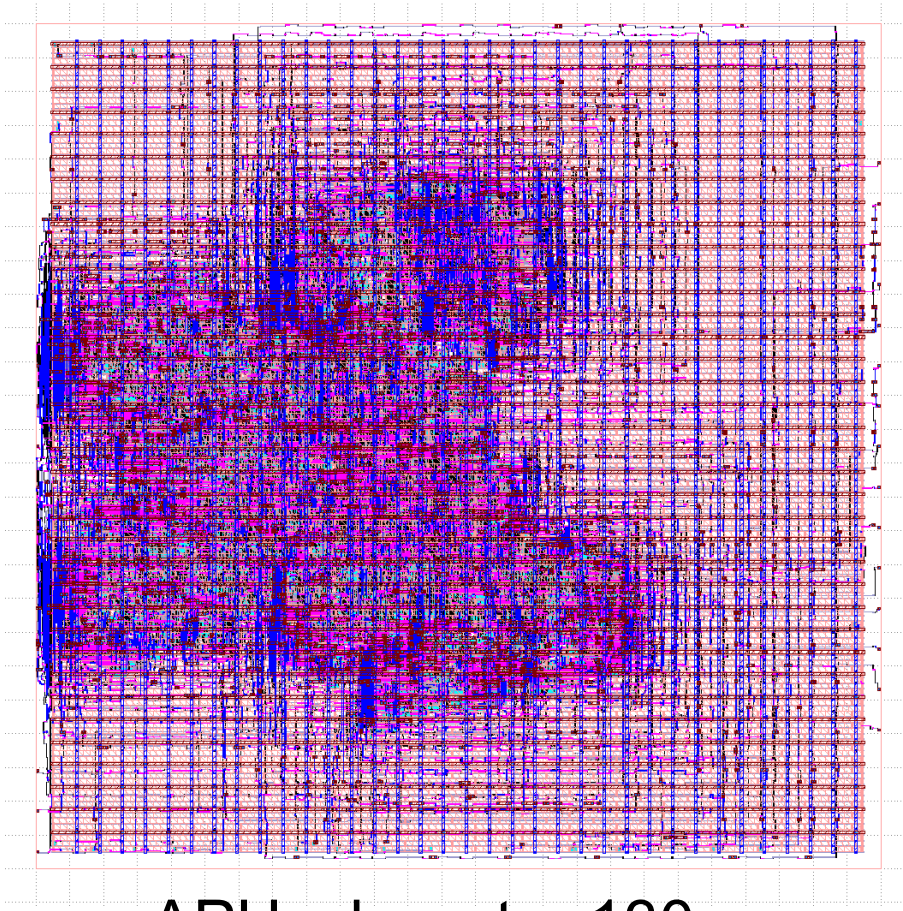

DRC

Example Design: from other users

- gcd & APU



gcd, skywater 130nm
Area：0.15mm × 0.15 mm



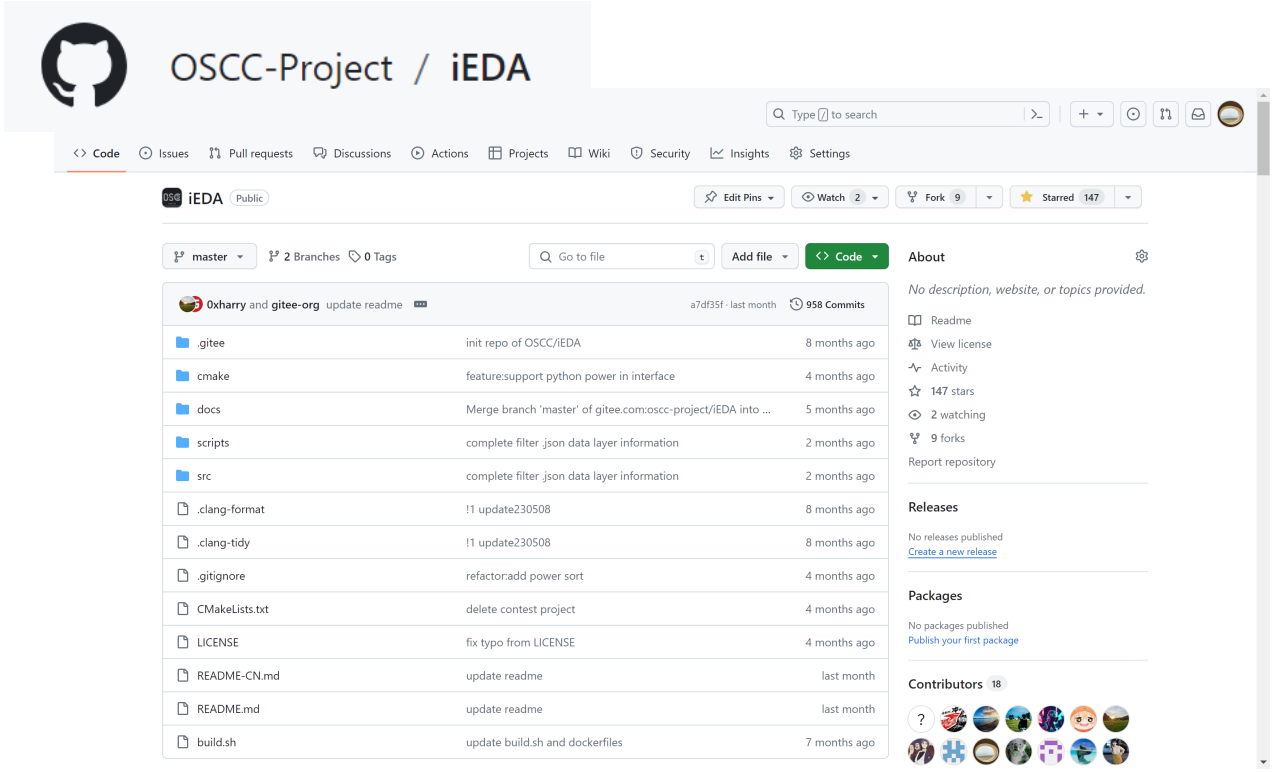
APU, skywater 130nm
Area：0.45mm × 0.45 mm

Conclusions

- **iPD design mode:**
  - Decomposition and integration
  - Unified software structure
- **iPD toolchain: from netlist to GDS EDA tool, include**
  - Floorplan and power deliver network
  - Macro placement and standard cell placement
  - Clock tree synthesis
  - Routing and design rule check
  - Timing analysis and optimization
  - Power analysis

Future Works

- **Upcoming EDA tools:**
  - Technology mapping (iMAP)
  - Parasitic extraction (iRCX)
  - IR drop analysis (iIR)
- **AI model:**
  - Metric prediction
  - Design space exploration
- **Development tool:**
  - Process data visualization



Thanks

Bei Yu
byu@cse.cuhk.edu.hk