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Performance-Driven Analog Layout Automation: Current Status and Future Directions

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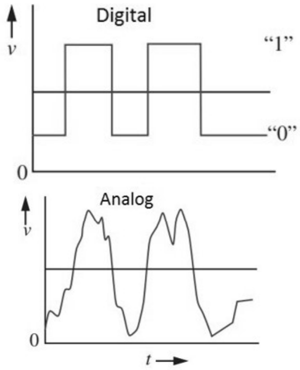
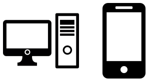
Outline

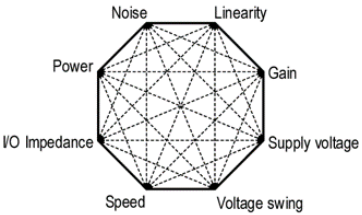
Introduction

Digital vs Analog Circuits



	Data	Reliability	Design
	Boolean	Robust	Automated
	Real	Sensitive	Manual

Analog IC Design & Challenges

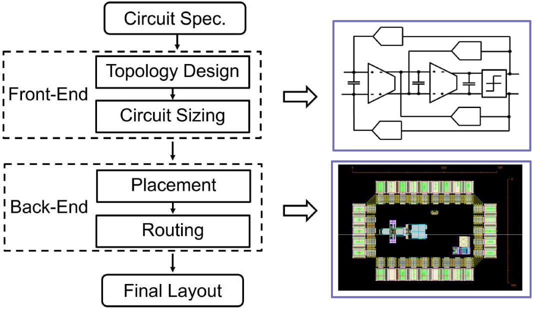


Courtesy [Razavi, Design of Analog IC]

- Heavily manual, iterative process involving multiple steps to achieve performance, power and area closure.
- More challenging with performance closure: complicated circuit performance metrics, sensitive signal integrity and performance trade-offs
- **Open question**: how can we optimize *performance* in automated layout generation?

AMS Design Automation

- Analog IC automation typical flow:



- Today we will focus on the back-end side

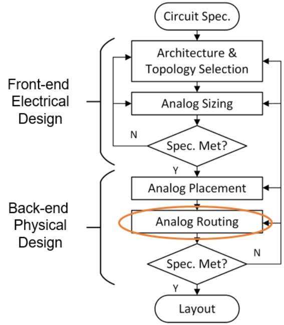
Develop optimization-based PNR algorithms for analog layouts

Pros

- Automatic optimization
- Low human efforts

Cons

- What is the optimization problem?
- How to consider performance?



The design flow of analog circuits.

Related Work

Existing Problems

Analog circuit placement and routing are critical to optimal performance, but obtaining a decent circuit layout requires significant time and expertise:

- Unlike digital circuits, analog circuits are sensitive to layout parasitics and coupling, which can complicate the relationship between performance and layout.
- There lacks a practical way to produce generalized performance models for layout implementation[1].

Let's first take a look on existing attempts to consider performance in PNR

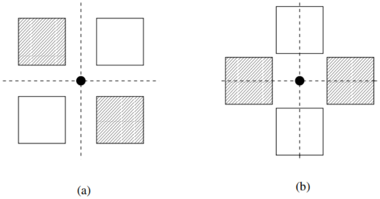
[1] Hao Chen et al. (1993). "Challenges and opportunities toward fully automated analog layout design". In: *The Journal of Supercomputing* 41.11, pp. 1674–4926.

Geometric Matching in Placement

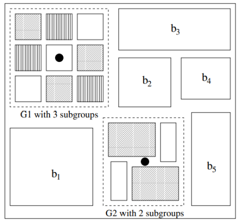
The existing analog layout placement methods are mainly focused on optimizing *proxy* objectives for performance:

- **Symmetry and common centroid**[2];

For example, using common centroid placement to reduce parasitic mismatch.
Question: Is symmetry good enough for the performance?



2-D symmetry (b) does not include placement (a) which also satisfies the common centroid constraint.



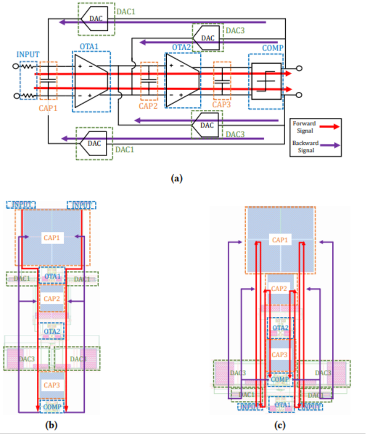
A packing with two common centroid groups.

[2]Qiang Ma, Evangeline F. Y. Young, and K. P. Pun (2007). "Analog placement with common centroid constraints". In: *Proc. ICCAD*, pp. 579–585.

Signal Path regularity for Performance-Driven Placement

- **Current path and signal flow**[3]

Zhu et al.[4] propose to consider the critical signal paths in automatic AMS placement. **Question**: enough for general circuits?

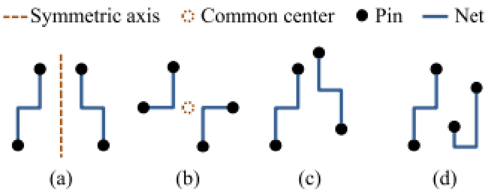


[3]Keren Zhu, Hao Chen, Mingjie Liu, et al. (2020). "Effective Analog/Mixed-Signal Circuit Placement Considering System Signal Flow". In: *Proc. ICCAD*, pp. 1–9.

The analog router cannot adopt specialized layout strategies for specific circuit classes like human layout experts, so *proxy* heuristic method is honored in performance-driven analog routing.

- **Symmetry** has been widely adopted as an essential component of the analog routing problem[5].

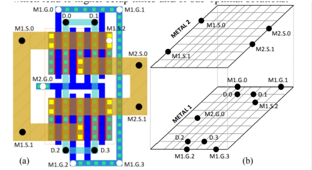
Example: different levels of geometrical matching constraints[6].



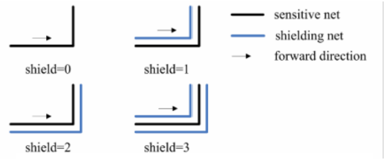
(a) Symmetric constraint. (b) Common-centroid constraint. (c) Topology-matching constraint. (d) Length-matching constraint.

[5] Hung-Chih Ou, Hsing-Chih Chang Chien, and Yao-Wen Chang (2012). "Non-uniform multilevel analog routing with matching constraints". In: *Proceedings of the 49th Annual Design Automation Conference*, pp. 549–554.

Other works optimize power routing[7] and propose shielding critical nets[8].



Optimize power routing.



Shielding critical nets.

[7]Ricardo Martins et al. (2014). "Electromigration-aware and IR-drop avoidance routing in analog multiport terminal structures". In: *2014 Design, Automation & Test in Europe Conference & Exhibition (DATE)*. IEEE, pp. 1–6.

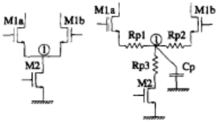
[8]Qiang Gao et al. (2010). "Analog circuit shielding routing algorithm based on net classification". In: *Proceedings of the 16th ACM/IEEE international symposium on Low power electronics and design*, pp. 123–128.

- **Linear approximation model**

Lampaert et al.[9] uses performance degradation term. Characterising performance degradation ΔP_j using the precalculated sensitivity information:

$$\Delta P_j = \sum_{k=1}^{m} \left(S^{j}_{C_{p,k}} C_{p,k} + \sum_{i=1}^{n_k} S^{j}_{R_{p,ki}} R_{p,ki} \right) \tag{1}$$

Issues: sensitivity computation scalability and accuracy.

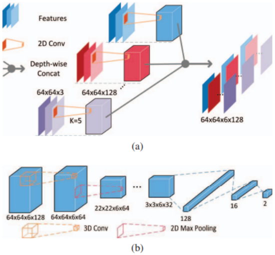


A packing with two common centroid groups.

[9] U. Choudhury and A. Sangiovanni-Vincentelli (1995). "A performance-driven placement tool for analog integrated circuits". In: *IEEE Journal Solid-State Circuits* 30.7, pp. 773–780.

Machine learning methods provide a **direct** way to model the post-layout analog performance[10]

- Automatically generate layout data and extract effective placement features based on functionality;
- Utilize 3D Convolutional Neural Networks (CNNs) as the performance predictor, incorporating coordinate channels.



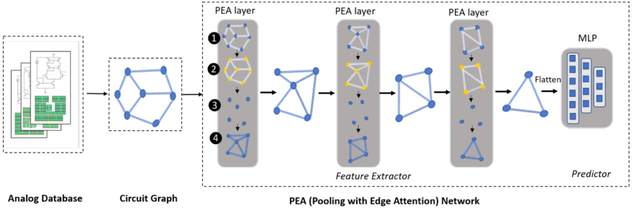
CNN

[10] Mingjie Liu, Keren Zhu, Jiaqi Gu, et al. (2020b). "Towards Decrypting the Art of Analog Layout: Placement Quality Prediction via Transfer Learning". In: *Proc. DATE*, pp. 496–501.

How to Optimize Performance in Placement and Routing?

There are also attempts to apply learning models to analog placement[11]:

- Utilize the GNN performance model as a predictor.
- Employ the performance predictor to guide the simulated annealing process.



[11] Yaguang Li, Yishuang Lin, Meghna Madhusudan, Arvind Sharma, Wenbin Xu, Sachin S. Sapatnekar, et al. (2020). "A Customized Graph Neural Network Model for Guiding Analog IC Placement". In: *Proc. ICCAD*, pp. 1–9.

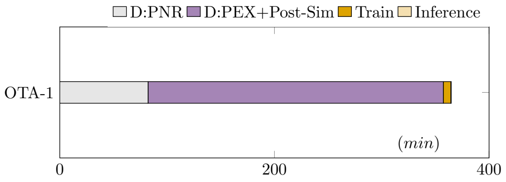
Case Study

The performance modeling cycle can be divided into three stages:

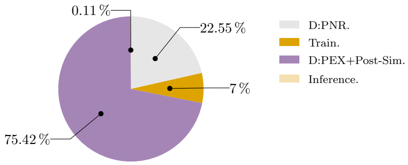
- **Data Acquisition**: The data acquisition stage includes **PNR** and parasitic parameter extraction (**PEX**) and post-layout performance simulation (**Post-Sim**).
- **Model Training**: The model training stage mainly includes the **Training** time for performance models.
- **Performance-aware PNR Inference**: The performance-aware PNR inference includes the model **Inference** time and a single **augmented PNR** process.

Case 1: Analog Performance Modeling Lifecycle

Profiling lifecycle for building a performance model on Operational Transconductance Amplifier (OTA) layout design using MAGICAL.



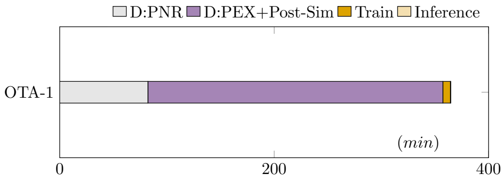
(a)



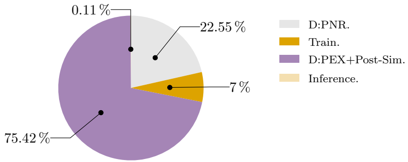
(b)

The runtime breakdown of different methods on OTA1 benchmarks.

Observations from Case 1



(a)



(b)

The runtime breakdown of different methods on OTA1 benchmarks.

We can draw two important observations from Case 1:

1. The **Data Collection** occupies **most** of the modeling lifecycle, which accounts for 92.89%.
2. The time required to obtain **inputs** $<<$ the time required to obtain **labels**. (*The PEX and Post-Sim time is roughly equivalent to 3-4 PNR iterations.*)

How to shorten the performance modeling lifecycle effectively?

Reduce the time spent on data acquisition, especially PEX and Post-Sim.

There are several promising solutions:

- From advancements in hardware-accelerated EDA workflows[12], we can see that parallelizing PEX and Post-Sim is an effective solution.
- Considering the cost of acquiring data inputs and labels, selecting representative samples through active learning[13] may also be an economically efficient approach.
- ...

[12] Siting Liu et al. (2022). "FastGR: Global Routing on CPU-GPU with Heterogeneous Task Graph Scheduler". In: *Proc. DATE*; Zhuolun He, Yuzhe Ma, and Bei Yu (2022). "X-Check: GPU-Accelerated Design Rule Checking via Parallel Sweepline Algorithms". In: *Proc. ICCAD*.

[13] Yuzhe Ma et al. (2018). "Cross-layer optimization for high speed adders: A pareto driven machine learning approach". In: *IEEE TCAD* 38.12, pp. 2298–2311.

Case 2: Exploring Model Transferability

In the case shown in the Table 1, we quantitatively discuss the issue of performance model transferability on OTA designs.

From Scratch

- A small amount of sampling data for the current design is collected.
- We then model the prediction as a binary classification problem to achieve accurate predictions[14].

Transfer

- The pre-trained model obtained from other designs is leveraged.
- We can obtain a relatively accurate model with a few samples through fine-tuning, which requires less time.

[14] Mingjie Liu, Keren Zhu, Jiaqi Gu, et al. (2020b). "Towards Decrypting the Art of Analog Layout: Placement Quality Prediction via Transfer Learning". In: *Proc. DATE*, pp. 496–501.

Case 2: Exploring Model Transferability

We mainly consider two scenarios of Transfer:

Transfer between the same topology

- We first train a performance model on OTA3. **OTA3 has the same topology and different sizing configurations as OTA1.**
- We then test the accuracy of model predictions on OTA1.

Transfer between different topologies

- We first train a performance model on OTA3. **OTA3 has different topologies from OTA2.**
- We then test the accuracy of model predictions on OTA2.

Observations from Case 2

Table: Placement prediction results for training from scratch and transfer learning results.

Design	Prediction Accuracy Metrics	From Scratch	Transfer	Acc-Δ
OTA1	Offset Voltage(%)	**95.54**	91.67	3.87
	CMRR(%)	**91.96**	77.68	14.29
	BandWidth(%z)	**96.43**	95.54	0.89
	DC Gain(%)	**93.62**	88.01	5.61
	Noise(%)	**91.96**	79.14	12.82
OTA2	Offset Voltage(%)	**81.35**	65.39	15.96
	CMRR(%)	**82.33**	62.02	20.31
	BandWidth(%)	**80.71**	72.14	8.58
	DC Gain(%)	**81.35**	59.50	21.85
	Noise(%)	**88.80**	69.29	19.52

From these data results, we can identify two important findings:

- The transferability of the models varies under different scenarios and metrics, with the accuracy reduction ranging from 3% to 22%.
- Transfer between different sizing configurations is often easier than transfer between different topologies.

Lessons from the Performance Modeling Transferability

From a Generalization Perspective

- We consider how to improve transfer training by obtaining effective pretraining weights using methods like meta-learning[15].

From a Detection Perspective

- We consider different distributions to determine when the transfer is safe.
- Current research on out-of-distribution (OOD) detection[16] provides technical support for identifying when the model is effective.

[15] Timothy Hospedales et al. (2021). "Meta-learning in neural networks: A survey". In: *IEEE Transactions on Pattern Analysis and Machine Intelligence* 44.9, pp. 5149–5169.

[16] Qitian Wu et al. (2022). "Energy-based Out-of-Distribution Detection for Graph Neural Networks". In: *Proc. ICLR*.

Case 3: Navigating the Multi-Objective Pitfall

In this case, we aim to demonstrate the importance of multi-objective optimization by comparing the placements obtained through weighted-based Bayesian optimization (BO) and multi-objective optimization Bayesian optimization (MOBO)[17] in four OTA benchmarks.

Weighted Method

- It is common practice to use a user-defined figure-of-merit (FOM) representation, a weighted sum of post-layout simulation metrics.

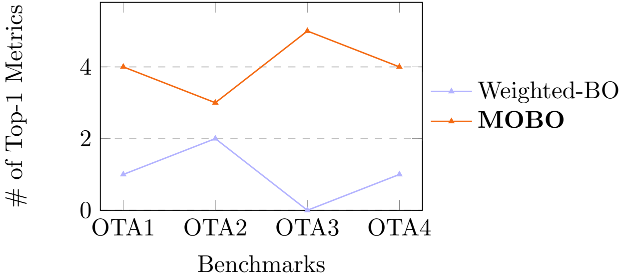
Multi-objective Optimization

- One alternative objective is to find solutions not dominated by others, known as **Pareto optimal solutions**.
- The problem of finding Pareto optimal solutions given multiple criteria is called **multi-objective optimization**.

[17] Mingjie Liu, Keren Zhu, Jiaqi Gu, et al. (2020a). "Closing the Design Loop: Bayesian Optimization Assisted Hierarchical Analog Layout Synthesis". In: *Proc. DAC*, pp. 496–501.

Observations from Case 3

As shown in Figure 12, the MOBO method outperforms Weighted-BO in terms of the number of top-1 metrics achieved for the obtained layout.



The number of top-1 metrics for different methods.

- MOBO achieves top-1 performance in almost all metrics in Offset Voltage, CMRR, BandWidth, and DC Gain.
- For all designs, MOBO outperforms the Weighted-BO for 3 to 5 metrics.

Lessons from the Multi-Objective Pitfall

- The results corroborate that the multi-objective optimization method moves the layout solution toward the Pareto frontier.
- Recent advancements have been witnessed in the field of multi-objective optimization, especially for **gradient-based strategies**[18].
- It is imperative to carefully consider how these advancements in the field of multi-objective optimization can be applied to enhance performance-driven analog layout automation.

[18] Jörg Fliege and Benar Fux Svaiter (2000). "Steepest descent methods for multicriteria optimization". In: *Mathematical Methods of Operations Research* 51, pp. 479–494; Stefan Schäffler, Reinhart Schultz, and Klaus Weinzierl (2002). "Stochastic method for the solution of unconstrained vector optimization problems". In: *Journal of Optimization Theory and Applications* 114, pp. 209–222; Jean-Antoine Désidéri (2012). "Multiple-gradient descent algorithm (MGDA) for multiobjective optimization". In: *Comptes Rendus Mathematique* 350.5-6, pp. 313–318.

Perspectives and Future Directions

Challenges in Modeling Performance-I

Efficient Data Acquisition

- Data collection bottleneck in building performance models;
- Active learning for selecting representative samples[19];
- Smart layout selection for an efficient training process;
- Accelerating simulation for more training data[20];

[19] Yuzhe Ma et al. (2018). "Cross-layer optimization for high speed adders: A pareto driven machine learning approach". In: *IEEE TCAD* 38.12, pp. 2298–2311.

[20] Tengcheng Wang et al. (2023). "Accelerating Sparse LU Factorization with Density-Aware Adaptive Matrix Multiplication for Circuit Simulation". In: *Proc. DAC*; Dan Niu et al. (2023). "OSSP-PTA: An Online Stochastic Stepping Policy for PTA on Reinforcement Learning". In: *IEEE TCAD* 42.11, pp. 4310–4323.

Challenges in Modeling Performance-II

Better Transferability

- Transferring pre-trained models to unseen circuits Managing multimodal input features;
- A general multimodal neural network for performance modeling may benefit the field[21];
- Adopting a pretraining methodology for data efficiency[22];

[21] Mingjie Liu, Keren Zhu, Jiaqi Gu, et al. (2020c). "Towards Decrypting the Art of Analog Layout: Placement Quality Prediction via Transfer Learning". In: *Proc. DATE*; Yaguang Li, Yishuang Lin, Meghna Madhusudan, Arvind Sharma, Wenbin Xu, Sachin Sapatnekar, et al. (2020). "A Customized Graph Neural Network Model for Guiding Analog IC Placement". In: *Proc. ICCAD*.

[22] Keren Zhu, Hao Chen, Walker J. Turner, et al. (2022). "TAG: Learning Circuit Spatial Embedding from Layouts". In: *Proc. ICCAD*.

Challenges in Physical Design Optimization-I

Placement and Routing Representation

- Placement and Routing Representation: An overlooked problem in ML-enabled performance-driven analog physical design is how to represent placement and routing. The work[23] treats the performance modeling as a black box.
- Bridging Placement and Routing Representation for Optimization: BO-based framework tunes net weights as a proxy to generate different placements in[24].

[23] Yaguang Li, Yishuang Lin, Meghna Madhusudan, Arvind Sharma, Wenbin Xu, Sachin Sapatnekar, et al. (2020). "A Customized Graph Neural Network Model for Guiding Analog IC Placement". In: *Proc. ICCAD*.

[24] Mingjie Liu, Keren Zhu, Xiyuan Tang, et al. (2020). "Closing the Design Loop: Bayesian Optimization Assisted Hierarchical Analog Layout Synthesis". In: *Proc. DAC*.

Challenges in Physical Design Optimization-II

Multi-objective Optimization

- Complexity of analog circuit performance
- Multiple competing performance metrics
- Efficient and effective multi-objective physical design optimization

THANK YOU!