CENG3420
Lab 3-2: RISCV-LC Datapath

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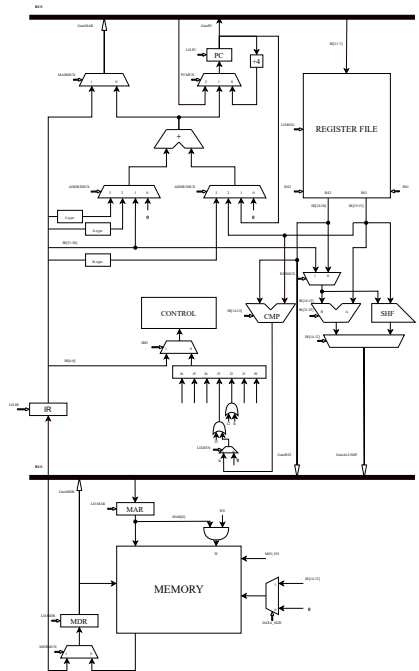
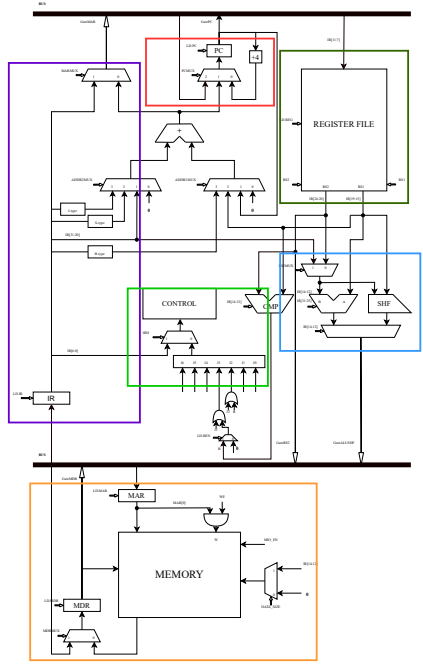
Overview

Overview

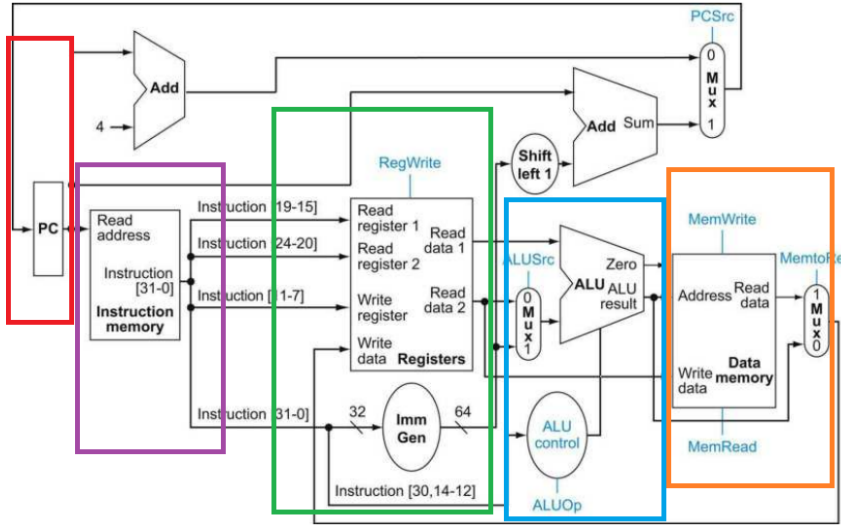
Datapath



Datapath Annotation



Datapath Annotation

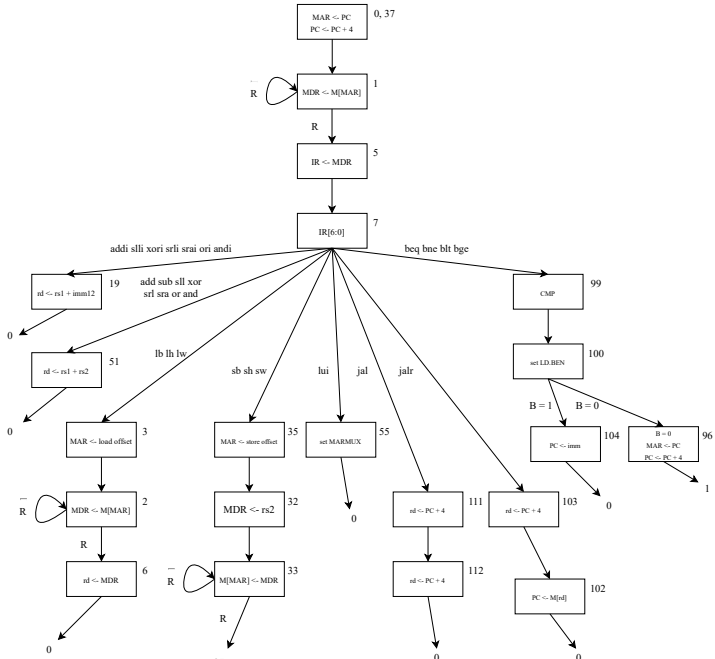


RISCV datapath annotation based on the textbook

FSM

- Clock cycle: The cycle time of a microprocessor is the duration of a clock cycle
- Finite State Machine: The behavior of the RISCV-LC microarchitecture during a given clock cycle is completely determined by the 33 control signals. These 33 control signals specify the state of the control structure of the RISCV-LC microarchitecture.

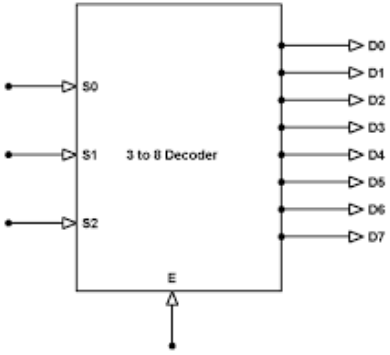
FSM


MAR <- PC
PC <- PC + 4
0, 37
R
MDR <- M[MAR]
1
R
IR <- MDR
5
IR[6:0]
7
addi slli xori srli srai ori andi
beq bne blt bge
rd <- rs1 + imm12
19
add sub sll xor
srl sra or and
CMP
99
0
rd <- rs1 + rs2
51
lb lh lw
sb sh sw
lui
jal
jalr
set LD.BEN
100
B = 1
B = 0
0
MAR <- load offset
3
MAR <- store offset
35
set MARMUX
55
PC <- imm
104
B = 0
MAR <- PC
PC <- PC + 4
96
1
R
MDR <- M[MAR]
2
MDR <- rs2
32
0
rd <- PC + 4
111
rd <- PC + 4
103
0
R
rd <- MDR
6
R
M[MAR] <- MDR
33
rd <- PC + 4
112
PC <- M[rd]
102
0
R
0
0

Overview

MUXs

You should pay attention to some MUXs



3-8 Decoder

- A2,A1,A0→Y0~~Y7
- 000→0 1 1 1 1 1 1 1
- 001→1 0 1 1 1 1 1 1
- 010→1 1 0 1 1 1 1 1
- 011→1 1 1 0 1 1 1 1
- 100→1 1 1 1 0 1 1 1
- 101→1 1 1 1 1 0 1 1
- 110→1 1 1 1 1 1 0 1
- 111→1 1 1 1 1 1 1 0

3-8 Decoder Truth Table

MUXs

- blockDATASIZEMUX: related to DATA_SIZE, i.e., sb/sh/sw/lb/lh/lw (IR[14:12], 0)
- blockADDR2MUX (0, SEXT(IR[31:20]) SEXT(S-type), SEXT(J-type))
- blockADDR1MUX (0, PC, IR[19:15], SEXT(B-type))
- blockMARMUX (valueOfMARMUXFromAdder, IR[31: 12] « 20)
- blockRS2MUX (REGS[IR[24, 20]], sext(IR[31:20]))
- blockALUSHFMUX (valueOfALU, valueOfSHF)
- blockMDRMUX (MemOut, BUS)
- blockPCMUX (PC + 4, BUS)

Tristate Drivers

You should pay attention to BUS values, and it can be

- 0
- valueOfGateMAR
- valueOfGateALUSHF
- valueOfGatePC
- valueOfGateRS2
- valueOfGateMDR

How do we assign BUS with these value?

0 - BUS = 0

1 - BUS = valueOfGateMAR

2 - BUS = valueOfGateALUSHF

4 - BUS = valueOfGatePC

8 - BUS = valueOfGateRS2

16 - BUS = valueOfGateMDR

Overview

Background

Introduction

Lab3-2 Assignment

Lab3.2 Assignment

It is challenging! In fact, there is still a plenty of optimization opportunities for the current system.

RISCV-LC codes have been released on 22 Apr.

- git clone https://github.com/baichen318/ceng3420.git; cd ceng3420
- git checkout lab3.2

Compile (Linux + x86_64 environment is suggested)

- make

Run RISCV-LC

- ./lc uop benchmarks/isa.bin # RISCV-LC runs isa.bin

Lab3.2 Assignment

- Finish cycle_memory
- Finish eval_bus_drivers
- Finish drive_bus
- Finish latch_datapath_values

These unimplemented codes are annotated with Lab3-2 assignment

Lab3.2 Assignment

Verify your codes with binary machine codes suffixed with .bin

- isa.bin
- count10.bin
- swap.bin

Submission Method:

Prepare a package into blackboard, including

- All source codes (C source files, header files, Makefile, etc.)
- A lab report (`<name-sid>-lab3.pdf`) with all console results and some illustrations of your implementation.
- Deadline: 23:59, 11 May

Thanks. For any question:

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