

2. Working speed decrease and storage size increase along above hierarchy level.

Q3 For the given SR Latch in Figure 2. Assume the initial state of \bar{Q} is 1. Try to draw the waveform of Q if S, R, and E(Clk) have shown in Figure 3.

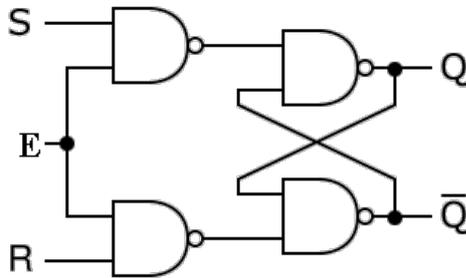


Figure 2: Gated SR Latch.

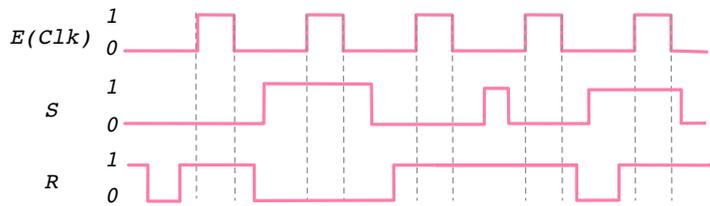
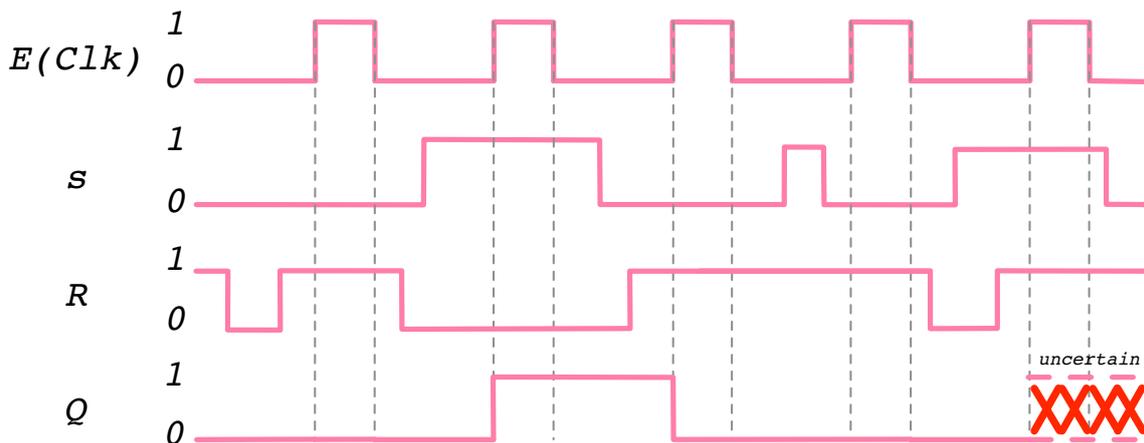


Figure 3: Gated SR Latch.

A3 The waveform is shown as in the following figure:



Q4 Design a finite state machine to detect the pattern of “11001” in the bit stream. How many states are required? Draw the state transition graph.

A4 The state transition graph is shown in the following figure:

You can also draw the **state transition table** as follows¹:

State	Coding	Current State	Input	Next State
S0	Initial	S0	0/1	S0/S1
S1	1	S1	0/1	S0/S2
S2	11	S2	0/1	S3/S2
S3	110	S3	0/1	S4/S1
S4	1100	S4	0/1	S0/S5
S5	11001	S5	0/1	S0/S2

¹Note: state transition graph and state transition table are equivalent, thus you only need to provide one.

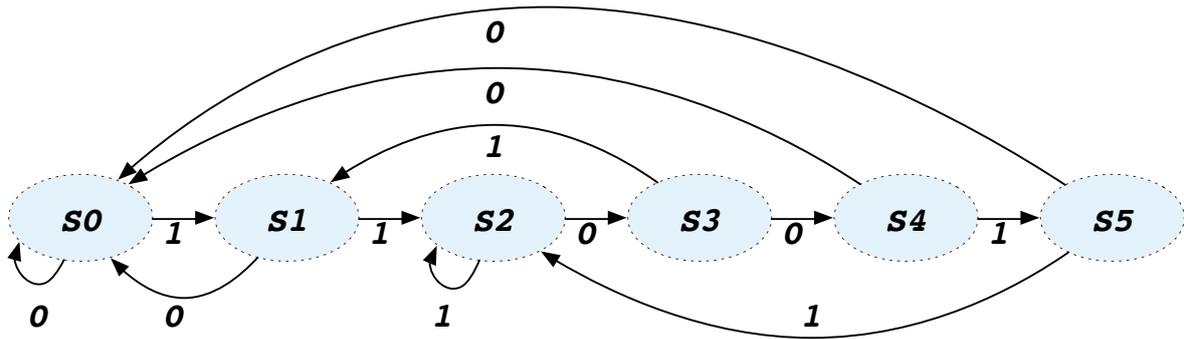
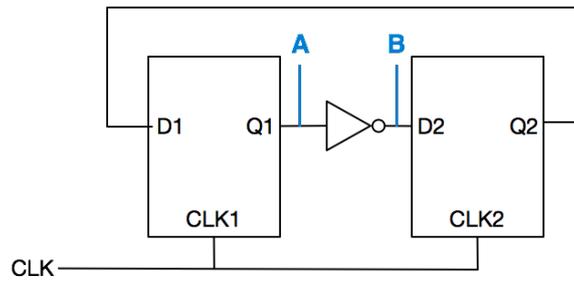


Figure 4: A4

Q5 A digital clock is important in circuit design. Please answer the following **three** questions.

(a) Given the following circuit, CLK1 = CLK2 = 25MHz; Tff = 5ns; Tsetup = 5ns. The gate delay TG = 10ns. Please calculate the time margin. Note: Tff= delay of a flip flop, Tsetup=setup time of a flip flop, and TG is delay of a gate.



(b) In the above circuit, currently there is already one delay gate with delay TG. How many more similar delay gates can you insert between A and B without creating error?

(c) Sometimes we can take advantage of clock skew. For the above circuit, if the delay from CLK to CLK2 is 4ns, calculate the minimal clock period of the clock CLK.

A5 1. $\text{Period} = \frac{1}{25\text{M}} = 40\text{ns}$. $\text{Margin} = 40 - 5 - 5 - 10 = 20\text{ns}$

2. $\text{Max \#gate} = \frac{20}{10} = 2$. So 2 more gates can be inserted.

3. Since we are searching for minimal period, no slack is desired.

$$T_{c1} + T_{ff} + T_G + T_{\text{setup}} = T_{\text{CLK}} + T_{c2} \quad (1)$$

From Equation (1) we have $T_{\text{CLK}} = 20 + T_{c1} - T_{c2}$. We set $T_{c1} = 0$, then we can obtain $T_{\text{CLK}} = 16\text{ns}$