香港中文大學
The Chinese University of Hong Kong

CENG3420

Lab 3-3: RISC-V Litter Computer (RISC-V LC)

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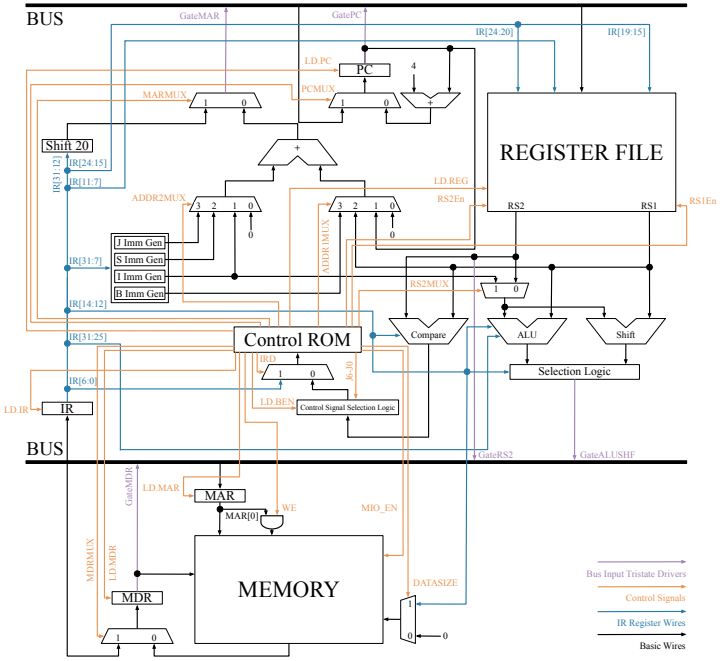
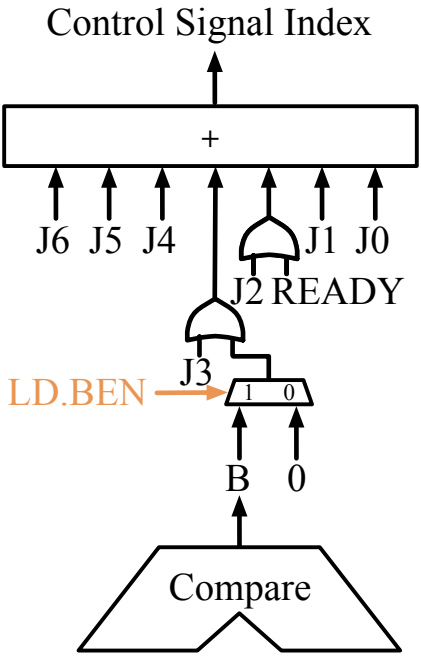
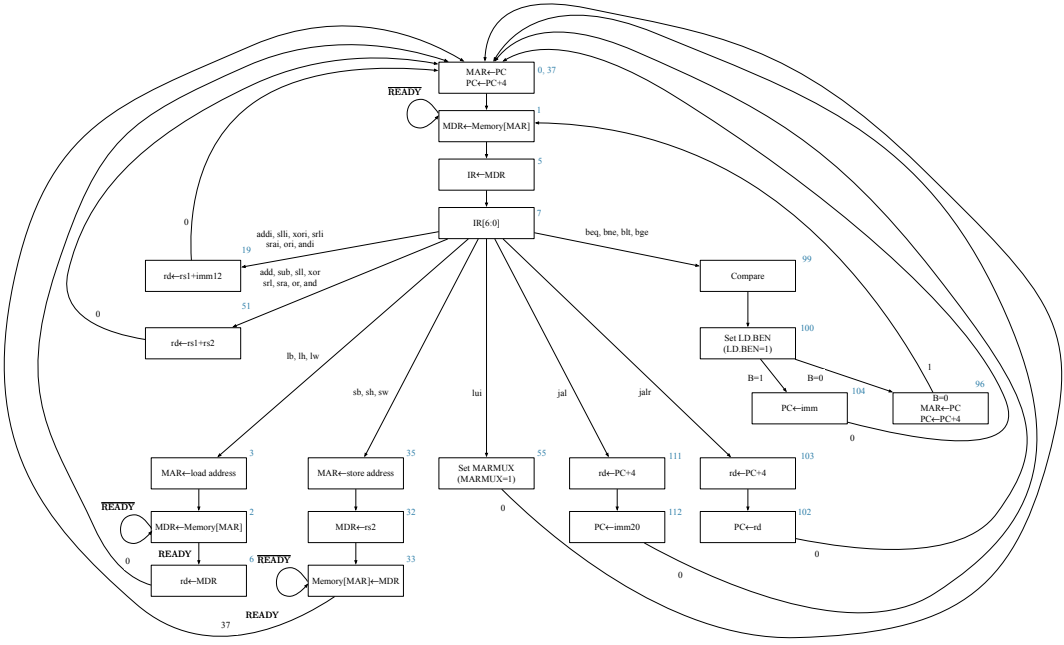
Spring 2022

Outline

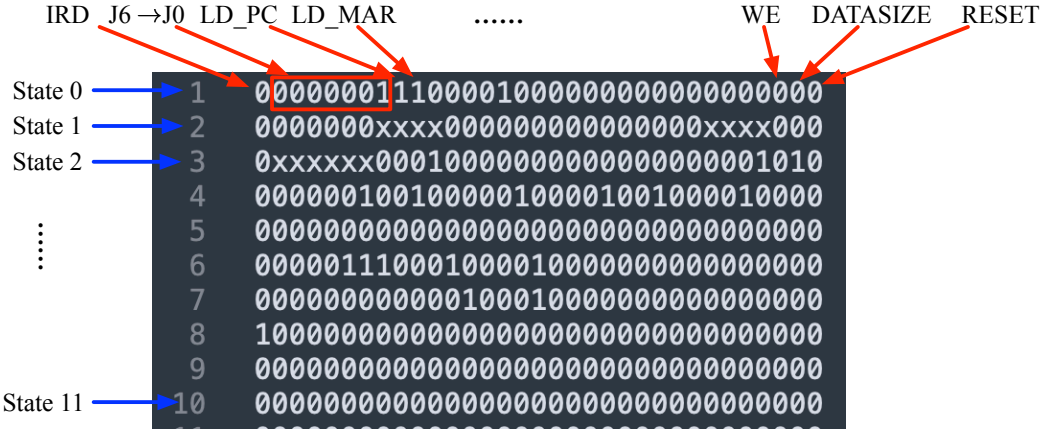
Introduction


BUS
GateMAR
GatePC
IR[24:20]
IR[19:15]
LD.PC
PC
4
+
MARMUX
PCMUX
REGISTER FILE
Shift 20
IR[24:15]
IR[31:12]
IR[11:7]
ADDR2MUX
LD.REG
RS2En
RS2
RS1
RS1En
ADDR1MUX
J Imm Gen
S Imm Gen
I Imm Gen
B Imm Gen
IR[31:7]
IR[14:12]
RS2MUX
IR[31:25]
Control ROM
Compare
ALU
Shift
IRD
IR[6:0]
Selection Logic
LD.IR
IR
LD.BEN
Control Signal Selection Logic
GateRS2
GateALUSHF
BUS
GateMDR
LD.MAR
MAR
MAR[0]
WE
MIO_EN
MDRMUX
LD.MDR
MEMORY
DATASIZE
MDR
Bus Input Tristate Drivers
Control Signals
IR Register Wires
Basic Wires


Control Signal Index
+
J6
J5
J4
J1
J0
J2 READY
J3
LD.BEN
1
0
B
0
Compare

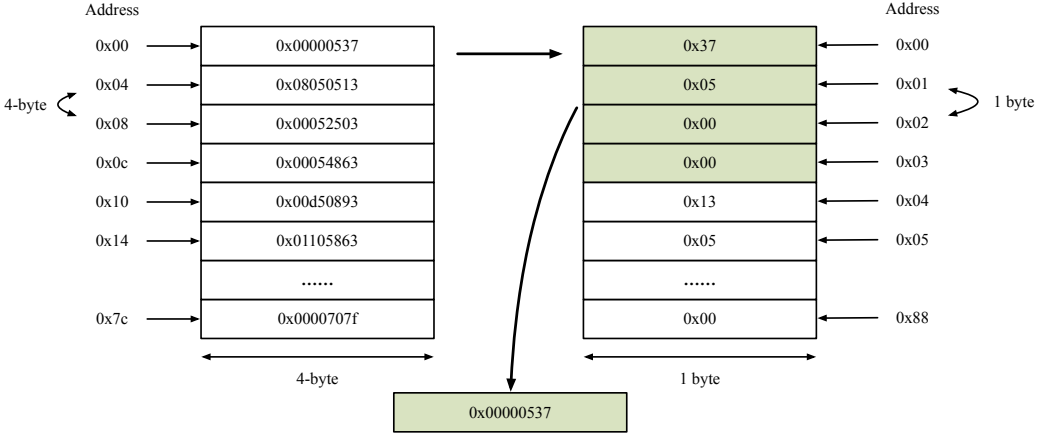

MAR←PC
PC←PC+4
0, 37
READY
MDR←Memory[MAR]
1
IR←MDR
5
IR[6:0]
7
addi, slli, xori, srli
srai, ori, andi
19
rd←rs1+imm12
add, sub, sll, xor
srl, sra, or, and
51
rd←rs1+rs2
beq, bne, blt, bge
99
Compare
100
Set LD.BEN
(LD.BEN=1)
B=1
B=0
104
PC←imm
96
B=0
MAR←PC
PC←PC+4
lb, lh, lw
sb, sh, sw
lui
jal
jalr
3
MAR←load address
35
MAR←store address
55
Set MARMUX
(MARMUX=1)
111
rd←PC+4
103
rd←PC+4
2
MDR←Memory[MAR]
32
MDR←rs2
112
PC←imm20
102
PC←rd
6
rd←MDR
33
Memory[MAR]←MDR
37

Details



Micro-ops specifications

Source codes ↔ Machine codes ↔ Organization in memory



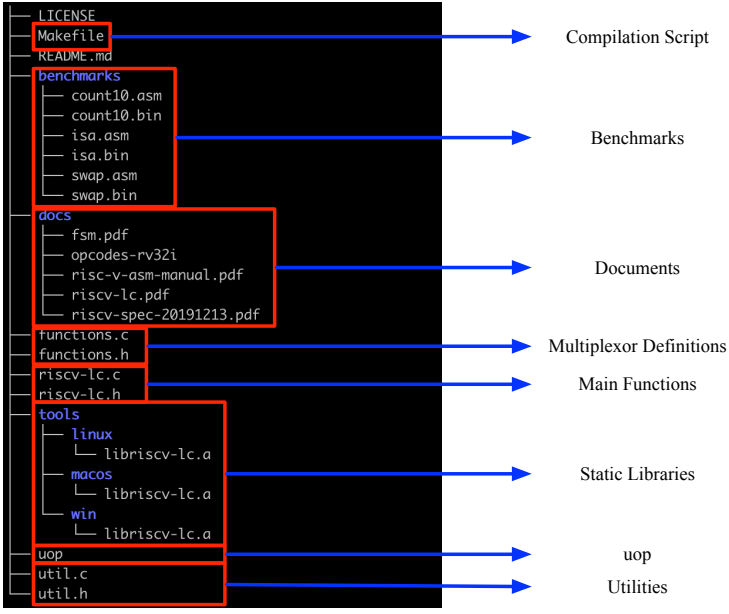
RISCV-LC adopts little endian one-byte addressed memory.

add a4, a2, a0

- PC $\rightarrow$ BUS
  - In state 0, GatePC is asserted.
- BUS $\rightarrow$ MAR
  - In state 0, LD_MAR is asserted.
- PC $+4 \rightarrow$ PC
  - In state 0, PCMUX is deasserted, and LD_PC is asserted.
- Memory[MAR] $\rightarrow$ MDR
  - In state 1, the step will take `MEM_CYCLES` clocks.)
  - J0, LD_MDR, MIO_EN are asserted.
- MDR $\rightarrow$ BUS
  - In state 5, J2, J1, J0 are asserted, GateMDR is asserted.
- BUS $\rightarrow$ IR
  - In state 5, LD_IR is asserted.

- Generate control signals according to IR[6:0]
  - In state 7, IRD is asserted.
- R-type addition: a2 + a0
  - In state 51, J6 $\sim$ J0 are deasserted, RS2En, RS1En are asserted.
- R-type addition: results write back to a4
  - In state 51, LD_REG, GateALUSHF are asserted.
- Go back to state 0

Implementations


LICENSE
Makefile
README.md
benchmarks
count10.asm
count10.bin
isa.asm
isa.bin
swap.asm
swap.bin
docs
fsm.pdf
opcodes-rv32i
risc-v-asm-manual.pdf
riscv-lc.pdf
riscv-spec-20191213.pdf
functions.c
functions.h
riscv-lc.c
riscv-lc.h
tools
linux
libriscv-lc.a
macos
libriscv-lc.a
win
libriscv-lc.a
uop
util.c
util.h
Compilation Script
Benchmarks
Documents
Multiplexor Definitions
Main Functions
Static Libraries
uop
Utilities

```
/*
 * execute a cycle
 */
void cycle() {
    /*
     * core steps
     */
    eval_micro_sequencer();
    cycle_memory();
    eval_bus_drivers();
    drive_bus();
    latch_datapath_values();

    CURRENT_LATCHES = NEXT_LATCHES;

    CYCLE_COUNT++;
}
```

```
value_of_GatePC = 0;
value_of_GateMAR = 0;
value_of_GateMDR = 0;
value_of_GateALUSHF = 0;
value_of_GateRS2 = 0;
```

```
int value_of_MARMUX = 0,
value_of_alu,
value_of_shift_function_unit = 0;
```

```
value_of_MARMUX = addr2_mux(
    get_ADDR2MUX(CURRENT_LATCHES.MICROINSTRUCTION),
    0,
    sext_unit(mask_val(CURRENT_LATCHES.IR, 31, 20), 12),
    sext_unit(
        s_format_imm_gen_unit(
            mask_val(CURRENT_LATCHES.IR, 11, 7),
            mask_val(CURRENT_LATCHES.IR, 31, 25)
        ),
        12
    ),
    sext_unit(
        j_format_imm_gen_unit(
            mask_val(CURRENT_LATCHES.IR, 31, 31),
            mask_val(CURRENT_LATCHES.IR, 30, 21),
            mask_val(CURRENT_LATCHES.IR, 20, 20),
            mask_val(CURRENT_LATCHES.IR, 19, 12)
        ),
        20
```

```
        )
    ) + addr1_mux(
        get_ADDR1MUX(CURRENT_LATCHES.MICROINSTRUCTION),
        0,
        CURRENT_LATCHES.PC,
        rs1_en(
            get_RS1En(CURRENT_LATCHES.MICROINSTRUCTION),
            0,
            CURRENT_LATCHES.REGS[mask_val(CURRENT_LATCHES.IR, 19,
                15)]
        ),
        sext_unit(
            b_format_imm_gen_unit(
                mask_val(CURRENT_LATCHES.IR, 7, 7),
                mask_val(CURRENT_LATCHES.IR, 11, 8),
                mask_val(CURRENT_LATCHES.IR, 30, 25),
                mask_val(CURRENT_LATCHES.IR, 31, 31)
            ),
            12
```

```
        )
    );
```

```
value_of_alu = alu(
    mask_val(CURRENT_LATCHES.IR, 14, 12),
    mask_val(CURRENT_LATCHES.IR, 31, 25),
    rs1_en(
        get_RS1En(CURRENT_LATCHES.MICROINSTRUCTION),
        0,
        CURRENT_LATCHES.REGS[mask_val(CURRENT_LATCHES.IR, 19,
            15)]
    ),
    rs2_mux(
        get_RS2MUX(CURRENT_LATCHES.MICROINSTRUCTION),
        rs2_en(
            get_RS2En(CURRENT_LATCHES.MICROINSTRUCTION),
            0,
            CURRENT_LATCHES.REGS[mask_val(CURRENT_LATCHES.IR,
                24, 20)]
        ),
        sext_unit(mask_val(CURRENT_LATCHES.IR, 31, 20), 12)
    )
```

```
);
```

```
int _GateMAR = get_GateMAR(CURRENT_LATCHES.MICROINSTRUCTION);
int _GateALUSHF = get_GateALUSHF(CURRENT_LATCHES.
    MICROINSTRUCTION);
int _GatePC = get_GatePC(CURRENT_LATCHES.MICROINSTRUCTION);
int _GateRS2 = get_GateRS2(CURRENT_LATCHES.MICROINSTRUCTION);
int _GateMDR = get_GateMDR(CURRENT_LATCHES.MICROINSTRUCTION);
```

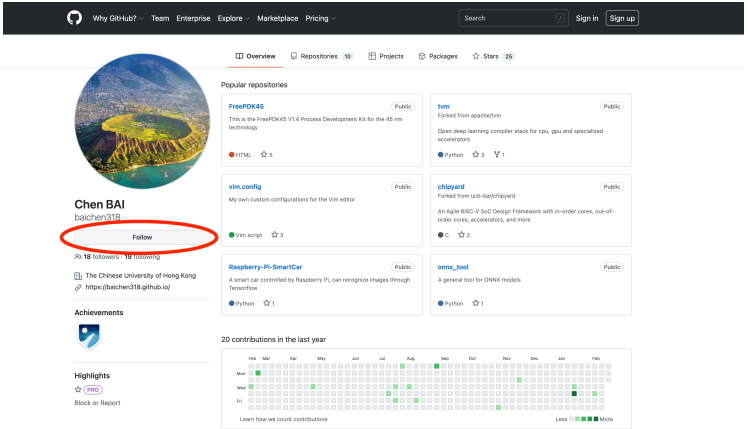
```
switch ((_GateMDR << 4) + (_GateRS2 << 3) + (_GatePC << 2) + (
    _GateALUSHF << 1) + (_GateMAR)) {
    case 0:
        BUS = 0;
        break;
    case 1:
        error("Lab3-3␣assignment:␣when␣value␣=␣1,␣BUS␣=␣?;\n")
            ;
    case 2:
        error("Lab3-3␣assignment:␣when␣value␣=␣1,␣BUS␣=␣?;\n")
            ;
    case 4:
        error("Lab3-3␣assignment:␣when␣value␣=␣1,␣BUS␣=␣?;\n")
            ;
    case 8:
        error("Lab3-3␣assignment:␣when␣value␣=␣1,␣BUS␣=␣?;\n")
            ;
    case 16:
```

```
            error("Lab3-3␣assignment:␣when␣value␣=␣1,␣BUS␣=␣?;\n")
                ;
        default:
            BUS = 0;
            warn("unknown␣gate␣drivers␣for␣BUS\n");
}
```

Lab 3-3 Assignment

Get Latest Updates of the Lab

- Click `https://github.com/baichen318`.
- Follow my GitHub account.
  Follow me through GitHub, so that you can see any latest updates of the lab!



Get RISC-V LC

- $ git clone https://github.com/baichen318/ceng3420.git
- $ cd ceng3420
- $ git checkout lab3.3

Compile (Linux/MacOS environment is suggested)

- $ make

Run the RISC-V LC

- $ ./riscv-lc <uop> <*.bin> # RISCV-LC can execute successfully if you have implemented it.

In **riscv-lc.c**,

- Finish eval_bus_drivers
- Finish drive_bus

These unimplemented codes are commented with Lab3-3 assignment.

Benchmarks

Verify your codes with these benchmarks (inside the `benchmarks` directory)

- isa.bin
- count10.bin
- swap.bin

Verification

- isa.bin → a3 = -18/0xffffffee and MEMORY[0x84 + 16] = 0xffffffee
- count10.bin → t2 = 55/0x00000037
- swap.bin → NUM1 changes from 0xabcd to 0x1234 and NUM2 changes from 0x1234 to 0xabcd

Submission Method:

Submit a zip file into **Blackboard**. The zip file includes

- Your implementations, *i.e.*, three riscv-lc.c source codes for three parts of Lab 3. The sources should be renamed to `name-sid-lab3-1.c`, `name-sid-lab3-2.c`, and `name-sid-lab3-3.c`, respectively (*e.g.*, `zhangsan-1234567890-lab3-1.c`, `zhangsan-1234567890-lab3-2.c`, *etc.*).
- A lab report (`name-sid-lab3.pdf`) illustrates your implementation for three parts of Lab 3 and all console results (screenshots).

Deadline: 23:59, 30 Apr. (Sat)

Tips

Inside `docs`, there are five valuable documents for your reference!

- riscv-lc.pdf
- fsm.pdf
- opcodes-rv32i: RV32I opcodes
- riscv-spec-20191213.pdf: RV32I specifications
- risc-v-asm-manual.pdf: RV32I assembly programming manual