CENG3420 Homework 1

Due: Feb. 15, 2022

All solutions should be submitted to the blackboard in the format of **PDF/MS Word**.

Q1 (20%) Assume a 20 cm diameter wafer has a cost of 15, contains 100 dies, and has 0.030 defects/cm^2.

1. Find the yield of this wafer.
2. Find the cost per die for this wafer.

Q2 (10%) Suppose we developed a new processor that has 75% of the capacitive load of the older processor. Also it can reduce voltage 20% compared to previous generation. What is the impact on dynamic power if the frequency keeps unchanged? Give the ratio of $\frac{\text{Power}_{\text{new process}}}{\text{Power}_{\text{old processor}}}$.

Q3 (10%) For the following C statement, write the corresponding RISC-V assembly code. Assume that the C variables f, g, and h, have already been placed in registers `x5`, `x6`, and `x7` respectively. Use a minimal number of RISC-V assembly instructions.

```
f = g + (h-8)
```

Q4 (20%)

Assume the following register contents:
`x5 = 0xAAAAAAAA, x6 = 0x12345678`
1. For the register values shown above, what is the value of `x7` for the following sequence of instructions?

```
slli x7, x5, 4
or x7, x7, x6
```

2. For the register values shown above, what is the value of `x7` for the following sequence of instructions?

```
srli x7, x5, 3
andi x7, x7, 0xFEF
```

Q5 (20%) Consider the following RISC-V loop:

```
LOOP: beq x6, x0, DONE
      addi x6, x6, -1
      addi x5, x5, 2
      jal x0, LOOP
DONE:
```

1. Assume that the register `x6` is initialized to the value 10. What is the final value in register `x5` assuming the `x5` is initially zero?
2. For the loop above, write the equivalent C code. Assume that the registers `x5` and `x6` are integers `acc` and `i`, respectively.
3. For the loop written in RISC-V assembly above, assume that the register `x6` is initialized to the value N. How many RISC-V instructions are executed?
4. For the loop written in RISC-V assembly above, replace the instruction "`beq x6, x0, DONE`" with the instruction "`blt x6, x0, DONE`" and write the equivalent C code.

Q6 (20%) Some RISC-V assembly instructions are shown below. Assume that the variables f, g are assigned to registers `x5, x6`, respectively. Assume that the base address of the arrays A and B are in registers `x10` and `x11`, respectively.

```
slli x30, x5, 2 // x30 = f*4
add x30, x10, x30 // x30 = &A[f]
slli x31, x6, 2 // x31 = g*4
add x31, x11, x31 // x31 = &B[g]
lw x5, 0(x30) // x5 = A[f]
addi x12, x30, 4
lw x30, 0(x12)
add x30, x30, x5
sw x30, 0(x31)
```

1. What's the meaning of the last four instructions.
2. What is corresponding C statement?