Layout Compliance for Triple Patterning Lithography: An Iterative Approach

Bei Yu†, Gilda Garreton‡, David Z. Pan†

†ECE Dept. University of Texas at Austin, Austin, TX, USA
‡Oracle Labs, Oracle Corporation, Redwood Shores, CA, USA

09/16/2014

ORACLE

Outline

Introduction

New Challenges in Triple Patterning Lithography (TPL)

Layout Compliance Algorithms

Results and Conclusions

Outline

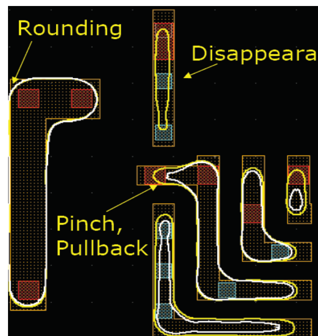
Introduction

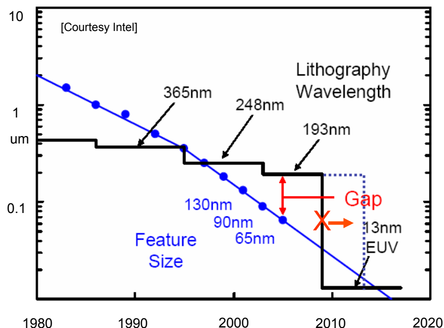
New Challenges in Triple Patterning Lithography (TPL)

Layout Compliance Algorithms

Results and Conclusions

Lithography Status & Challenges





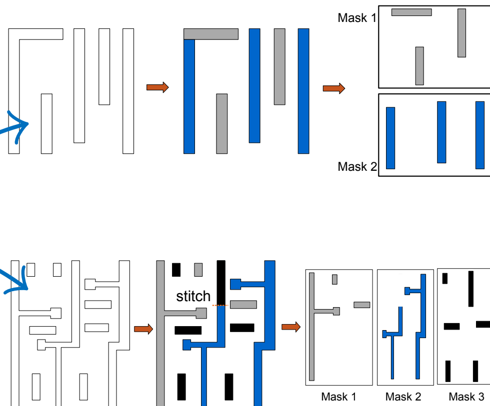
Advanced lithography to extend 193nm lithography

- Now and near future: double/triple/quadruple patterning
- Long term future: other advanced lithography

From Double Patterning to Triple Patterning

ITRS roadmap

28nm	Single Patterning
22nm	Double Patterning
14nm	Triple Patterning
11nm	Quadruple Patterning

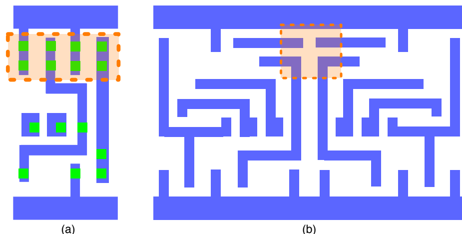


- Layout decomposition
- Patterning friendly design

Previous Works in TPL Layout Decomposition

- ILP or SAT
  [Cork+,SPIE'08][Yu+,ICCAD'11][Cork+,SPIE'13]
- Greedy or Heuristic
  [Ghaida+,SPIE'11][Fang+,DAC'12]
  [Kuang+,DAC'13][Yu+,DAC'14][Fang+,SPIE'14]
- SDP or Graph based (trade-off)
  [Yu+, ICCAD'11][Chen+,ISQED'13][Yu+,ICCAD'13]

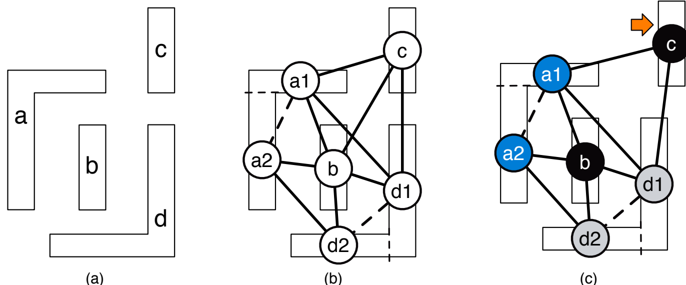
Limitations: can NOT guarantee TPL friendly



Layout Compliance Problem Formulation

Input:

- Input layout patterns (may not be TPL friendly)
- Minimum coloring distance min_s

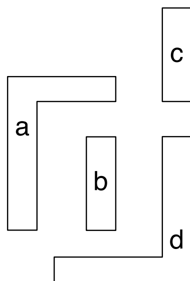


(a) (b) (c)

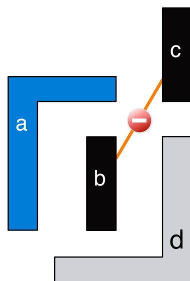
Output:

- Apply layout decomposition and layout modification
- Remove all conflicts

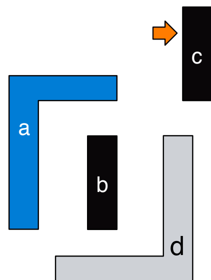
Layout Decomposition v.s. Layout Compliance



(a) Input layout



(b) Layout decomposition



(c) Layout Modification

Layout Compliance

= Layout Decomposition + Layout Modification

Outline

Introduction

New Challenges in Triple Patterning Lithography (TPL)

Layout Compliance Algorithms

Results and Conclusions

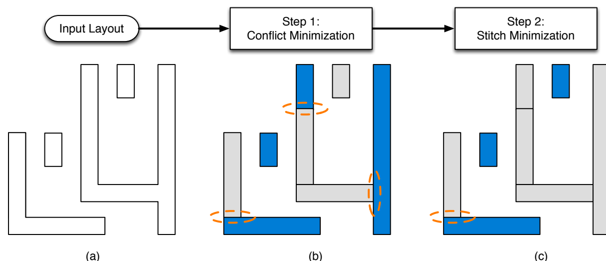
Challenge 1: NO Shortcut in TPL

Complexity

Optimizing conflict & stitch simultaneously is NP-hard for DPL/TPL.

Shortcut in DPL:

- Step by step
- Each step can be optimally solved



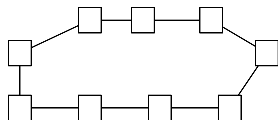
TPL:

- **NO** such shortcut, as conflict minimization is NP-hard
- Door closed?

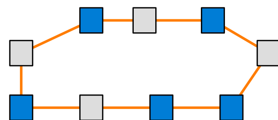
Challenge 2: Where do the conflicts come from?

DPL:

- Detect odd-cycle
- Long pattern chains



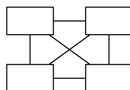
(a)



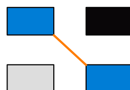
(b)

TPL:

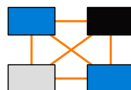
- NP-hard to detect
- But mostly local 4-clique



(a)

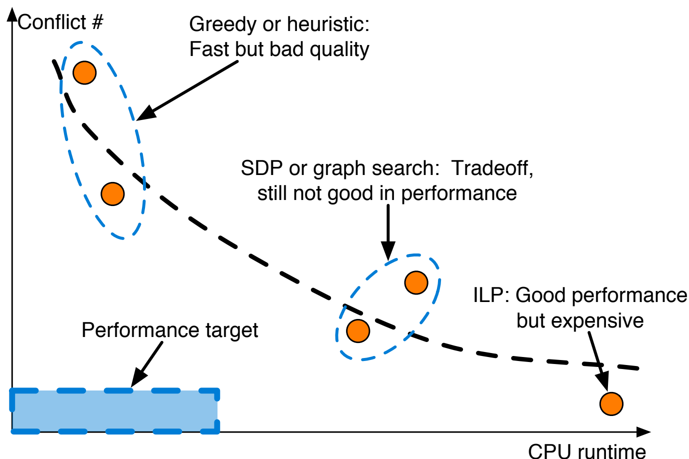


(b)



(c)

Challenge 3: Decomposer – Clutching at Straws



- Gap
- Our performance target

Outline

Introduction

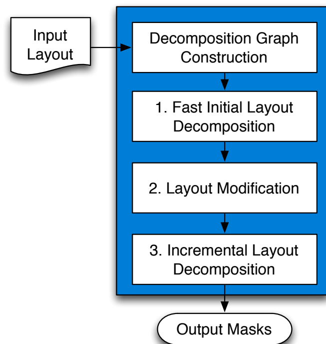
New Challenges in Triple Patterning Lithography (TPL)

Layout Compliance Algorithms

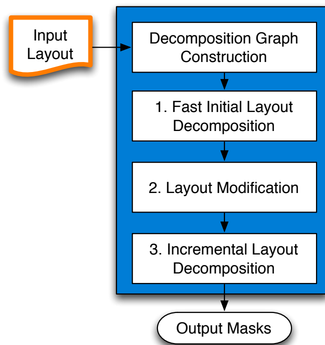
- Step 1: Initial Layout Decomposition
- Step 2: Layout Modification
- Step 3: Incremental Layout Decomposition

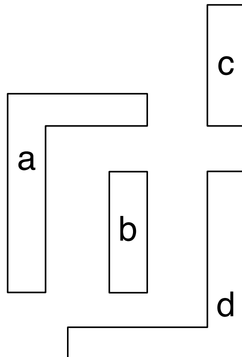
Results and Conclusions

Overall Flow

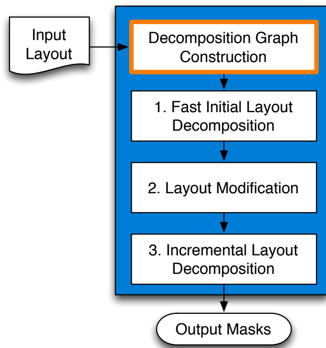


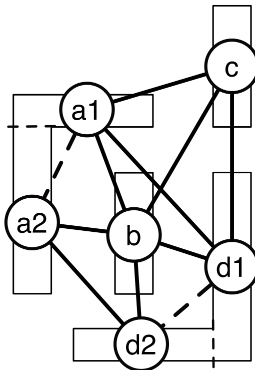
Overall Flow



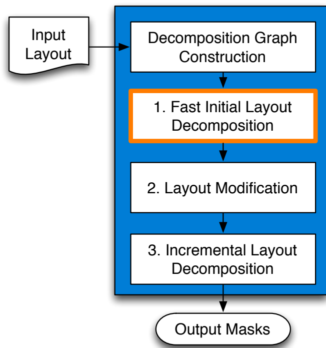


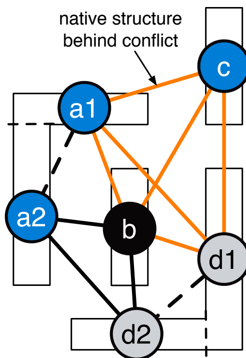
Overall Flow



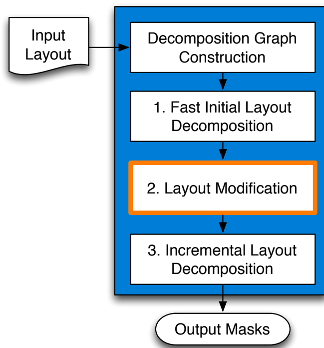


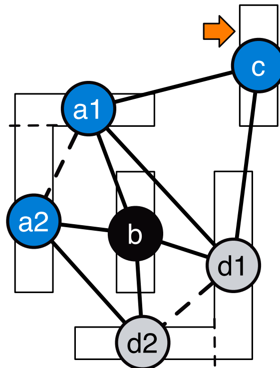
Overall Flow



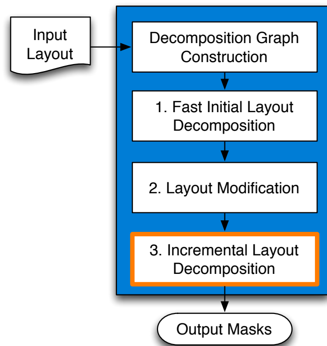


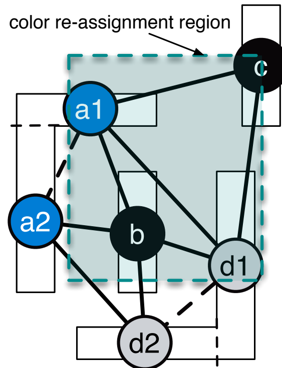
Overall Flow



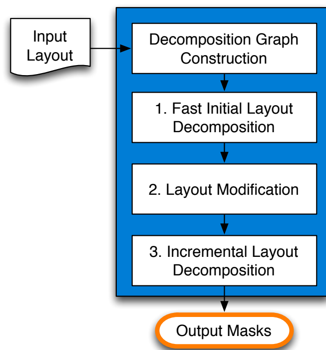


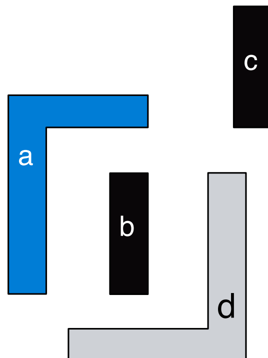
Overall Flow





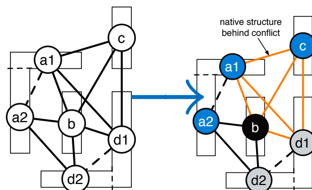
Overall Flow



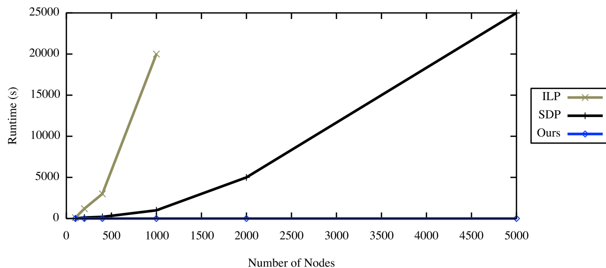


Step 1: Initial Layout Decomposition

- Our method: linear color assignment
- Linear runtime complexity [Yu+,DAC'14]
- May leave some conflicts to Step 2 & 3
- Much faster than ILP or SDP

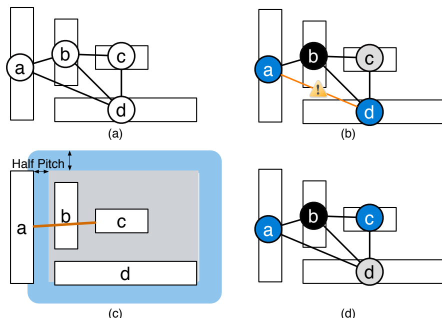


Runtime comparisions:



Step 1: Fast Layout Decomposition (cont.)

- But, Any coloring order results in **Local Optimality**
- Example: order a-b-c-d



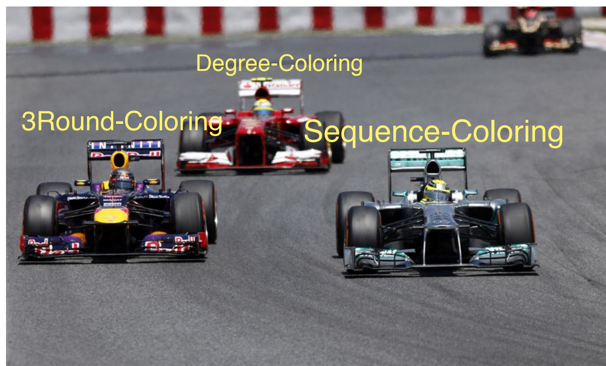
Color-Friendly Rules:

- a-c tend to be with the same color

Step 1: Fast Layout Decomposition (cont.)

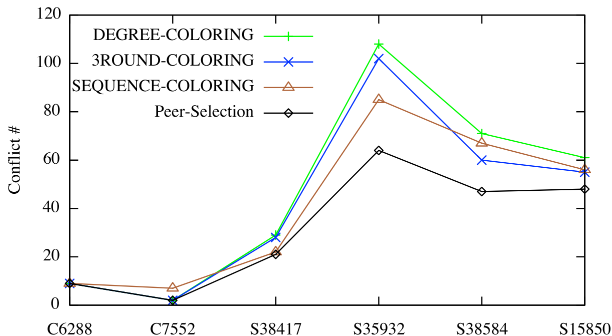
Peer Selection:

- Three orders would be processed simultaneously
- Best solution would be selected
- Still Linear runtime complexity



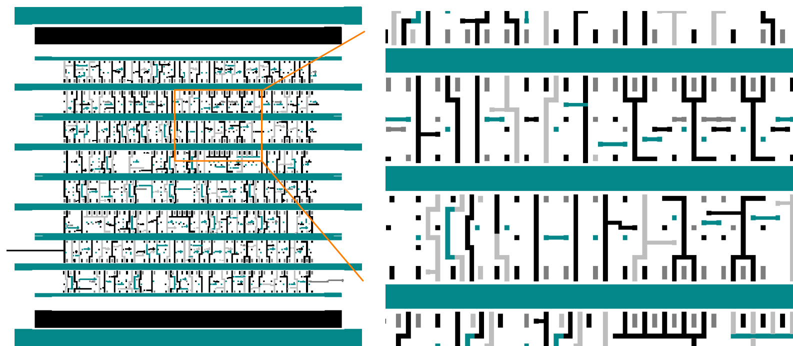
Step 1: Fast Layout Decomposition (cont.)

Peer Selection:



- Whole problem $\rightarrow$ a set of components
- Different components have different dominant orders
- Overall better results than any single order

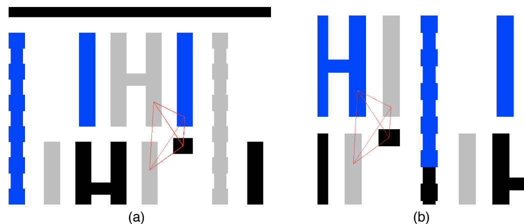
Fast Layout Decomposition Result Example



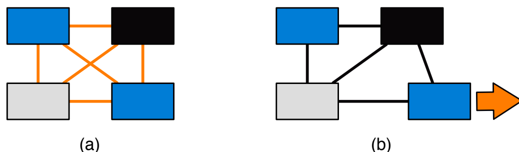
- Row by row
- Resolved in 0.1 second

Step 2: Layout Modification

Initial layout decomposition output: native conflict is labeled:

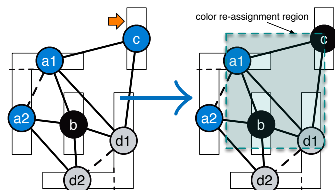


Layout modification to break down each four-clique:

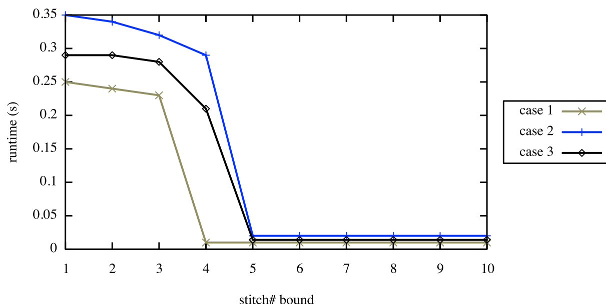


Step 3: Incremental Layout Decomposition

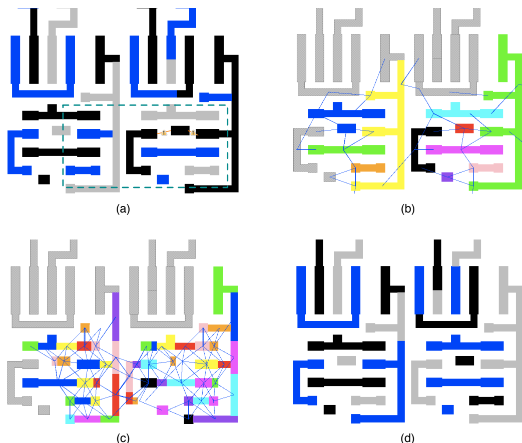
- **Input**: One layout region & stitch# bound
- **Output**: color re-assignment in the region
- **Method**: branch-and-bound
- Early return if satisfy stitch# bound



Runtiem & stitch# bound trade-off:



Step 3: Incremental Layout Decomposition– Example



- a Decomposed result after initial layout decomposition.
- b All layout patterns to be re-assigned colors are labeled.
- c The constructed local decomposition graph.
- d The result of incremental layout decomposition.

Outline

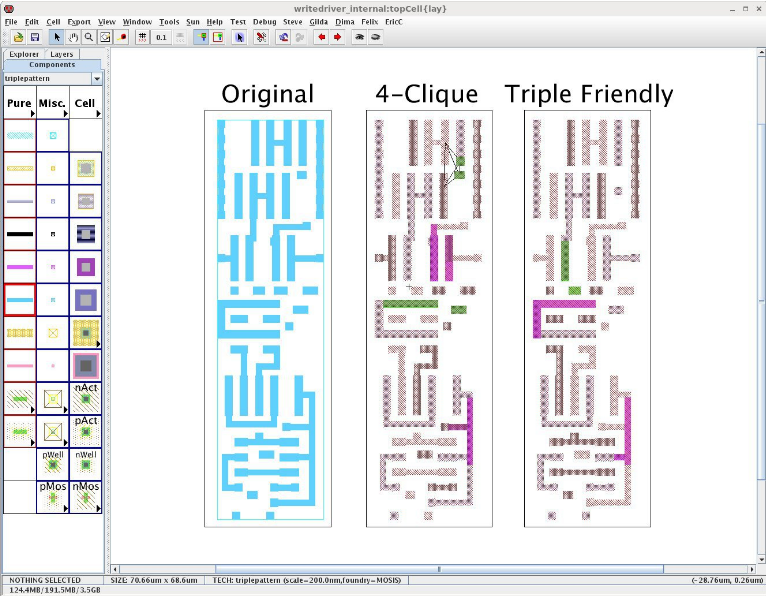
Introduction

New Challenges in Triple Patterning Lithography (TPL)

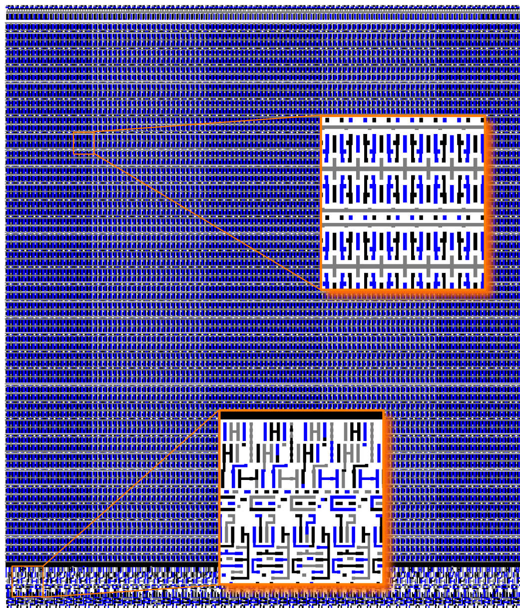
Layout Compliance Algorithms

Results and Conclusions

Interfaced with open source tool **Electric**

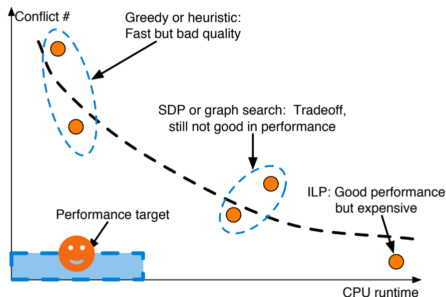


Layout Compliance Results



Conclusions

- First attempt for TPL layout compliance
- Faciliating the advancement of patterning technique



Future works

- Timing issue
- Smarter automatically layout modification

Thank You !