Detailed Placement In Advanced Technology Nodes: A Survey
(Invited Paper)

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***Abstract*—With the continued scaling to emerging technology nodes, modern circuit designs in nanometer era introduce many strict or even unprecedented design constraints and challenges. On one hand, conventional 193i wavelength lithography has pushed to its resolution limit, and the gap between manufacturing capability and design expectation becomes more critical. On the other hand, new metal layer (e.g. middle-of-line layers) as well as new device layer rules become more complex and restricted. We argue that detailed placement is the appropriate stage to consider the emerging manufacturing and design rule constraints. In this paper, we discuss sophisticated design constraints and challenges in emerging technology nodes, and survey the state-of-the-art detailed placement solutions and methodologies to overcome these challenges.**

I. Introduction

For more than two decades, standard cell based design has been a prevalent approach, where a standard cell library consists of pre-designed basic cells (units) and each cell is implemented with a particular logic function. In VLSI circuit design flow, placement determines locations of these cells and largely defines the overall interconnect quality. Due to the large problem sizes, placement consists of three major steps: global placement, legalization, and detailed placement [1]. Global placement determines the rough locations of cells optimizing objectives such as wirelength, timing, and routability, though the solution from global placement often contains overlap and thus is not design rule friendly [2]–[5]. Legalization removes cell overlaps and aligns cells to placement sites [6]–[9]. Finally, detailed placement further improves the solution by moving or swapping cells locally [10]–[13].

With the continued scaling to emerging technology nodes (e.g. sub-$10nm$), modern circuit designs in nanometer era introduce many strict or even unprecedented design constraints and challenges. On one hand, conventional 193i wavelength lithography has pushed to its resolution limit, and the gap between the manufacturing capability and the design expectation becomes considerably more critical [14]. On the other hand, new metal layer (e.g. middle-of-line layers) as well as new device layer rules become more complex and restricted. Due to the rapid development of technology node along with more and more complicated lithography constraints and design rules, consideration of these emerging challenges in early design stage has become a necessity.

We argue that **detailed placement** is the appropriate stage to consider the emerging manufacturing and design rule constraints. In global placement stage, due to the large problem size only an approximation of complex design constraints is integrated in the objective function. In legalization stage, the typical objective is to minimize the total displacement against global placement output. By contrast, in detailed placement manufacturing and design rule objectives can be transformed into cell abutting costs and more sophisticated models (e.g. timing) can be integrated, all of which can be optimized through local search in detailed placement engines.

In this paper, we discuss emerging constraints and challenges in nanometer circuit era, and survey the state-of-the-art detailed placement solutions and methodologies to overcome these challenges. The rest of the paper is organized as follows. Section II introduces detailed placement for lithography challenges. Section III elaborates the detailed placement to emerging design challenges, followed by conclusion in Section IV.

II. Detailed Placement for Lithography Compliance

In this section, we will discuss various constraints and corresponding solutions derived from lithography manufacturing process.

A. MPL aware Detailed Placement

With the increasing popularity of multiple patterning lithography (MPL), the placement problem related to MPL has been studied deeply, including double patterning lithography (DPL) [15]–[17], self-aligned double patterning (SADP) [18], and triple patterning lithography (TPL) [19]–[25]. To achieve DPL friendly layout, Gupta et al. [15] study the timing model for cell layouts and propose a dynamic programming based algorithm to solve coloring conflicts. To further improve DPL friendliness, a new DPL aware design flow is proposed including standard cell design, DPL aware placement, and DPL aware routing [16]. Gao et al. [18] solve decomposition conflicts for SADP at placement stage with cell flipping and spreading.

Yu et al. [19] propose a TPL friendly design flow, where standard cells are pre-colored with candidate coloring solutions and a look-up table (LUT) is constructed to store all the candidates. Although there might be large amount of coloring solutions for even a single cell, the number of pre-coloring solutions is limited due to the observation that only wire segments near cell boundary matter. Fig. 1 illustrates an example of conflict removal between two abutting cells, either by inserting whitespaces between two cells (see Fig. 1(b)) or by switching the coloring solutions (see Fig. 1(c)). A unified graph based algorithm is proposed to determine cell locations and coloring solutions simultaneously for a single row placement problem. In [23], Yu et al. further propose a linear dynamic programming, which can achieve good trade-off between runtime and performance. Kuang et al. [21] extend Yu's flow by predetermining coloring solution for each standard cell and try avoiding conflicts only by placement techniques. Chien et al. [24] also propose row based approaches to solve detailed placement and cell decomposition problems. Tian et al. [20] and Lin et al. [22] argue that cells of the same type should have the same color assignment for better timing variation. This additional constraint results in the $\mathcal{NP}$-completeness of the problem even for ordered single row version [22]. With further shrinking of feature sizes, middle-of-line (MOL) layers are introduced for local interconnection, which may involve new cell level design (e.g. [26]) and is also possible to cause cross-row conflicts. Very recently, Lin et al. [25] consider the detailed placement towards zero cross-row conflict from

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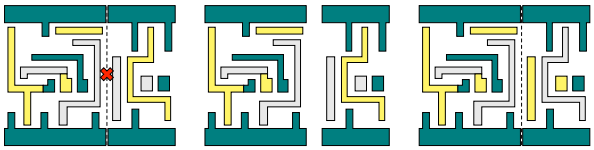


(a) (b) (c)

Fig. 1: (a) An example of TPL conflict; (b) Conflict removal by whitespace insertion; (c) Conflict removal by switching coloring solutions.

MOL layers, where the unified graph model is enhanced to consider local cell reordering. Note that the graph model in TPL placement can be naturally extended to consider most of other lithography or design rule constraints.

B. Other lithography aware placement

Extreme ultraviolet (EUV) lithography has a wavelength of 13.5nm which is able to achieve much higher resolution than conventional 193i lithography [27]. The small wavelength also leads to the difficulty in transmission and hence it requires reflective optical components and masks. However, there would be undesired scattered light, called *flare*, from those materials due to the roughness that causes critical dimension (CD) distortion and variation. Liu et al. [27] observe that it is better to have denser distribution of layout patterns in the central regions of a chip than that in the boundaries for flare reduction owing to the *flare periphery effect*. This is conflicting to the density uniformity requirement from the chemical mechanical polishing (CMP) in the manufacturing process [28]. They evaluate flare cost by a convolution model while CMP cost by variation and density gradient. The placement framework consists of non-linear global placement, legalization and detailed placement where the EUV flare- and CMP-awareness is incorporated as a part of cost functions to all stages. The detailed placement is based on a bipartite matching algorithm for independent cells (no connection between cells) followed by a local swapping for cells within each placement row.

Direct self-assembly (DSA) lithography has great potential to reduce the number of masks and improve critical dimension for contacts and vias. Contacts that are close to each other are printed in clusters with two steps [29]. A guiding pattern (GP) is patterned by optical lithography enveloping the contact cluster. Then GP is filled with block copolymers (BCPs) which spontaneously form separate contacts due to the forces between polymers and GP. Some cluster patterns are likely to result in poor quality of contacts, called *DSA defects*. Shim et al. [29] argue that cells abutting to each other within each placement row often result in large contact clusters that have higher probability to cause DSA defects. They identify the probability of DSA defects for various cluster patterns through repeated lithography- and DSA-simulations and perform post-placement optimization, such as cell flipping and local swapping in a row-by-row manner to minimize the probability of defects.

Multiple e-beam lithography (MEBL) improves the throughput of e-beam lithography (EBL) by massive parallel beam printing. In advanced nodes, MEBL is a promising candidate for small volume production or complementary layers. In MEBL, a layout is divided into stripes where each stripe is printed by one beam. It is observed that shape distortion occurs at the boundaries of stripes due to overlay and misalignment of beams, which is called stitch [30]. Vias and vertical lines turn out to be more susceptible to stitches than horizontal lines. Lin et al. [30] analyze the correlation between

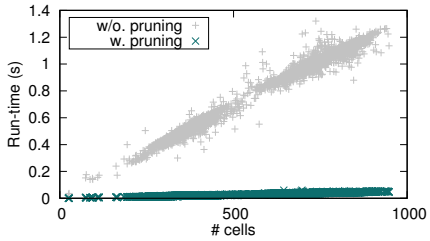


Fig. 2: Pruning speed-up proposed by [30], which can be naturally extended for different metrics, such as wirelength, routability, and congestion.

intra-cell routing and stitches at placement level; then a linear-time pruning technique in dynamic programming is proposed to minimize the impact of stitches as well as wirelength in a row-by-row manner. Fig. 2 compares the runtime difference between whether applying the new pruning technique or not, in which we can see that the linear-time pruning technique can provide around 30× speedup without any loss of optimality. Note that although the pruning technique is hard to be utilized in MPL aware detailed placement, it can be naturally embedded into conventional placement framework with different metrics (e.g., wirelength, routability, and congestion).

III. Detailed Placement for Emerging Constraints

In this section, we will explain various emerging design constraints, including drain-to-drain constraint, minimum implant area constraint, minimum jog length constraint for oxide diffusion, etc.

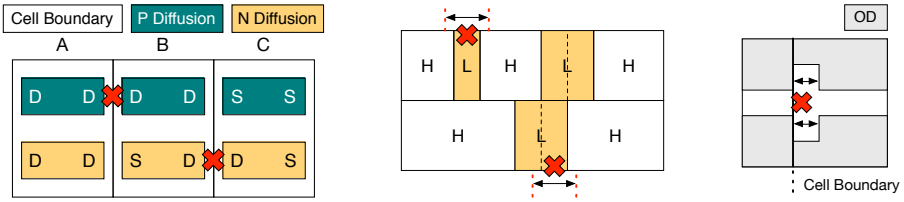
A. Drain-to-Drain Abutment Constraint

FinFET has been adopted as the main stream since $16nm$ and beyond due to its high control of short channel effects. However, fin degradation at left and right boundaries of a standard cell is observed from irregular fin stress and thus dummy gates are inserted to keep the uniformity of fin stress [31]. The gate and source of dummy transistors must be tied to power rails properly to be fully turned off for leakage issues, but such connections are not always available. Du et al. [32] identify the case where the drains of two adjacent cells facing each other cause the requirement of additional source nodes for power rail connection, which is called drain-to-drain (D2D) abutments, shown as Fig. 3(a). Then they propose a D2D abutment minimization problem on each placement row by swapping cells locally and solve by finding the shortest path in a graph model in which cells are allowed to swap with their left and right neighbors.

B. Minimum Implant Area Constraint

In modern manufacturing process, the regions for ion implantation must subject to a minimum area constraint as the lithography tools have limitation of resolutions. With the feature sizes shrinking to sub-$22nm$ and beyond, such minimum implant area constraint (MinIA) becomes critical due to the fact that layout geometries get tighter [33]. As the implant regions affect the threshold voltage of transistors, MinIA plays an important role in multi-V_t designs for leakage and performance control. In advanced technology nodes, some cells are too small to meet the MinIA rules such that they have to be grouped with other cells or filler cells of the same V_t. As a result, MinIA rules are likely to be violated for small cells or improper vertical alignment of cells, as shown in Fig. 3(b) where there are both intra-row violation and inter-row violation [34].

Kahng et al. [33] propose an iterative flow including MinIA aware placement and gate sizing to remove MinIA rule violations greedily



(a) (b) (c)

Fig. 3: Example of N10 FEOL rules such as (a) drain-to-drain (D2D) abutment rule and (b) minimum implant area (MinIA) rule and (c) minimum OD jog length (OW) rule.

while minimizing power subjecting to timing constraints. Lei et al. [35] try to remove MinIA rule violations by only placement perturbation and threshold voltage refinement in a row-by-row manner. They formulate an MILP for cells in a row to minimize weighted sum of power overhead and total cell displacement with timing and MinIA rules satisfied in the constraints. Tseng et al. [36] propose an approach to achieve MinIA compliance with pure placement techniques by moving and flipping cells. In their algorithm, violating cells are clustered with the same V_t cells where each cluster no longer has MinIA rule violations and fed to traditional detailed placement engine for wirelength minimization. However cells may exceed the original boundaries to resolve violations, by observing that the minimum spacings vary from cell boundaries, so a following-up step is performed to compress the layout by flipping cells.

C. Minimum Jog Length Constraint of Oxide Diffusion

In spite of the D2D abutment and MinIA rules, Kahng et al. [34] further identify a rule for minimum jog length of oxide diffusion (OD) starting from $10nm$ technology node. The minimum OD jog length (OW) constraint comes from different heights of OD between adjacent cells in which the length of OD jog has to be no smaller than a minimum value due to lithographic corner rounding and variability in device performance, shown as Fig. 3(c). OW rule violations can be fixed by inserting spacing between cells.

The set of rules for device layers (front end of line or FEOL) mentioned from Section III-A to III-C, become critical to placement in $10nm$ technology node and beyond, which is summarized as N10 FEOL rules [34]. Kahng et al. [34] argue that it is more feasible to correct all violations in a post-legalization phase than doing it in conventional placement. At the same time they come up with an MILP formulation for each small window of cells to address these N10 FEOL rules with an objective of minimizing total displacement, where speedup is achieved by massive parallelism between windows.

D. Multi-Row Height Detailed Placement

The number of tracks per row has seen a steady decrease with each new technology node, from 10 to 7.5 [37]. Previous methodology of designing standard cells that can be fit into single-row height becomes increasingly difficult for complex circuit components, such as flip-flops, muxes, etc., while satisfying performance and routing requirements. Thus designs in advanced technology nodes start to enable multi-row height standard cells for such complex circuit components. In addition, multi-bit flip-flops (MBFFs) or flop trays are becoming essential to power reduction and area compaction, which often introduces multi-row height cells in the design as well [38]–[40]. To further compress the design for area, power, and cost reduction, the layout density sometimes reaches up to 90%, resulting in the difficulty of resolving local routing congestion without proper detailed placement. Conventional legalization algorithms usually distribute cells into

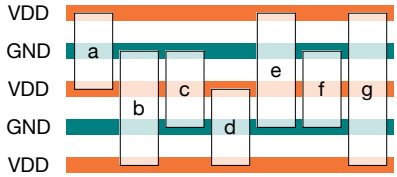


Fig. 4: Example of multiple-row height cells in a layout.

placement rows and perform row based algorithms to remove overlaps [7], [13], [41]. It becomes harder to legalize the placement due to the existence of multi-row height cells that breaks the independence of cells on individual rows. These emerging challenges make it critical for detailed placement and legalization to support multi-row height cells and produce overlap-free placement solutions with optimized wirelength and congestion.

The adoption of multi-row height cells introduces a special constraint in placement for power line alignment, shown as Fig. 4 where two cells take odd number of rows and five cells take even number of rows. Those cells taking even number of rows must be placed in alternative rows because they have VDD/GND rails on top and bottom, while GND/VDD rails in the middle. For example, the bottom of cell a has to align to rows with VDD rails at bottom, while the bottom of cell c must be aligned to rows with GND rails at bottom. But cells that occupy odd number of rows do not have such constraint since cell flipping is able to fix the alignment.

Dobre et al. [42] conduct the first study in the literature for the impacts of mixed cell-height designs at fine granularity level. They propose an implementation of mixing 12-track and 8-track cells with existing physical design flow that can achieve 25% area reduction or 20% better performance versus designs with 12-track cells only or 8-track cells only in their experiment. Designs are divided into two types of regions for 12-track and 8-track cells where each region only allows specific height of cells. Actually it is more practical to adopt cells that occupy integral number of rows such that they are more compatible to be placed in a layout.

In the perspective of placement algorithms, to deal with double-row height cells, Wu et al. [43] try to group two single-row height cells or extend a single-row height cell to double-row height, which unifies all the cell heights to double-row height for conventional detailed placement engines. As an elementary study on multi-row height cells, it is unable to consider various multi-row height and power rail alignment configurations. Chow et al. [44] propose the first legalization framework to minimize displacement for designs with general multi-row height cells. It removes overlaps by exploring the insertion points in the layout. Lin et al. [37] further propose a detailed placement framework to optimize wirelength and congestion with the existence of multi-row height cells, where they integrate the max prefix sum scheme into conventional global move algorithm and

also develop a nested dynamic programming algorithm to solve the placement of two rows of cells simultaneously.

IV. Conclusion

With the continued scaling of feature sizes, we have been confronted and will still see many unprecedented challenges, from various key aspects of manufacturing and design rule constraints. We argue that detailed placement, due to its capability of integrating sophisticated models, is the right stage to address these complex design constraints. In this paper, we have motivated and surveyed the state-of-the-art detailed placement solutions to overcome these design constraints and challenges. We hope this paper will stimulate more studies on detailed placement to address increasingly complex constraints in emerging technology nodes.

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