Standard Cell Layout Regularity and Pin Access Optimization Considering Middle-of-Line

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ABSTRACT

As minimum feature size and pitch spacing further decrease in advanced technology nodes, many new design constraints and challenges are introduced, such as regularity, middle of line (MOL) structures, and pin-access challenges. In this work, we propose a comprehensive study on standard cell layout regularity and pin access optimization. Given irregular cell layout from old technology nodes, our cell optimization tool can search unidirectional migrated result where the self-aligned double patterning (SADP) and MOL based design constraints are satisfied, and the pin-accessibility is optimized. This problem is formulated as a general integer linear programming (ILP), which may suffer from long runtime for some large standard cell cases. Therefore, we also develop a set of hybrid techniques to quickly search for high-quality solutions. The experimental results demonstrate the effectiveness of our approaches.

Categories and Subject Descriptors

B.7.2 [**Hardware, Integrated Circuit**]: Design Aids

Keywords

Standard Cell Design, Layout Regularity, Middle of Line, Self-Aligned Double Patterning, Pin Access

1. INTRODUCTION

As VLSI technology continues scaling down into advanced technology nodes, the semiconductor industry is greatly challenged by the printability and the design complexity issues. On the one hand, under the constraint of 193nm wavelength lithography, circuit designs are vulnerable to open/shorts, performance degradation, or even parametric yield loss. Although various resolution enhancement techniques are utilized, random geometrical configurations are still hard to implement due to lithography limitation [1]. Therefore, unidirectional layout styles have been proposed to improve the manufacturability and achieve manageable post-layout processing complexity [2, 3, 4]. On the other hand, the technology scaling also translates denser I/O pins to the standard cells, which may cause severe local congestion problem. That means if a standard cell is not properly designed, it cannot be easily accessed by physical design routing tool [5].

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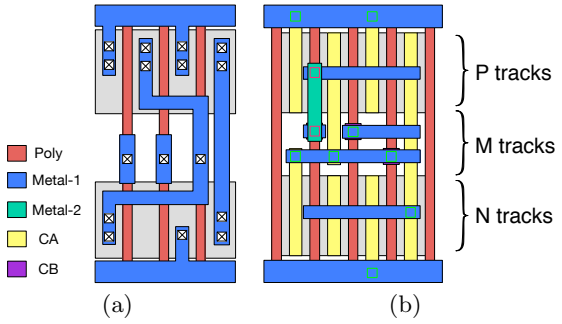


Figure 1: Example of cell regularity and pin access optimization. (a) The input layout with ten tracks. (b) The optimized layout with nine tracks.

To improve the regularity of standard cell, a Tungsten-based middle of line (MOL) structure is introduced to connect intra-cell transistors [6]. MOL structure is made up of two different local interconnection layers, CA and CB (sometimes called IM1 and IM2, respectively) [7]. In addition, MOL is able to achieve better manufacturability while paying little performance penalty [8]. Due to the regularity, both Metal-1 and MOL layers can be manufactured through self-aligned double patterning (SADP) technique [9], which has better overlap and line edge roughness control than multiple litho-etch based techniques [10, 11, 12]. Therefore, SADP with extreme unidirectional layout is a viable candidate for lower layer metallization at the 10nm technology node.

To overcome the local congestion problem, physical design tools should be aware of the congestion derived from the dense I/O pin cells. For instance, in placement stage local congestion mitigation can be applied to prevent placing hard-to-routed cells too close together [5]. Due to limited local routing resources and dense I/O pins, pin access is becoming a serious problem for detailed routing. More importantly, the standard cell library should be carefully designed to enhance the pin accessibility. That is, I/O pins need to be balanced distributed within a cell, as the alignment or the densely packing of pins make the cell more difficult to be accessed.

Based on these motivations, there has been growing interest in standard cell design toward regularity and pin access optimization. Tang and Yuan [13] studied the cell migra-

tion problem where the conventional shape-based layouts are transformed to simplified layouts with restrictive design rule constraints. There are some cell synthesis works for conventional 2D cells [14, 15], or 1D cells [16, 17, 18, 19]. Recently, an I/O pin extension approach was proposed to alleviate the pin access problem [20]. However, these existing studies suffer from one or more of the following issues. (1) Conventional layout migration or pin extension is with the assumption that the topologies of all pins and intra-cell wires are fixed, which limits the ability to resolve some very challenging cell designs. (2) When considering MOL structure, so far most of the cells are manually designed and there is no automatic flow to transform conventional 2D cell layout into unidirectional layout patterns. (3) Existing approaches may be ad hoc, thus there is very limited work providing a robust and generic flow to automatically optimize cell layout toward all the design metrics and requirements.

In this paper we study the problem of cell layout regularity and pin access optimization under MOL structure. Fig. 1 gives an example of our proposed cell optimization, where the input 2D cell in older technology node is shown in Fig. 1 (a), while the optimized unidirectional cell is in Fig. 1 (b). The MOL structure is utilized that CA connecting drain or source is parallel to gates, while CB is enabling connections between via0 to polys. Due to the unidirectional shapes of MOL and Metal-1 layers, the patterns are SADP friendly. That is, the line-space array decomposition can be applied to SADP with trim masks, with tight control on overlay and wafer-print artifacts. To the best of our knowledge, this is the first systematic work toward cell regularity and pin access optimization under MOL structure. Our contributions are highlighted as follows.

- We propose a general integer linear programming (ILP) formulation to solve the unidirectional cell optimization under MOL structure.
- We propose a set of hybrid techniques to search for high quality cell optimization solution.
- We have successfully migrated a set of library cells from the conventional 2D layout to the legal unidirectional layout while satisfying a set of gridded based design rules.
- Our framework is very generic that it can not only provide SADP friendly, but also be extended to consider other lithography techniques, e.g., LELE type double patterning.

The rest of this paper will be organized as follows. Section 2 gives the problem formulation. Section 3 proposes the details of unidirectional cell routing and pin access optimization algorithms. Section 4 presents the experimental results, followed by conclusion in Section 5.

2. PROBLEM FORMULATION

In this paper we utilize a regular cell layout that both polys and metal layers have fixed directions, i.e., Metal-1 has horizontal direction while poly and Metal-2 have vertical direction. Metal-1 connects to active areas of transistors through Via-0 and CA, while it connects to polys through Via-0 and CB. MOL is a contactless structure that makes routing denser. That is, CA-to-diffusion and CB-to-poly are directly

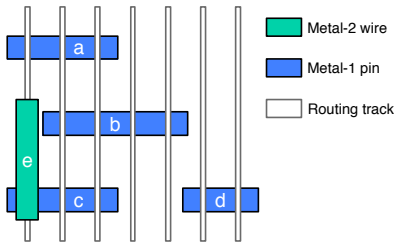


Figure 2: An example of pin access value calculation.

connected by shape overlap. CA strips can be extended in vertical direction to make power and ground connections to the transistors or to connect P transistors and N transistors together. All the Metal-1 and MOL wires must be compliant with a set of design rules [19, 20]. Since CA and Metal-1 are different layers, intersection of two perpendicular wire segments is allowed.

Metric 1 (Metal Wirelength). Wirelength is a good metric to evaluate the quality of standard cells. Performance and pin capacitance may be degraded due to longer wirelength. Therefore, a cell with shorter wirelength on metal layers is preferred.

Metric 2 (Pin Access Value). Optimized cell layout is required to provide flexible I/O pin access. Since most modern standard cell designs primarily use Metal-1 for local connections and I/O pins, Metal-1 wires present a new set of problems to standard cell I/O pin access. To evaluate pin accessibility of each pair of I/O pins, we define its corresponding pin access value as follows:

$$p(i,j) = h_i + h_j - \alpha \cdot o(i,j) \tag{1}$$

where h_i is the available routing track number on pin i, h_j is the available routing track number on pin j, $o(i,j)$ is the number of vertical routing tracks overlapping pin i and pin j simultaneously, and α is a parameter to evaluate the effect of the overlapping part to pin accessibility. Note that if one vertical track is occupied by a Metal-2 intra-cell wire, the available routing track number would be reduced by 1.

Pin access value in Eq. (1) is decided by two factors: the available length of the two pins and the overlapping track numbers. Longer pins have more routing tracks, which allows better flexibility for Via-1 position. However, if there are vertical routing tracks overlapping two pins, Metal-2 access to the overlap part is restricted. Thus we consider the overlapping issue in the pin access value calculation. A simple example is demonstrated in Fig. 2, where a, b, c and d are pins, and e is intra-cell Metal-2 wire. Due to the wire e, the available routing track number of c is 2. If α is set to 0.6, due to Eq. (1), $p(a,c) = 3.8$, $p(a,d) = 5, p(c,d) = 4$, $p(a,b) = 5.8$, and $p(b,d) = 6$. Note that Metal-2 pitch is not necessarily equal to the grid width.

For a standard cell, the total pin access value is calculated as follows:

$$PA = \sum_{i=1}^{m} \sum_{j>i}^{m} p(i,j) \tag{2}$$

where PA represents the total pin access value of all pin pairs in a standard cell, and m is the total pin number.

Based on above metrics, the **Unidirectional Routing with Pin Access Optimization (URPAO)** problem is defined as follows.

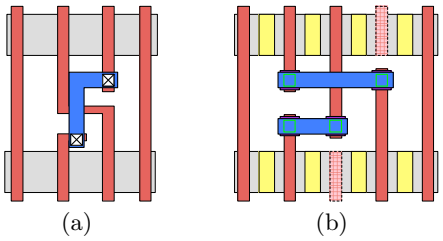


Figure 3: Dummy columns to resolve the native interconnect conflict.

Problem 1 (URPAO). *Given an original standard cell, a required total track number T and a maximum M track number T_m, URPAO problem seeks a unidirectional cell layout considering the MOL and SADP friendly. The objective is to minimize the cell wirelength, and maximize the pin access value PA.*

3. ALGORITHMS

In this section we detail our algorithms to solve the URPAO problem. Given an input cell layout, all the geometric information is parsed into a grid graph. Then ILP based approach and fast hybrid approach are proposed, respectively.

3.1 Dummy Column Insertion

In some complex standard cells such as DFF, there may be some cross-couple gate connection structures. As shown in Fig. 3 (a), one pair of polys is joined by bending Metal-1 wire, and another pair is merged into a single bent poly. Without modification, there will be no legal unidirectional routing solutions as their polys always overlap mutually. As illustrated in Fig. 3 (b), to resolve the cross-couple poly conflict, we insert a dummy poly column. The useless polys (shadow rectangles in Fig. 3 (b)) can be removed in final layout, or kept with floating for better lithography variation.

3.2 Grid Graph Construction

The geometric information of an input cell layout is parsed and stored in a grid graph. We use a coarse grain grid graph to indicate all the intra-cell interconnections. As illustrated in Fig. 4, polys are placed at regular intervals, and CA strips lie between these intervals. We use columns to represent them. Besides, as mentioned in Fig. 1, we divide routing area into three parts: P tracks, M tracks and N tracks. Utilizing grid graph effectively can simplify design rules. Since the SADP-specific parameters in [20] are much smaller than the grid width, the layout derived from the grid graph is SADP friendly intrinsically.

For a typical net, there are three types of terminals: poly gates, diffusion terminals on P transistors, and diffusion terminals on N transistors, which are denoted as M-terminals, P-terminals, and N-terminals, respectively. Besides, we distinguish power/ground nets from local interconnect nets. Since all power/ground nets only connect to power/ground rails located in the top or the bottom of the standard cell, we do not take them into consideration during cell routing stage.

3.3 M/P/N Track Number Negotiation

The input of URPAO problem specifies a total track number T and a maximum allowed M track number T_m. Under these specific track number constraints, our framework will automatically decide track numbers among M tracks, P tracks, and N tracks. The basic idea is that the M track number will be determined first, followed by the track numbers for P/N tracks. The segment length in M tracks of each intra-cell net will be estimated, then we can further estimate the required minimum M track number. The M track number for the cell is set to this number if it is smaller than T_m, otherwise is set to T_m. Once the middle track number is fixed, the P/N track numbers would be decided evenly.

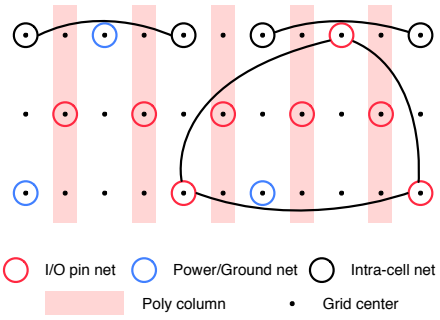


Figure 4: A grid graph example for AOI221_X1 Gate.

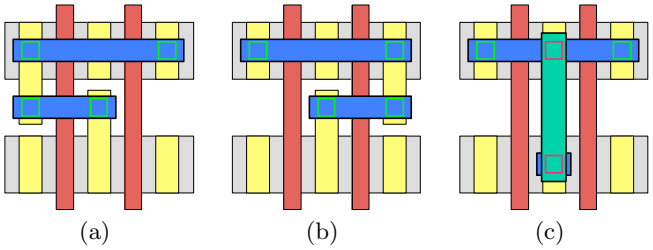


Figure 5: An example of P/N terminals connection for a net.(a), (b), and (c) are the three possible routes for the net with two P-terminals and one N-terminal.

3.4 ILP Based URPAO

In this subsection the URPAO problem is formulated as an integer linear programming (ILP). For each net we enumerate all its possible routing geometries, all of which will be considered in the ILP formulation.

3.4.1 Intra-Cell Net Topology Enumeration

We are given a standard cell with a set of intra-cell nets $N = \{n_1, n_2, \ldots, n_m\}$. If a net has P-terminals or N-terminals, its P-terminals are connected by a wire segment running on one of P tracks and its N-terminals are connected by a wire segment running on one of N tracks. Then we choose one P-terminal and one N-terminal respectively, and join them through a middle wire segment. Taking combination of P-terminals and N-terminals into consideration, there are many possible routes for a net. For instance, as shown in Fig. 5, three possible routes exist for the net. In addition, deciding which tracks to assign these horizontal wire segments adds some more possible routes. Note that sometimes the middle wire segment needs to extend to guarantee the connection between P-terminals and N-terminals. Improvement of I/O pin accessibility is another purpose to extend wire segments.

3.4.2 ILP Formulation

After intra-cell net topology enumeration, each net n_i constructs a set of routes R_i. For each $r_i^p \in R_i$, we introduce a

binary decision variable x_i^p such that x_i^p is 1 if the route r_i^p is selected for net n_i, otherwise route r_i^p is not selected.

In the ILP formulation, the objective function is to maximize

$$\beta \cdot PA - WL \tag{3}$$

where PA represents the total pin access value, WL represents the total wirelength of all the nets in the cell, and β is user specified parameter to assign the importance of pin access value. PA and WL are calculated as follows.

$$PA = \sum_{p_i,p_j \in N} \sum_{r_i^p \in R_i} \sum_{r_j^q \in R_j} p_{i,j}^{p,q} \cdot x_i^p \cdot x_j^q \tag{4}$$

$$WL = \sum_{n_i \in N} \sum_{r_i^p \in R_i} w_i^p \cdot x_i^p \tag{5}$$

Next, we describe the constraints for the ILP formulation. Since each net is assigned only to a route, we have constraint below

$$\sum_{r_i^p \in R_i} x_i^p = 1 \quad \forall n_i \in N \tag{6}$$

$$x_i^p \in \{0,1\} \quad \forall r_i^p \in R_i \ , \forall n_i \in N \tag{7}$$

Violation of design rules is modeled as conflicts between pair of routes as follows.

$$x_i^p + x_j^q \leq 1, \quad \text{if } r_i^p, r_j^q \text{ conflict} \tag{8}$$

which indicates that, to ensure the final layout satisfies correct electrical connection and specific design rules, two routes conflict with each other cannot be chosen at the same time. The rules to check whether there is any conflict between route r_i^p and route r_j^q are adapted from the 1-D gridded design rules in [19] and the SADP-specific design rules in [20].

Note that Eq. (4) is not linear equation, thus we introduce a new variable $x_{i,j}^{p,q}$ to replace $x_i^p \cdot x_j^q$ with the additional constraints:

$$\begin{cases} x_{i,j}^{p,q} \geq x_i^p + x_j^q - 1 \\ x_{i,j}^{p,q} \leq x_i^p, \quad x_{i,j}^{p,q} \leq x_j^q \\ x_{i,j}^{p,q} \in \{0,1\} \end{cases} \tag{9}$$

Similarly, we can rewrite Eq. (4) as

$$PA = \sum_{p_i,p_j \in N} \sum_{r_i^p \in R_i} \sum_{r_j^q \in R_j} w_{i,j}^{p,q} \cdot x_{i,j}^{p,q} \tag{10}$$

3.5 Fast URPAO with Hybrid Techniques

Although the 0-1 ILP formulation in the preceding section provides high-quality results, it may suffer from runtime overhead problem, especially for some cell cases with a large number of variables. In this section we propose a fast URPAO approach with hybrid techniques. The basic idea is that instead of search for optimal total metal wirelength and pin access value simultaneously, we divide the whole problem into two sub-problems. Firstly, each net is selected one basic topology through track assignment. Secondly, I/O pin extension is carried out to optimize the pin accessibility.

The details of the fast URPAO approach is summarized in Algorithm 1. Given the grid graph, we construct all horizontal wire segments of each net (line 1). We choose the middle wire segments with the shortest length. Therefore,

Algorithm 1 Fast URPAO

Input: Grid graph;

1: Generate all wire segments from nets N;
2: M track assignment using LP;
3: P/N track assignment using 2-SAT;
4: I/O pin extension using LP;
5: Transfer the wire segments to layout;

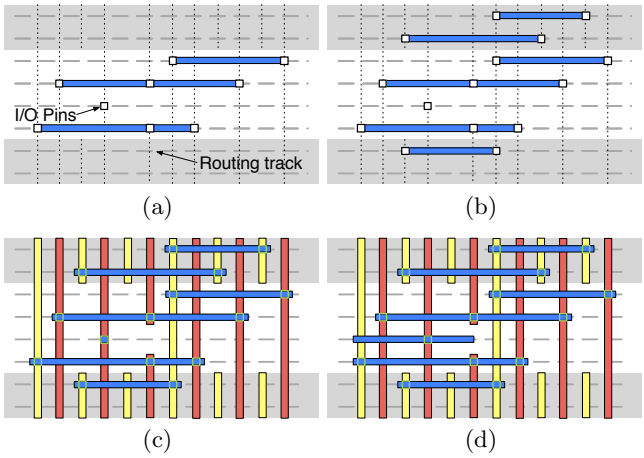


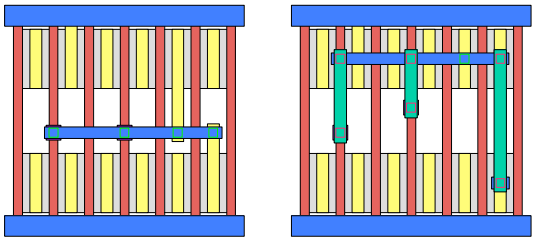
Figure 6: Example of fast URPAO approach, (a) M track assignment, (b) P/N track assignment, (c) Before pin extension, and (d) After pin extension.

sometimes P-terminal and N-terminal are directly connected through CA. After processing each net $n_i \in N$, we get a set of horizontal wire segments. The second step is M track assignment using linear programming (LP) (line 2), followed by track assignment for P/N tracks (line 3). After all wire segments are assigned to tracks, the I/O pin wire segments are extended to achieve better pin accessibility (lines 4). In the last step (line 5), we transfer the wire segments information into layout and dump out the final layout. Fig. 6 illustrates the corresponding steps of our URPAO approach.

3.5.1 LP Formulation for M Track Assignment

In MOL structure, some horizontal wire segments prefer to be assigned to M tracks, if they are connected to poly terminals (Fig. 7 (a)). In fast URPAO approach, given a set of horizontal segments, we identify those ones preferring on M tracks. However, since the M track number is limited, sometimes not all of them can be successfully assigned. If a segment connecting to poly terminal cannot be assigned to M tracks, additional Metal-2 wires are introduced to shift it to P/N tracks (Fig. 7 (b)). Besides, some poly grids are blocked due to connection to these Metal-2 wires, which are called block points. Since the M track assignment directly impact the intra-cell routability and the Metal-2 wirelength, we rely on an LP formulation to search for a reasonable assignment solution.

Let a variable x_i indicates whether the wire segment w_i is assigned to a M track. For each column c_i in the grid graph, there exist two sets $BLK(i)$ and $NET(i)$. If net n_j produces no block points when assigned to a P/N track, n_j is added to $NET(i)$ of the columns c_i which n_j overlaps when it is assigned to a M track. Otherwise, net n_j is added to set $BLK(i)$ of the columns c_i which n_j blocks when not assigned to a M



(a) (b)

Figure 7: (a) Assign the horizontal wire segment to a M track. (b) Additional Metal-2 wires when assign wire segment to a P/N track.

track. Based on the above definitions, the LP formulation is as follows.

$$\max \sum_i b_i \cdot x_i \tag{11}$$

$$\text{s.t.} \sum_{i \in NET(j)} x_i \leq T_m - |BLK(j)|, \quad \forall \text{ column } j \tag{12}$$

where b_i is the benefit of w_i when it is assigned to one of M tracks. $|BLK(j)|$ is the cardinality of set $BLK(j)$. After solving LP, selected wire segments are assigned to M tracks one-by-one according to the order. The sequence of wire segments is determined based on the LP solutions in descending order. That is, the wire segment with the biggest x_i is assigned first. After a segment is assigned, the capacity of the corresponding track is dynamically updated, and the next segment would be assigned to an available track which can accommodate this segment and has highest capacity.

3.5.2 2-SAT Formulation for P/N Track Assignment

Several wire segments may not be assigned during the M track assignment. Besides, there are some horizontal segments that only connects P-terminals or N-terminals. All these segments are assigned to P/N tracks. It is observed that certain pairs of wire segments have vertical constraints. For example, one segment w_i cannot be placed below another segment w_j. To consider these constraints during P/N track assignment, we define a binary variable x_i for each wire segment w_i. $x_i = 1$ if and only if the i-th segment is assigned to a P track, otherwise it is assigned into an N track. Then all vertical constraints are considered by a 2-SAT formulation.

$$\text{FALSE} = \bar{x}_i \cdot x_j \Leftrightarrow \text{TRUE} = (x_i + \bar{x}_j) \tag{13}$$

That is, the clause $(x_i + \bar{x}_j)$ is introduced into the 2-conjunctive normal form (CNF) formula. 2-SAT problem can be optimally solved in linear time [21] based on strongly connected component. The track type for each segment is set according to the topological order of each component. Then the similar algorithm in Section 3.5.1 is adopted to determine the detailed track for each wire segment.

3.5.3 LP Formulation for I/O Pin Extension

After all wire segments are assigned to the tracks, the next step is line end extension for pin wire segments. Here we denote PW as all the pin wire segments. Because we want to maximize the total amount of line end extensions, the objective function is defined in (14). Constraints (15) - (16) define the line end extension limits, while constraint (17) indicates the minimum wire length of each pin wire segment. For each pair of pin wire segments, the initial relative order in x-coordinate is determined. Suppose that pin wire segment w_i is on the left of pin wire segment w_j, constraint (18) is developed to prevent overlap of pairs of extended pins.

$$\max \sum_{i=1}^{m} (l_i^0 - l_i) + (r_i - r_i^0) \tag{14}$$

$$\text{s.t.} \quad c_L \leq l_i \leq l_i^0 \qquad \forall w_i \in PW \tag{15}$$

$$r_i^0 \leq r_i \leq c_R \qquad \forall w_i \in PW \tag{16}$$

$$r_i - l_i \geq l_0 \qquad \forall w_i \in PW \tag{17}$$

$$l_j - r_i \geq l_1 \qquad \forall w_i, w_j \in \text{same track} \tag{18}$$

We can simplify the objective function by omitting item l_i^0 and r_i^0, which are constants for the pin extension problem. It shall be noted that the dual problem of the line end extension is a min-cost flow problem [22]. But in our implementation the line end extension is formulated and solved through LP, as for standard cell level design problem the LP solver is fast enough.

4. EXPERIMENTAL RESULTS

The proposed standard cell routing algorithms are implemented in C++, and tested on a Linux machine with 3.3GHz CPU. The GUROBI solver [23] is used to generate the ILP/LP solutions. The experiments are carried out on Nangate $45nm$ standard cell library [24]. In our implementation the α value in (1) is set to 0.6, the β value in (3) is set to 0.02. Our cell routing framework is targeting at $10nm$ technology node with SADP process. The regular gridded based design rules [19] and SADP-specific design rules [20] are adapted in our work.

In Table 1 we compare two proposed algorithms for URPAO problem, where ILP based URPAO (Section 3.4) and fast URPAO with hybrid techniques (Section 3.5) are applied, respectively. Since the Nangate $45nm$ library consists of more than 130 standard cells, it is hard to list all the results. Therefore, ten typical standard cells are listed here. Columns "WL(nm)", "PA" and "CPU(s)" are the total metal wirelength, pin accessibility, and the cell routing runtime in seconds. We can see that although ILP based cell routing can achieve optimal solutions in theory, for some cells it suffers from long runtime overhead. Compared with expensive ILP based cell routing, our fast cell routing can achive more than 10000× speed-up. Besides, the fast method can get very comparable results, in terms of both wire-length and pin access values. That is, through fast cell routing the pin access value is 2% less, the wirelength is increased 0.7%.

5. CONCLUSION

In this paper, we propose a comprehensive study for the MOL based unidirectional cell layout regularity and pin access optimization. To the best of our knowledge, this work is so far the only one to automatically perform cell synthesis toward regularity, pin access optimization, and SADP friendly design. In addition, our framework is generic and flexible that it can be easily extended to consider other lithography techniques, e.g., LELE type patterning. As MOL structure ensures better regularity and better routability, we hope this paper will stimulate more future research into the automatic cell design for emerging technology nodes.

Table 1: Comparison of Two Cell Routing Approaches

Cell Name	Net#	T	ILP Based URPAO			Fast URPAO		
			WL(nm)	PA	CPU(s)	WL(nm)	PA	CPU(s)
XOR2_X2	5	9	3072	101.6	1.99	3072	101.6	0.14
		10	3072	101.6	8.05	3072	99.2	0.13
HA_X1	7	9	2448	91.2	0.55	2448	91.2	0.13
		10	2448	91.2	0.95	2448	91.2	0.14
MUX2_X1	6	9	1920	66.6	33.51	1920	66.6	0.11
		10	1920	66.6	242.99	1920	66.0	0.12
AND2_X1	4	9	864	21.0	1.57	864	21.0	0.13
		10	864	21.0	16.17	1008	23.4	0.12
AOI21_X1	5	9	960	38.4	22.30	960	38.4	0.13
		10	1104	42.0	57.51	1104	42.0	0.12
CLKGATE_X1	8	9	3552	30.0	3.60	3600	30.0	0.14
		10	3312	30.0	4.80	3312	30.0	0.11
DLL_X2	7	9	3120	29.4	76.09	3120	28.8	0.11
		10	2928	29.4	297.47	2928	28.8	0.11
DFFS_X1	12	9	8496	145.6	185.48	8880	149.0	0.13
		10	8064	145.6	520.69	8352	149.0	0.13
AOI221_X1	8	9	2208	181.2	>7202	2160	175.4	0.13
		10	2256	184.8	>7201	2160	177.2	0.12
NAND4_X1	5	9	1440	118.2	2087.63	1296	108.4	0.13
		10	1488	120.8	>7202	1296	109.6	0.12
avg.			2776.8	82.8	>1260	2796.0	81.3	0.12
ratio			**1.0**	**1.0**	**1.0**	**1.007**	**0.982**	**0.0001**

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