Multi-Voltage and Level-Shifter Assignment Driven Floorplanning

Bei Yu* , Sheqin Dong† and Satoshi GOTO‡

Abstract— As technology scales, low power design has become a significant requirement for SOC designers. Among the existing techniques, Multiple-Supply Voltage (MSV) is a popular and effective method to reduce both dynamic and static power. Besides, level shifters consume area and delay, and should be considered during floorplanning. In this paper, we present a new floorplanning system, called MVLSAF, to solve multi-voltage and level shifter assignment problem. We use a convex cost network flow algorithm to assign arbitrary number of legal working voltages and a minimum cost flow algorithm to handle level-shifter assignment. The experimental results show MVLSAF is effective.

Index Terms—Voltage-Island, Multi-Voltage Assignment, Level Shifter Assignment, Floorplanning

I. INTRODUCTION

As technology scales, low power design has become a significant requirement for system-on-chip designers. Many techniques were introduced to deal with power optimization. Among the existing techniques, Multiple-Supply Voltage (MSV) is one of the most effective methods for both dynamic and static power reduction while maintaining performance. In the MSV design, one of the most important problem is voltage assignment: timing critical modules are assigned to higher voltage while noncritical modules are assigned to lower voltage, so the power can be saved without degrading the overall circuit performance.

There are a number of previous works addressing voltage assignment in floorplanning. Among these works, voltage assignment is considered at various stages, including pre-floorplanning[4, 5]; during floorplanning[6, 7, 8, 9]; and post-floorplaning[10, 11, 12].

Level-shifter [1] has to be inserted to an interconnect when a lower voltage module drives a higher voltage module or a circuit may suffer from excessive short-circuit current energy. From [5, 9] we can observe that the number and the area of level shifters can not be ignored when modules increase. As a result, level-shifters may cause performance and area overhead, and should be considered during floorplanning. Accordingly, MSV aware floorplanning includes two major problems: voltage assignment and level shifter assignment, which make the design process much more complicated.

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Lee et al.[5] handle voltage assignment by dynamic programming, and level shifters are inserted as soft blocks. An approach based on ILP is used in [11] for voltage assignment at the post-floorplanning stage. To make use of physical information among modules during floorplanning, Ma et al.[8] transform voltage assignment problem into a convex cost network flow problem. However, their approach consider neither level-shifters' area overhead nor level-shifters' physical infomation.

Yu et al.[9] use a convex cost network flow algorithm to assign voltage and a minimum cost flow algorithm to handle level-shifter assignment which considers level-shifters' positions and areas. However, their work can only assign two legal working voltages. Besides, level shifters are assumed to be soft modules and ratios can not controlled well.

In this paper, we propose a new floorplanning system MVLSAF, which is extended from [9]. At floorplanning phase, we use: a convex cost network flow algorithm to assign multi-voltages; a minimum cost flow algorithm with more accurate model to assign level shifters.

The remainder of this paper is organized as follows. Section 2 defines the voltage-island driven floorplanning problem. Section 3 presents our algorithm flow. Section 4 reports our experimental results. At last, Section 5 concludes this paper.

II. PROBLEM FORMULATION

Definition 1 (DP-Curve)**.** *The power-delay trade-off of each module is represented by a DP-Curve* $\{(d_1, p_1), (d_2, p_2), \ldots, (d_k, p_k)\}$*, where each pair* (d_i, p_i) *is the corresponding delay and power consumption when module is operated at voltage* v_i *(Fig.1(a)).*

We assume that power is a convex function of delay when each point (d_i, p_i) is connected to its neighboring point(s) by a linear segment in the DP Curve. Besides, each level shifter has its own DP-Curve ((d_i, p_i) is delay and power consumption when it is driving voltage i). Lower voltage module needs bigger level shifter to drive other modules. Since bigger level shifter consumes more delay and power, we assume the level shifter's DP-Curve is also convex(as shown if Fig.1(b)). We extend the problem in [9] to Multi-Voltage and Level-Shifter Assignment driven Floorplanning (MVLSAF):

Problem 1. *(MVLSAF) We are given following input to generate floorplanning result: minimize the area, power cost and wirelength; satisfying timing constraint; insert all the level-shifters in need.*

1) *A set of modules, each module has its DP–curve.*
2) *A netlist* $\hat{G} = (\hat{V}, \hat{E})$ *and timing constraint* T_{cycle}*.*
3) *Level-shifter's area, ratio and DP-Curve.*
4) *Number of legal working voltage* k*.*

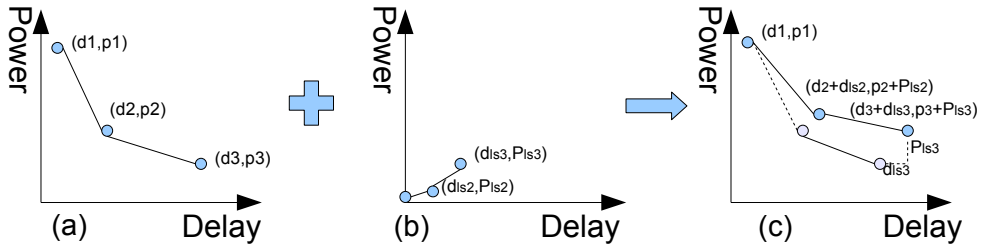

Fig. 1. Delay Power Curve of (a)module with three legal voltages; (b)corresponding level shifter. (c)modified DP-Curve of module.

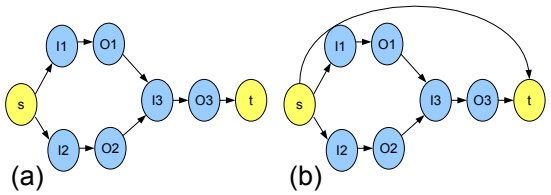

Fig. 2. (a)$\bar{G} = \{\bar{V}, \bar{E}\}$, after adding nodes s, t and diving nodes N_i into I_i and O_i (b)Transformed $\bar{G} = \{V, E\}$ by adding edge $e(\bar{s}, \bar{t})$ to remove constraint $\mu_t - \mu_s \leq T_{cycle}$ in equation (1).

III. ALGORITHM of MVLSAF

Our work is similar to that presented in [9], in which a two phases framework is presented to deal with voltages and level-shifters assignment during floorplanning. However, our approach differs from [9] in the following ways: during voltage assignment, we support arbitrary number of legal voltages allowing further power reductions in certain applications; during level-shifter assignment, we adopt more accurate model to calculate possible level-shifter number in white space, which control level shifter under certain H/W ratio.

A. Multi-Voltages Assignment

To take consumption of level-shifter into consider, for each module, we modify its DP-Curve: replace each pair (d_i, p_i) by $(d_i + d^i_{ls}, p_i + p^i_{ls})$, where (d^i_{ls}, p^i_{ls}) islevel shifter's delay and power consumption. Modified DP-Curve is shown in Fig.1(c).

LEMMA 1. *$f(x)$ is convex $\iff$ $f(x_1 + x_2) < \frac{f(x_1)+f(x_2)}{2}$, $\forall x_1, x_2 \in Z$.*

LEMMA 2. *If $f(x)$ and $g(x)$ are convex, then $P(x) = f(x) + g(x)$ is also convex.*

THEOREM 1. *Modified DP-Curve is piecewise linear convex function with integer breakpoints, and we can apply convex cost flow algorithm to solve voltage assignment problem[3].*

Given netlist $\hat{G}$, we translate it into $\bar{G} = (\bar{V}, \bar{E})$(adding start node s and end node t, dividing each node $n_i \in \hat{G}$ into 2 nodes I_i and O_i, as shown in Fig.2(a)). So $\bar{V} = \{s, t, I_1, O_1, I_2, O_2, \ldots, I_m, O_m\}$. And I_i is connected to O_i by a directed edge. We denote these new created edges $\{e(I_i, O_i) | I_i, O_i \in \bar{V}\}$ as $\bar{E}_1$, denote edges $\{e(s, I_k) | I_k \in \bar{V}\}$ as $\bar{E}_3$, and other edges as $\bar{E}_2$, and $\bar{E} = \bar{E}_1 \cup \bar{E}_2 \cup \bar{E}_3$.

The mathematical program of voltage assignment is in (1),where d_{ij} is delay from node i to node j.

$$Minimize \sum_{e(i,j)\in\bar{E}} P_{ij}(d_{ij}) \tag{1}$$

$$s.t. \begin{cases} \mu_j - \mu_i \geq d_{ij} & \forall e(i,j) \in \bar{E} \quad (1a) \\ \mu_t - \mu_s \leq T_{cycle} & \quad (1b) \\ d_{ij} \in \{d^1_{ij}, d^2_{ij}, \ldots, d^k_{ij}\} & \forall e(i,j) \in \bar{E}_1 \quad (1c) \\ d_{ij} = delay_{ij} & \forall e(i,j) \in \bar{E}_2 \quad (1d) \\ d_{ij} = 0 & \forall e(i,j) \in \bar{E}_3 \quad (1e) \end{cases}$$

We can incorporate constraints $(1b)$ and $(1a)$ by transforming $(1b)$ into $\mu_s - \mu_t \geq -T_{cycle}$, and define d_{st}, s.t. $\mu_t - \mu_s = d_{st}$ & $d_{st} \leq T_{cycle}$. Accordingly, $\bar{E}_3 = \{\bar{E}_3 \cup e(s,t)\}$, and the transformed DAG $\bar{G}$ is shown in Fig.2(b). Besides, we dualize the constraints $(1a)$ using a nonnegative Lagrangian multiplier vector $\bar{x}$, obtaining the following Lagrangian subproblem:

$$L(\vec{x}) = \min \sum_{e(i,j)\in\bar{E}} [P_{ij}(d_{ij}) + x_{ij} d_{ij}] \tag{2}$$

We define function $H_{ij}(x_{ij})$ for each $e(i,j) \in E$ as follows:

$$H_{ij}(x_{ij}) = \min_{d_{ij}} \{P_{ij}(d_{ij}) + x_{ij} d_{ij}\} \tag{3}$$

THEOREM 2. *The function $H_{ij}(x_{ij})$ is a piecewise linear concave function of x_{ij}, and $\forall e(i,j) \in E_1$, $H_{ij}(x_{ij})$ is described in the following manner:*

$$H_{ij}(x_{ij}) = \begin{cases} P_{ij}(d^k_{ij}) + d^k_{ij} x_{ij} & 0 \leq x_{ij} \leq b_{ij}(k) \\ \ldots \\ P_{ij}(d^q_{ij}) + d^q_{ij} x_{ij} & 0 \leq x_{ij} \leq b_{ij}(q) \\ \ldots \\ P_{ij}(d^1_{ij}) + d^1_{ij} x_{ij} & k \leq x_{ij} \end{cases} \tag{4}$$

where $b_{ij}(q) = \frac{P_{ij}(d^{q-1}_{ij}) - P_{ij}(d^q_{ij})}{d^q_{ij} - d^{q-1}_{ij}}$.

To transform the problem into a minimum cost flow problem, we construct an expanded network $G' = (V', E')$. There are three kinds of edges to consider:

- $e(i,j)$ in E1:we introduce k edges in G', and the costs of these edges are: $-d^k_{ij}, -d^{k-1}_{ij}, \ldots - d^1_{ij}$; upper capacities: $b_{ij}(k), b_{ij}(k-1) - b_{ij}(k), b_{ij}(k-2) - b_{ij}(k-1), \ldots M - b_{ij}(2)$, where M is a huge confficient; lower capacities are both 0.

TABLE I
NOTATION USED IN LS ASSIGNMENT

r_j	Room containing module j
R	Set of rooms, $R = \{r_1, r_2, \ldots, r_m\}$
LS	Set of LSs, $LS = \{ls_1, ls_2, \ldots, ls_n\}$
$p_{jk}, k = 1, 2, 3$	Three parts of white spaces in r_j.

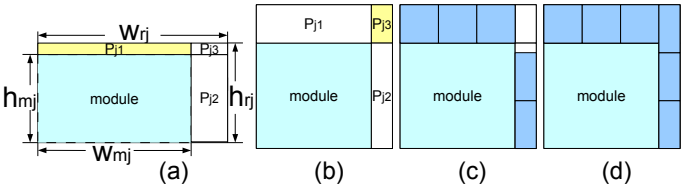

Fig. 3. (a)Area of p_{j1} is bigger than area of level shifter but is too narrow to insert. (b)p_{j3} can merge with either p_{j1} or p_{j2}. (c)If p_{j3} merges with p_{j1}, can insert only 5 level shifters. (d)If p_{j3} merges with p_{j2}, can insert totally 6 level shifters.

- $e(i, j)$ in E2: cost, lower and upper capacity is $-d_{ij}$, 0, M.
- Edge in E3: two edges are introduced in G', one with cost, lower and upper capacity as $(-K_j, -M, 0)$, another is $(0, 0, M)$.

Using the cost-scaling algorithm, we can solve the minimum cost flow problem in G'. For the residual network $G(x^*)$ and solve a shortest path problem to determine shortest path distance $d(i)$ from node s to every other node. By implying that $\mu(i) = d(i)$ and $d_{ij} = \mu(i) - \mu(j)$ for each $e(i, j) \in E_1$, we can finally solve voltage assignment problem.

B. Level-shifters Assignment

After voltage assignment, each module is assigned a voltage, then the number of level shifters n is determined. In level shifter assignment we carry out minimum cost flow algorithm to try to assign every level-shifters one room. Compared with [9], we present a more accurate model estimating possible number of level shifters in white space to avoid too much ratio.

We construct a network graph $G^* = (V^*, E^*)$, and then use a min-cost max-flow algorithm to determine which room each level shifter belong to.

- $V^* = \{s, t\} \cup LS \cup R$.
- $E^* = \{(s, ls_i) | ls_i \in LS\} \cup \{(ls_i, r_j) | \forall fr_{ij} = 1\} \cup \{(r_j, t) | r_j \in R\}$.
- Capacities: $C(s, ls_i) = C(ls_i, r_j) = 1, C(r_j, t) = NumLS(j)$.
- Cost: $F(s, ls_i) = 0, F(r_j, t) = 0; F(ls_i, r_j) = F_{ij}$.

where $fr_{ij} = \begin{cases} 1, & \text{if } ls_i \text{ can be inserted into } r_j \\ 0, & \text{others} \end{cases}$ and F_{ij} can refer to [9].

The algorithm of $NumLS(i)$, which accurately estimates number of possible level shifters in white space, is shown in Algorithm 1. In room r_j, white space is split into at most three parts: p_{j1}, p_{j2}, p_{j3}(as shown in Fig.3).

Algorithm 1 NumLS(i)

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1: Initialize p_{i1}, p_{i2}, p_{i3};
2: a_{ls} ← area of level shifter;
3: if p_{i1} is too narrow then
4:    areaof(p_{i1}) ← 0;
5: end if
6: if p_{i2} is too narrow then
7:    areaof(p_{i2}) ← 0;
8: end if
9: if areaof(p_{i1}) % a_{ls} > areaof(p_{i2}) % a_{ls} then
10:   p_{i1} ← p_{i1} ∪ p_{i3};
11: else
12:   p_{i2} ← p_{i2} ∪ p_{i3};
13: end if
14: return ⌊areaof(p_{i1}) / a_{ls}⌋ + ⌊areaof(p_{i2}) / a_{ls}⌋;
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It can be shown that any flow in the network G^* assigns level shifters to white spaces. The minimum cost flow algorithm can be run in polynomial time[3].

After level-shifter assignment, level shifters that can not be assigned to any room are belong to set ELS. We use heuristic method to assign level shifters in ELS, so more level shifters in ELS, more ILO(Interconnect Length Overhead[9]). If white space ws_i is too narrow, then level shifters being assigned to ws_i are all belong to ELS. More accurate model we used (Algorithm 1) can reduce the number of level shifters in ELS and then reduces ILO.

IV. EXPERIMENTAL RESULTS

We implemented algorithm MVLSAF in the C++ programming language and executed on a Linux machine with a 3.0GHz CPU and 1GB Memory. Fig. 4 shows the experimental results of the benchmarks n50 and n100.

We use CBL[2] to represent every floorplan generated. Besides, all the multi-pin nets are decomposed into a set of source-sink two-pin nets. Cost function in floorplanning is: $\Phi = \lambda_A A + \lambda_W W + \lambda_P P + \lambda_R R + \lambda_N N$, where A and W represent the floorplan area and wire length; P represents the total power consumption; R represents the power network resource; and N records the number of level shifters that can not be assigned.

The previous work [9] is the recent one in handling floorplanning problem considering voltage and level-shifter assignment. We performed our algorithm MVLSAF and VLSAF in [9] on the same test circuits, which are based on the GSRC benchmarks adding power and delay specifications. For each test circuit, we set k as 4, and run MVLSAF and VLSAF 5 times. Table II lists the average results. The column Power Cost means the actual power consumption. When allowing four legal working voltages, MVLSAF can save 8.5% power while not deteriorating wirelength, dead space and run time. The column ILO and the column LS Number show that using more accurate model in level shifter assignment, even level shifters number increases 18.6% ILO does not increase.

TABLE II
THE COMPARISON BETWEEN THE VLSAF AND THE PREVIOUS WORK [9]

Data	Power Cost		Wire Length w. LS		LS Number		ILO(%)		White Space(%)		Run Time(s)	
	[9]	MVLSAF	[9]	MVLSAF	[9]	MVLSAF	[9]	MVLSAF	[9]	MVLSAF	[9]	MVLSAF
n10	189142	162794	15504	16474	9	11	0.37	0.12	10.96	11.54	3.36	3.96
n30	146483	138463	43265	45388	25	42	0.07	0.21	14.28	17.63	21.0	19.83
n50	143596	133564	94622	93296	114	151	0.28	0.50	22.63	22.95	41.37	49.35
n100	135607	120885	185382	181280	153	167	0.49	0.34	27.05	26.07	436.65	414.7
n200	129615	117538	349562	344111	203	248	0.44	0.46	36.35	34.84	1980.4	2036.4
n300	216554	206354	552616	568364	366	417	0.49	0.53	37.73	38.54	2384.3	2377.2
Avg	160166	146599	206825	208152	145	172	0.36	0.36	24.83	25.26	811.2	816.8
Diff	-	-8.5%	-	+0.6%	-	+18.6%	-	± 0%	-	+1.7%	-	+0.7%

TABLE III
EXPERIMENTAL RESULTS WITH MORE LEGAL WORKING VOLTAGE

Data	k	Power Cost	Wire Length	LS Num	ILO (%)	Dead Space(%)	Run Time(s)	Data	k	Power Cost	Wire Length	LS Num	ILO (%)	Dead Space(%)	Run Time(s)
n10	2	189142	15341	9	0.10	10.21	3.05	n100	2	133775	178685	122	0.17	26.45	431.7
	3	163352	16386	10	0.13	11.58	3.03		3	131394	180023	150	0.50	26.8	438.05
	4	162794	16474	11	0.12	11.54	3.96		4	120885	181280	167	0.34	26.07	414.7
n30	2	146483	42591	25	0.1	15.0	21.5	n200	2	127044	344010	204	0.42	35.64	1955.8
	3	139466	45103	42	0.32	15.85	20.82		3	112801	331627	242	0.55	35.44	1949.4
	4	138463	45388	42	0.21	17.63	19.83		4	117538	344111	248	0.46	34.84	2036.4
n50	2	144489	93459	104	0.25	22.05	49.21	n300	2	223574	548502	321	0.23	37.88	2363.9
	3	132199	94105	130	0.37	22.72	51.10		3	218636	556718	389	0.44	37.14	2390.2
	4	133564	93296	151	0.50	22.95	49.35		4	206354	568364	417	0.53	38.54	2377.2

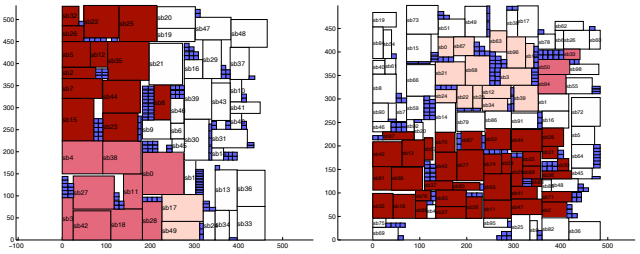

Fig. 4. Experimental results of n50 and n100. Four legal working voltages. Modules in the same voltage are nearly clustered together to reduce the power-network resource, and level shifters (small dark blocks) are inserted in white spaces.

In order to demonstrate the effectiveness of our approach, we have done three sets of experiments in which the number of legal working voltage for each module is set two, three and four. The detailed results are listed in Table III.

V. CONCLUSIONS

We have extended framework in [9] to solve multi-voltage and level shifter assignment problem: a convex cost network flow algorithm to assign arbitrary number of legal working voltages; a minimum cost flow algorithm to handle level shifter assignment. Experimental results have shown that our framework is effective in reducing power cost while considering level shifters' positions and areas.

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