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Best Paper Award

Best Paper Award 2022

DeePattern: Layout Pattern Generation with Transforming Convolutional Auto-Encoder
(https://ieeexplore.ieee.org/document/9665719)

Authors: Haoyu Yang, Shuhe Li, Wen Chen, Piyush Pathak, Frank Gennari, Ya-Chieh Lai, and Bei Yu

Honorable Mention Award 2022

Integrated Test Pattern Extraction and Generation for Accurate Lithography Modeling
(https://ieeexplore.ieee.org/document/9800926)

Authors: Gangmin Cho, Yonghwi Kwon, Pervaiz Kareem and Youngsoo Shin

ℓ_1 Trend Filtering-Based Change Point Detection for Pumping Line Balance of Deposition Equipment
(https://ieeexplore.ieee.org/document/9650548)

Authors: Jeongsun Ahn, Duyeon Kim, Mingi Song, Jaehong Min, Jimin Hwang, Juhye Kwon, and Hyun-Jung Kim

Practical Q-learning-based route-guidance and vehicle assignment for OHT systems in semiconductor fabs
(https://ieeexplore.ieee.org/document/9759491)

Authors: Sangpyo Hong, llhoe Hwang, and Young Jae Jang

Best Paper Award 2022 Editorial

The IEEE Transactions on Semiconductor Manufacturing congratulates Haoyu Yang, Shuhe Li, Wen Chen, Piyush Pathak, Frank Gennari, Ya-Chieh Lai, and Bei Yu whose paper "DeePattern: Layout Pattern Generation with Transforming Convolutional Auto-Encoder" (Vol. 35, No.1, February 2022) was selected as the Best Paper for 2022 by a team of Associate Editors. This paper proposes generative machine learning models to synthesize VLSI layouts through a pattern generation framework that reduces the challenging creation problem into two simpler subproblems with the aid of an efficient squish pattern representation. The problem is treated by designing an innovative transforming convolutional auto-encoder in TCAE architecture, aiming to generate efficient and representative pattern shapes. The paper introduces a GAN-guided TCAE ML analysis that targets massive DRC-clean and content-specific pattern generation following certain design rules, without losing pattern library diversity. Through experiments on 7nm EUV designs, the authors demonstrate that each latent vector node in TCAE has a real physical meaning in layout domain and transformations on latent vectors can produce additional topologies of interest. Results show that the generated pattern library exhibits larger pattern number and pattern diversity compared to the traditional state-of-the-art industry layout generator. Three other papers were recognized with an Honorable Mention:

a) "Integrated Test Pattern Extraction and Generation for Accurate Lithography Modeling" by Gangmin Cho, Yonghwi Kwon, Pervaiz Kareem and Youngsoo Shin (Vol.35, N0. 3, August 2022)

b) "L1 Trend Filtering-based Change Point Detection for Pumping Line Balance of Deposition Equipment" by Jeongsun Ahn, Duyeon Kim, Mingi Song, Jaehong Min, Jimin Hwang, Juhye Kwon, and Hyun-Jung Kim, (Vol.35, No. 1, February 2022)

c) "Practical Q-learning-based route-guidance and vehicle assignment for OHT systems in semiconductor fabs", by Sangpyo Hong, Ilhoe Hwang, and Young Jae Jang (Vol. 35, N0. 3, August 2023)

The Editorial Board of IEEE Transactions on Semiconductor Manufacturing Journal continues to explore innovative all of semiconductor manufacturing with special attention to design, modeling and process control aspects. The entire editorial team for IEEE TRANSACTIONS ON SEMICONDUCTOR MANUFACTURING welcomes authors to submit their papers for review. We also encourage all authors and readers to participate in the manuscript review process. The 2022 Best Paper selection team consisted of Dr. Chia-Yen Lee, Dr. Lars Monch and Dr. Mircea Dusa

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