THE CHINESE UNIVERSITY OF HONG KONG
Print Course Catalog Details

Academic Org: Dept of Computer Sci & Engg – Subject: Computer Engineering

Course: CENG4120 **Course ID:** 012811 **Eff Date:** 2022-07-01 **Crse Status: Active** **Apprv. Status:** Approved **[**Course Rev**]**

Computer-aided Design for Very Large Scale Integrated Circuits **超大規模集成電路的計算機輔助設計**

This course aims at providing students basic knowledge and background on VLSI CAD. The course will cover various topics on automation across the design of a VLSI circuit including but not limited to, Boolean matching, logic optimization, chip planning, placement, routing, interconnect optimization, testing and manufacturing. Students will learn to use some EDA tools and also develop some algorithms to solve EDA problems.

本科旨在賦予學生VLSI（超大規模集成）CAD（計算機輔助設計）的基本知識和背景。本科會覆蓋VLSI電路設計過程的自動化話題，包括但不限於：布爾匹配、邏輯優化、芯片規劃、布局、布線、互聯優化、測試和製造。學生將學習一些EDA（電子設計自動化）工具，並且開發一些解決EDA問題的算法。

Grade Descriptor:

A

EXCELLENT – exceptionally good performance and far exceeding expectation in all or most of the course learning outcomes; demonstration of superior understanding of the subject matter, the ability to analyze problems and apply extensive knowledge, and skillful use of concepts and materials to derive proper solutions.

有關等級說明的資料，請參閱英文版本。

B

GOOD – good performance in all course learning outcomes and exceeding expectation in some of them; demonstration of good understanding of the subject matter and the ability to use proper concepts and materials to solve most of the problems encountered.

有關等級說明的資料，請參閱英文版本。

C

FAIR – adequate performance and meeting expectation in all course learning outcomes; demonstration of adequate understanding of the subject matter and the ability to solve simple problems.

有關等級說明的資料，請參閱英文版本。

D

MARGINAL – performance barely meets the expectation in the essential course learning outcomes; demonstration of partial understanding of the subject matter and the ability to solve simple problems.

有關等級說明的資料，請參閱英文版本。

F

FAILURE – performance does not meet the expectation in the essential course learning outcomes; demonstration of serious deficiencies and the need to retake the course.

有關等級說明的資料，請參閱英文版本。

Equivalent Offering:
Units: 3 (Min) / 3 (Max) / 3 (Acad Progress)
Grading Basis: Graded
Repeat for Credit: N
Multiple Enroll: N
Course Attributes:

Topics:

COURSE OUTCOMES

Learning Outcomes:

At the end of the course of studies, students will have acquired the ability to
1. Use some EDA tools from vendors like Cadence and Synopsys.
2. Understand the objectives and constraints in different stages of an EDA flow.
3. Understand the basic methodologies and algorithms to solve problems in different stages of an EDA flow.
4. Innovate and develop some new methods in solving EDA problems.
5. Know and appreciate the new developments in the EDA industry.

Course Syllabus:

This course aims at providing students basic knowledge and background on VLSI CAD. The course will cover various topics on automation across the design of a VLSI circuit including but not limited to, Boolean matching, logic optimization, chip planning, placement, routing, interconnect optimization, testing and manufacturing. Students will learn to use some EDA tools and also develop some algorithms to solve EDA problems.

Assessment Type:

Essay test or exam	: 40%
Homework or assignment	: 20%
Lab reports	: 10%
Presentation	: 10%
Short answer test or exam	: 20%

Feedback for Evaluation:

1. Quiz and examinations
2. Course evaluation and questionnaire
3. Question-and-answer sessions during class
4. Student consultation during office hours or online

Required Readings:

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Recommended Readings:

1. "VLSI Physical Design: From Graph Partitioning to Timing Closure" by A.B. Kahng, J. Lienig, I.L. Markov and J. Hu. (Publisher: Springer)
2. "Practical Problems in VLSI Physical Design Automation" by Sung Kyu Lim, (Publisher: Springer)
3. "VHDL for Logic Synthesis", Andrew Rushton, 3rd. Ed. (Publisher: Wiley)
4. "CMOS VLSI Design - A Circuits and Systems Perspective" by Neil H.E., Weste and D. Harris 3rd. Ed. (Publisher: Addison-Wesley)

OFFERINGS

1. CENG4120 — Acad Organization=CSD; Acad Career=UG

COMPONENTS

LEC : Size=30; Final Exam=Y; Contact=3
TUT : Size=30; Final Exam=N; Contact=1

ENROLMENT REQUIREMENTS

1. CENG4120

Enrollment Requirement Group:
Prerequisite: CSCI2100 or CSCI2520 or ESTR2102

New Enrollment Requirement(s):
Pre-requisite = no change

CAF

eLearning hrs for blended cls 0
No. of micro-modules 0

Research components (UG) 0%

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