Lecture 11: Virtual Memory & Performance

Name: _____

ID: _____

TLB Event Combinations

- TLB / Cache miss: page / block not in “cache”
- Page Table miss: page NOT in memory

TLB	Page Table	Cache	Possible? Under what circumstances?
Hit	Hit	Hit	
Hit	Hit	Miss	
Miss	Hit	Hit	
Miss	Hit	Miss	
Miss	Miss	Miss	
Hit	Miss	Miss / Hit	
Miss	Miss	Hit	

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Hit	Hit	Miss	Yes – although page table is not checked if TLB hits
Miss	Hit	Hit	Yes – TLB miss, PA in page table
Miss	Hit	Miss	Yes – TLB miss, PA in page table but data not in cache
Miss	Miss	Miss	Yes – page fault
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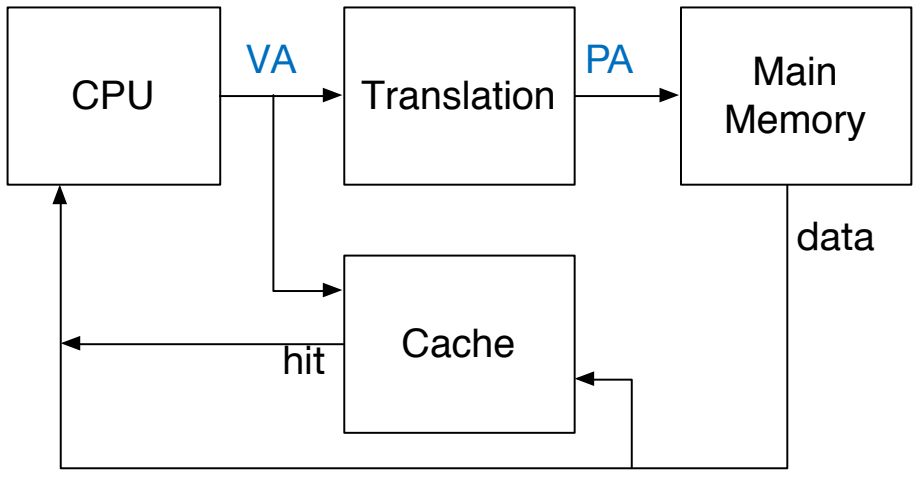
Miss	Miss	Miss	Yes – page fault
Hit	Miss	Miss / Hit	Impossible – TLB translation not possible if page is not in memory
Miss	Miss	Hit	Impossible – data not allowd in cache if page is not in memory

QUESTION: Why Not a Virtually Addressed Cache?

- Access Cache using virtual address (VA)
- Only address translation when cache misses



Answer:

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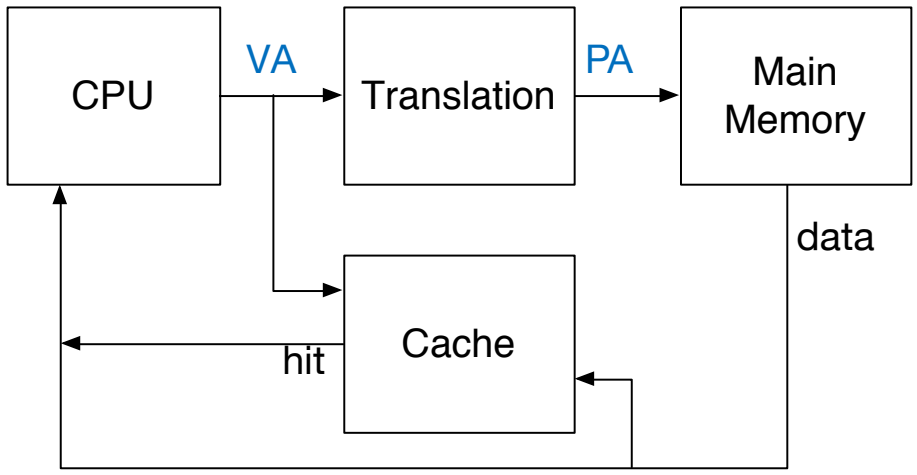

Answer:

- aliasing: 2 programs may share data w. different VAs for the same PA
- Coherence issues: must update all cache entries with same PAs

Question: Memory Access Time Example

- Assume 8 cycles to read a single memory word;
- 15 cycles to load a 8-word block from main memory (previous example);
- cache access time = 1 cycle
- For every **100** instructions, statistically **30** instructions are data read/ write
- Instruction fetch: 100 memory access: assume hit rate = 0.95
- Data read/ write: 30 memory access: assume hit rate = 0.90

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- Cycle# w/o. cache: $(100 + 30) \times 8$
- Cycle# w. cache:
$100 \cdot [0.95 \times 1 + 0.05 \times (1 + 15 + 1)] + 30 \cdot [0.9 \times 1 + 0.1 \times (1 + 15 + 1)]$