CENG 3420 Midterm (2018 Spring)

Name: __________
ID: __________

Solutions

Q1 **(20%)** Check or fill the correct answer:

1. Temporal / Spatial locality keeps recently accessed data items closer to the processor.
2. Drive strength of a gate can be increased by reducing resistance / capacitance.
3. Name 3 instructions that can do branch _____ , _____ and _____.
4. MIPS stack address grows from low / high to low / high.
5. As one of the evaluation metrics of computer, throughput / CPI is defined by the total amount of work done in a given time.
6. A flip-flop is level-sensitive / edge-triggered.
7. There are 3 mapping strategies in cache design, direct / fully-associative / set-associative mapping is widely used in current CPU design.

A1

1. Temporal
2. resistance
3. j, jr, jal, beq, blt, bgt (any 3 can get full mark)
4. high, low
5. throughput
6. edge-triggered
7. set-associative.

Q2 (15%) Following problems assume that logic blocks needed to implement a processor's datapath has the following latencies:

Item	I-Mem	Add	Mux	ALU	Regs	D-Mem	Sign-Extend	Shift-Left-2
Latency (*ps*)	200	70	20	90	90	250	15	10

1. If the only thing we need to do in a processor is fetch consecutive instructions (Figure 1), what would the cycle time be?
2. Consider a datapath similar to the one in Figure 2, but for a processor that only has one type of instruction: unconditional PC-relative branch. What would the cycle time be for this datapath?
3. Repeat 2, but this time we need to support only conditional PC-relative branches.

A2

1. 200*ps*.

2. Critical path include: Instruction memory, Sign-extend, Shift left 2, Add and Mux. The cycle time will be

$$CycleTime = 200 + 15 + 10 + 70 + 20 = 315ps. \tag{1}$$

An example of this problem can be found at slides L06.12, L06.13. Because we are talking about unconditional branch, no need to access Register File and ALU. Note that the architecture in Fig 2 is slightly different from L06.13 with an additional MUX between Add and PC.

3. For the PC-relative conditional branch, there are two sub-datapath to finish the instruction before entering the final MUX. (1) IM→Sign-ext→ Shift left 2→ADD and (2) IM→Register File→MUX→ALU. Then,

$$Path_1 = 200 + 15 + 10 + 70 = 295ps \tag{2}$$
$$Path_2 = 200 + 90 + 20 + 90 = 400ps > Path_1. \tag{3}$$

Thus, the cycle time is determined by the longest path,

$$CycleTime = Path_2 + MUX = 420ps. \tag{4}$$

Q3 (15%) Given the following specs of the datapath latencies:

Table 1: Question 3

Stages	IF	ID	EX	MEM	WB
Latencies (ps)	200	170	220	210	150

1. What is the clock cycle time in a pipelined and non-pipelined processor?
2. What is the total latency of an `LW` instruction in a pipelined and non-pipelined processor?
3. If we can split one stage of the pipelined datapath into two new stages, each with half the latency of the original stage, which stage would you split and what is the new clock cycle time of the processor?

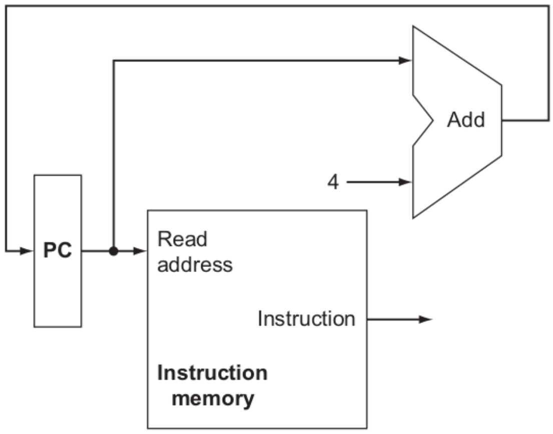

Figure 1: A portion of the datapath used for fetching instructions and incrementing the program counter.

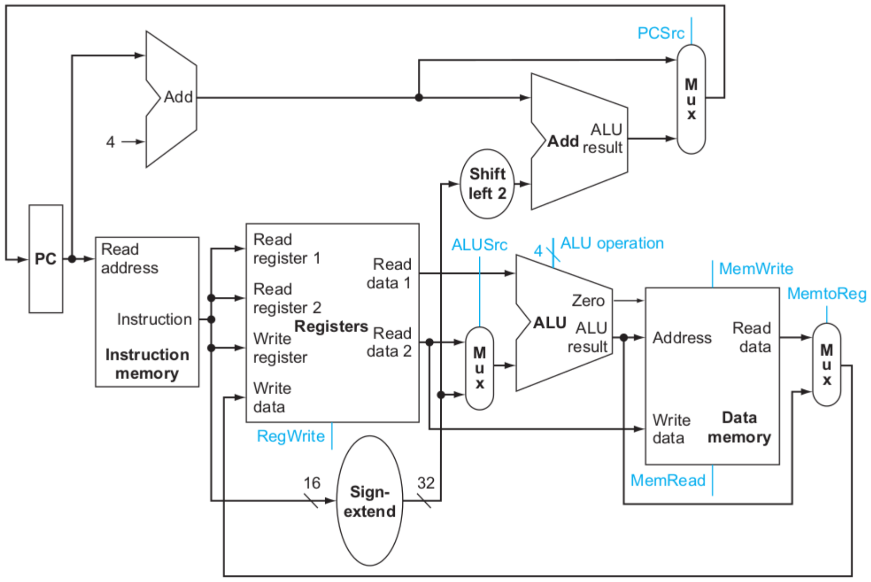

Figure 2: The simple datapath for the core MIPS architecture combines the elements required by different instruction classes.

A3
1. Non-pipelined: 950ps; Pipelined: 220ps.
2. Non-pipelined: 950ps; Pipelined: 1100ps.
3. Split EX stage. New clock cycle will be 210ps.

Q4 (10%) Consider a 4-block empty Cache, and all blocks initially marked as not valid, Given the main memory word addresses “4 1 2 0 4 3 7 2”, calculate Cache hit rate.

A3 Only last mem(2) hits. Hit rate is 0.125.

Q5 (10%) A program runs in 10 s on computer A with 2 GHz clock. If we want to design a computer B such that the same program can be finished in 10 s, determine the clock frequency of computer B. Assume it requires 1.5× clock cycles to execute the program on computer B due to different CPU design.

A5 CPU clock cycle of the program on computer A is,

$$cycle_A = 10s \times 2\text{GHz} = 2 \times 10^{10}\text{cycles}. \tag{5}$$

CPU clock cycle of the program on computer B is,

$$cycle_B = 1.5 \times cycle_A = 3 \times 10^{10}\text{cycles}. \tag{6}$$

Clock frequency of computer B will be,

$$cycle_B/10s = 3\text{GHz}. \tag{7}$$

Q6 (**20%**) Consider a single-level cache with an access time of 2.5 ns, a line size of 64 bytes, and a hit ratio of H = 0.95. Main memory uses a block transfer capability that has a firstword (4 bytes) access time of 50 ns and an access time of 5 ns for each word thereafter.

1. What is the access time when there is a cache miss?
2. Suppose that increasing the line size to 128 bytes increases the H to 0.97. Does this reduce the average memory access time?

A6 1. $T_{miss} = 2.5 + 50 + (15)(5) + 2.5 = 130ns$

2. $T_s = (0.95)(2.5) + (0.05)(130) = 8.875ns$
   After modification,
   $T_s = (0.97)(2.5) + (0.03)(210) = 8.725ns$
   Therefore average memory access time is reduced.

Q7 (**10%**) You are required to develop some simple measures of pipeline performance and relative speedup.

1. Let $T_{k,n}$ be the total time required for a pipeline with k stages to execute n instructions. Speedup of k stage pipeline is given by,

$$S_k = \frac{T_{1,n}}{T_{k,n}}. \tag{8}$$

Determine S_k in terms of k and n.

2. Consider an instruction sequence of length n that is streaming through the instruction pipeline. Let p be the probability of encountering a conditional or unconditional branch instruction, and let q be the probability that execution of a branch instruction I causes a jump to a nonconsecutive address. Assume that each such jump requires the pipeline to be cleared, destroying all ongoing instruction processing, when I emerges from the last stage. Determine S_k in terms of k, n, p and q.

A7 1.

$$S_k = \frac{nk}{k+n-1}.$$

2.

$$S_k = \frac{nk}{pqnk + (1-pq)(k+n-1)}.$$