CENG3420 Homework 1

Due: Feb. 04, 2018

Solutions

Q1 (10%) Draw the schematic view of four-input NAND gate.
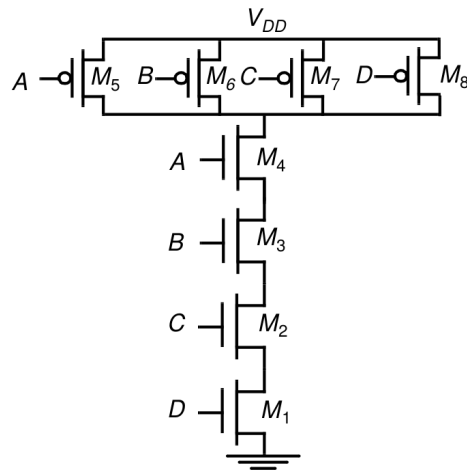
A1 As shown in Figure 1.

Figure 1: Schematic view of four-input NAND gate.

Q2 (20%) Solve the problems about multiplexer.

1. (10%) Write down the logic expression of a multiplexer with 2^n inputs and n selection lines.

2. (10%) Design the multiplexer when $n = 1$ with only **NAND** and **NOT** gates (Use the symbols given in slides L02.13).

A2 1.

$$Y = (S_{n-1}^- \ldots \bar{S}_1 \bar{S}_0 I_0) + (S_{n-1}^- \ldots \bar{S}_1 S_0 I_1) + \cdots + (S_{n-1} \ldots S_1 S_0 I_{n-1}), \quad (1)$$

where S_is are selection signals and I_is are inputs.

2. When $n = 1$, Equation (1) becomes,

$$Y = S_0 I_1 + \bar{S}_0 I_0 = \overline{\overline{\bar{S}_0 I_0} \overline{S_0 I_1}}, \quad (2)$$

which corresponds to the circuit as shown in Figure 2.

Q3 (15%)

1. (10%) Translate the following C function into MIPS assembly.
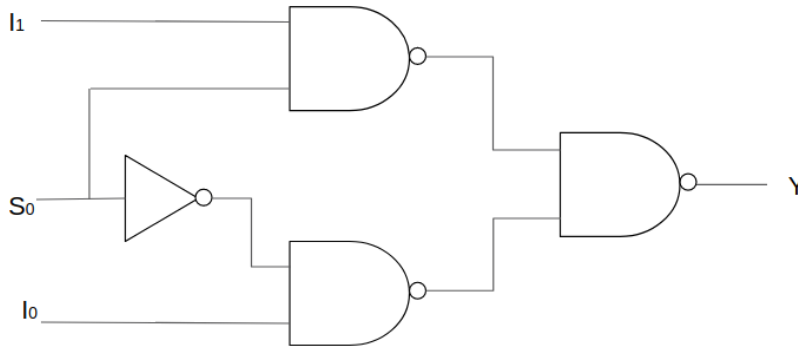
Figure 2: 2-input multiplexer.

```
int sum(int n, int rst){
    if (n>0)
        return sum(n-1, rst+n)
    else
        return rst
}
```

2. (5%) Is the access to the stack necessary? Please elaborate the resons.

A3 As shown below (assume that $a0=n and $a1=rst):

```
sum:
slti $t0, $a0, 1
bne $t0, $zero, sum_exit
add $a1, $a1, $a0
addi $a0, $a0, -1
j sum
sum_exit:
add $v0, $a1, $zero
jr $ra
```

Q4 (15%) Write an assembly function to clear an array `array[]` with size `size` (i.e. set every elements to zero). Assume two parameters `array` and `size` are stored in `$a0` and `$a1`.

A4 Here is a sample solution:

```
move $t0, $zero
loop:
sll $t1, $t0, 2
add $t2, $a0, $t1
sw $zero, 0($t2)
addi $t0, $t0, 1
slt $t3, $t0, $a1
bne $t3, $zero, loop
```

Q5 (10%) A program runs in $10s$ on computer A with 2GHz clock. If we want to design

a computer B such that the same program can be finished in $6s$, determine the clock frequency of computer B. Assume it requires 1.2X clock cycles to execute the program on computer B due to different CPU design.

A5 CPU clock cycle of the program on computer A is,

$$cycle_A = 10s \times 2GHz = 2 \times 10^{10} \text{cycles.} \tag{3}$$

CPU clock cycle of the program on computer B is,

$$cycle_B = 1.2 \times cycle_A = 2.4 \times 10^{10} \text{cycles.} \tag{4}$$

Clock frequency of computer B will be,

$$cycle_B/6s = 4GHz. \tag{5}$$

Q6 (10%) Dynamic power of one transistor is proportional to the capacitive load (C), square voltage (V^2) and working frequency (f). Suppose we have developed new versions of a processor with the following characteristics.

Version	Voltage	Clock Rate
Version 1	1.3 V	5 GHz
Version 2	0.8V	4 GHz

1. (5%) How much has the capacitive load varied between versions if the dynamic power of version 2 is 20% less than version 1?

2. (5%) How much has the dynamic power been reduced if the capacitive load does not change?

A6 1. $4 \times 0.8^2 C_2/5 \times 1.3^2 C_1 = 0.8 \implies C_2/C_1 = 2.64.$

2. $4 \times 0.8^2/5 \times 1.3^2 = 0.3$, i.e., reduced by 70%.

Q7 (10%) Figure 3 shows a simple multiplication algorithm in ALU design. Write down the step by step procedure to calculate 7×3 or 00000111×0011. Use 4-bit numbers in the calculation.
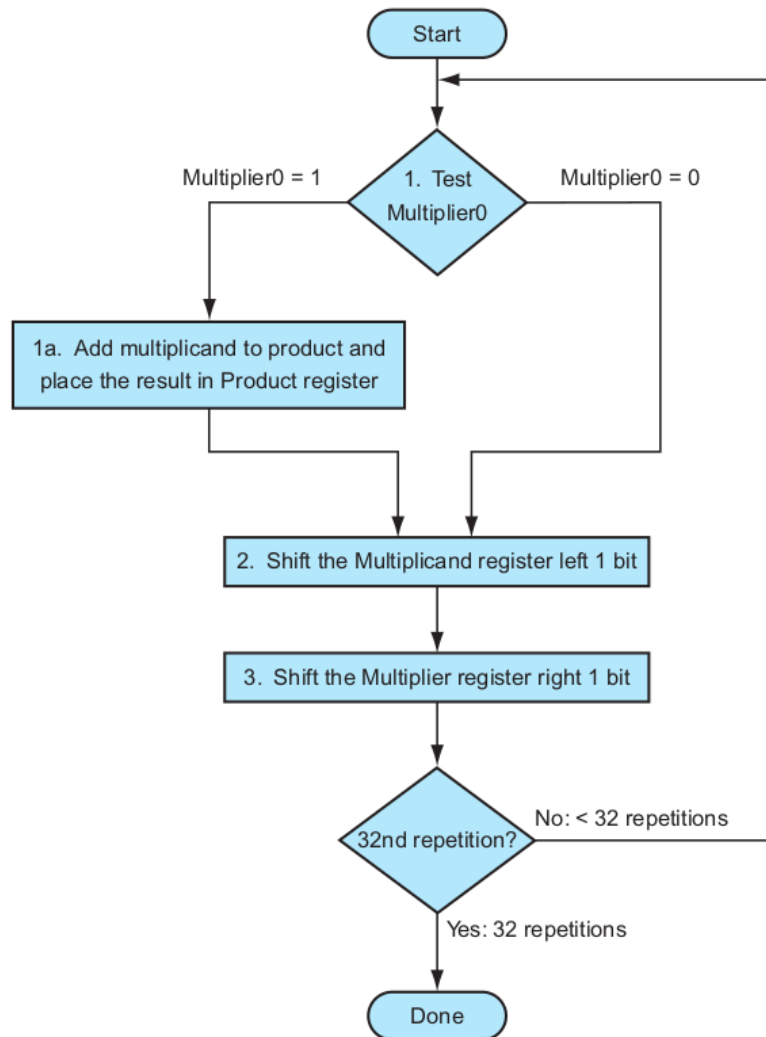

Figure 3: A simple multiplication algorithm.

A7 As shown in Table 1.

Multiplcand	Multiplier	Multiplier0	Product
0111	0011	1	00000111
1110	0001	1	00010101
1100	0000	0	00010101

Q8 (10%) Figure 4 shows a simple division algorithm in ALU design. Write down the step by step procedure to calculate $7 \div 3$ or $00000111 \div 0011$. Use 4-bit numbers in the calculation.
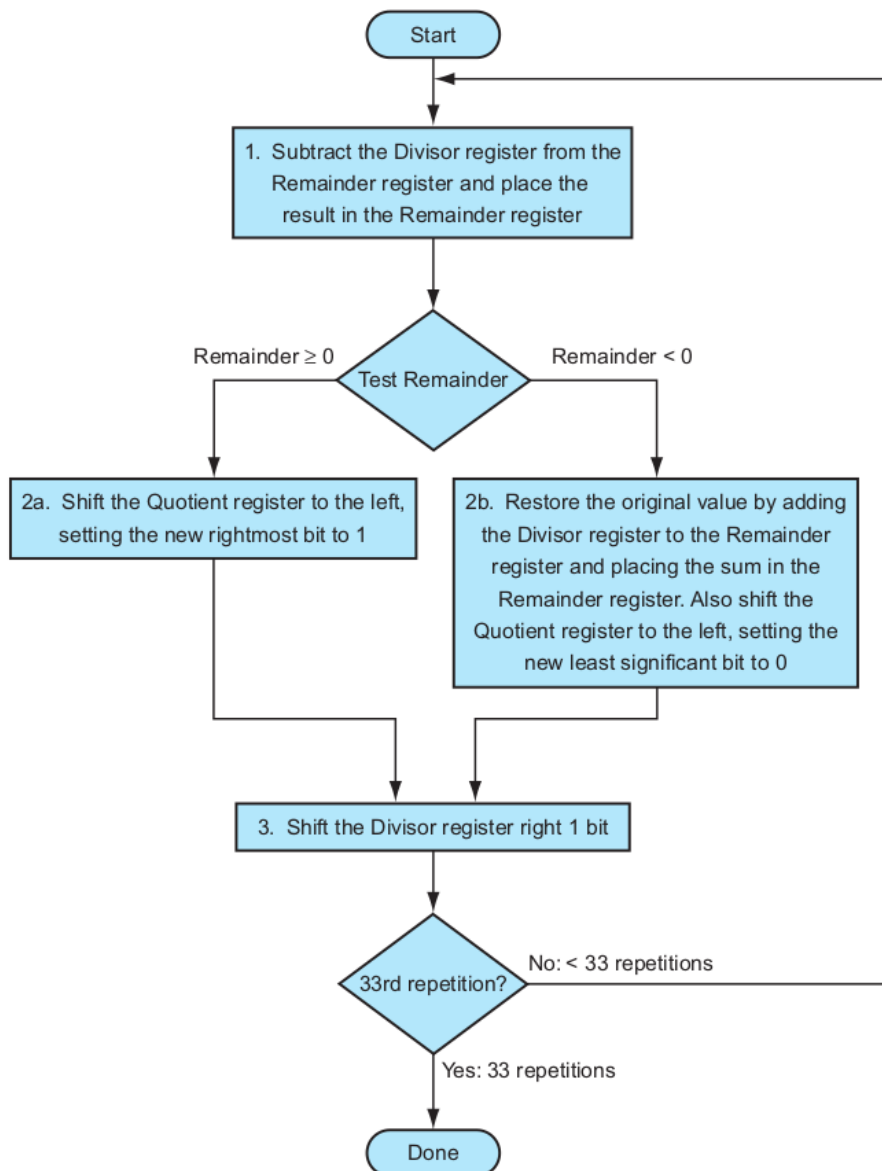

Figure 4: A simple division algorithm.

A8 As shown in Table 2.

Table 2: $7 \div 3$

Quotient	Divisor	Remainder
0000	00110000	00000111
0000	00011000	00000111
0000	00001100	00000111
0000	00000110	00000111
0001	00000011	00000001
0010	00000001	00000001