



香港中文大學
The Chinese University of Hong Kong

CENG4480

Lecture 04: Analog/Digital Conversions

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Overview

Preliminaries

Digital to Analog Conversion (DAC)

Analog to Digital Conversion (ADC)

Sample-and-Hold Amplifier



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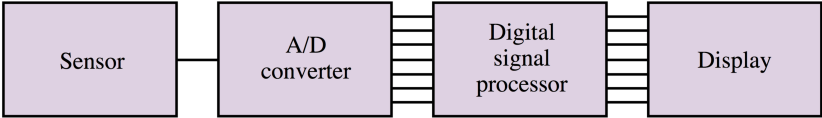
Analog/Digital Conversions

Topics:

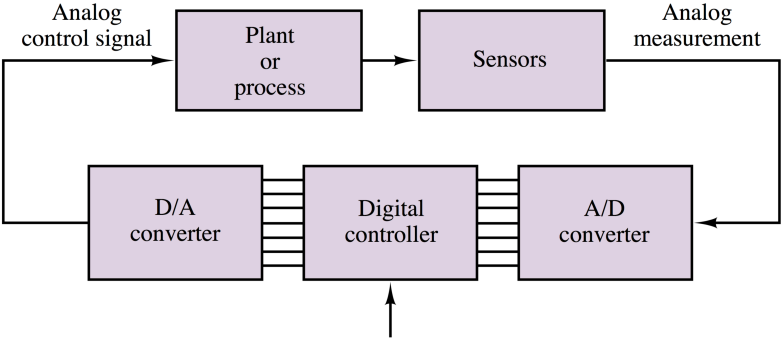
- ▶ Digital to analog conversion
- ▶ Analog to digital conversion
- ▶ Sampling-speed limitation
- ▶ Frequency aliasing
- ▶ Practical ADCs of different speed



Block Diagrams



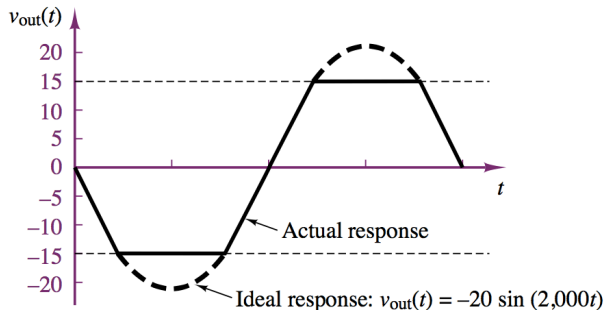
Digital measuring instrument



Digital control system



Voltage Supply Limits

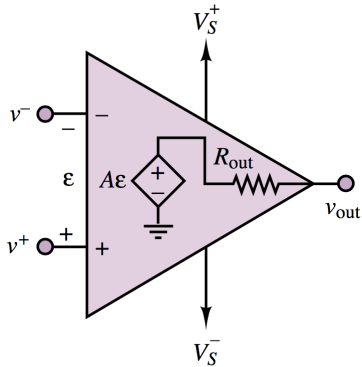


Op-amp output with voltage supply limit ($V_S^+ = V_S^- = 15$)

- ▶ Powered by external DC voltage supplies V_S^+ & V_S^-
- ▶ Amplifying signals **only** within the range of supply voltages



Op-Amp Comparator



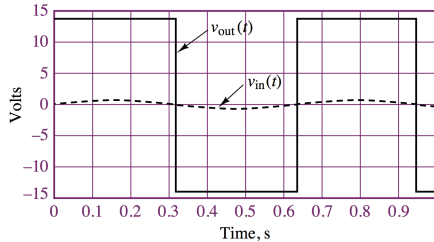
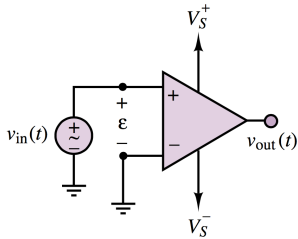
Open-Loop Mode

$$v_{out} = A_V(v^+ - v^-)$$

- ▶ Extreme large gain
- ▶ Any small difference ϵ will cause large outputs.



Switching waveforms by Comparator



Switching waveforms of non-inverting comparator.

Since $\epsilon = V \cos(\omega t)$, therefore

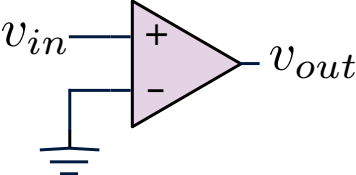
$$\epsilon > 0 \Rightarrow v_{out} = V_{sat}^+$$

$$\epsilon < 0 \Rightarrow v_{out} = V_{sat}^-$$

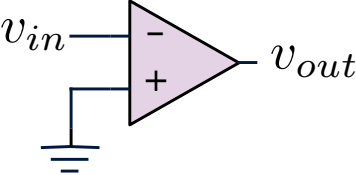
* V_{sat} : saturation voltage (e.g., ± 15 V supplies is approximately ± 13.5 V)



Noninverting & Inverting Comparator



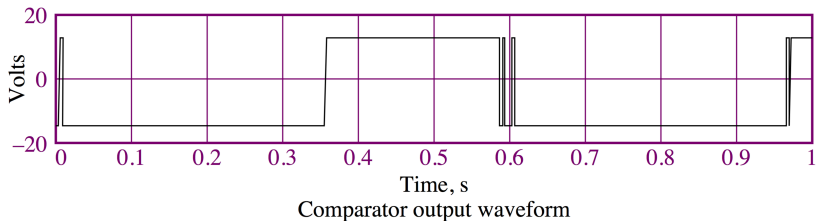
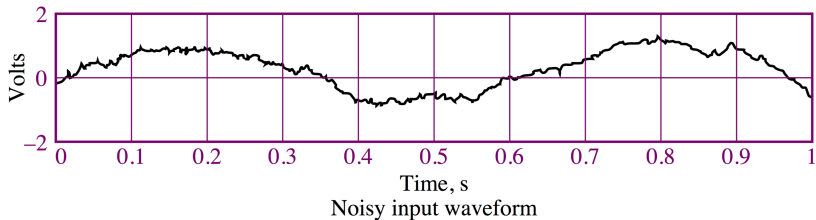
(a) Noninverting comparator



(b) Inverting comparator



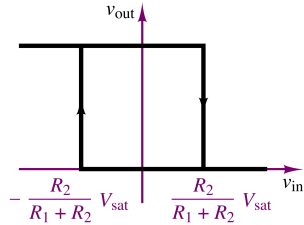
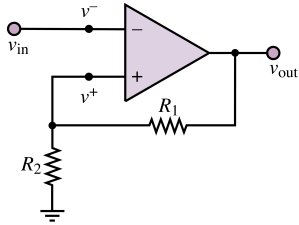
Limitation of Conventional Comparator



- ▶ In the presence of noisy inputs
- ▶ Cross the reference voltage level repeatedly
- ▶ Cause multiple triggering

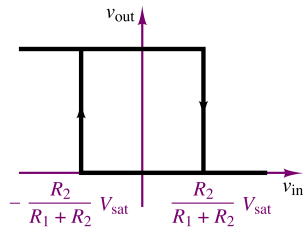
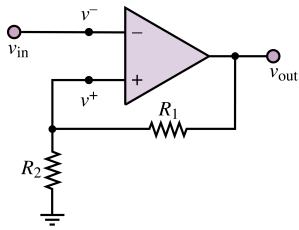


Schmitt Trigger



- ▶ Based on **Inverting** comparator
- ▶ Positive feedback
- ▶ (+) Increase the switching speed
- ▶ (+) Noise immunity





Question: prove two reference voltages of schmitt trigger.



Overview

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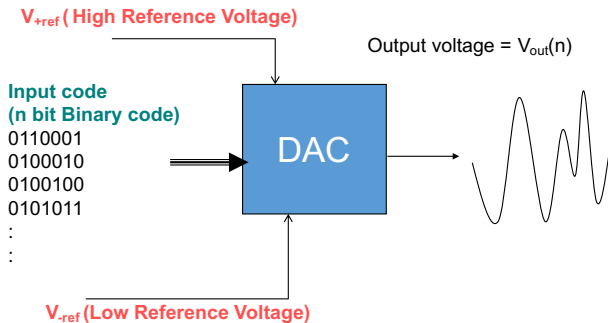
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Digital-to-Analog Converter (DAC)

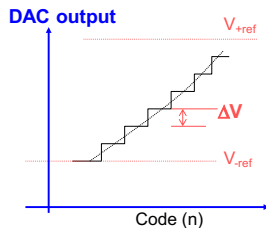
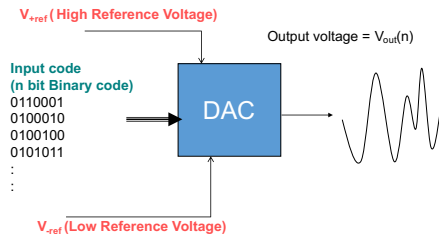


$$\begin{aligned}V_{out} &= (b_3b_2b_1b_0)_2 \\ &= (b_3 \cdot 2^3 + b_2 \cdot 2^2 + b_1 \cdot 2^1 + b_0 \cdot 2^0)_{10} \\ &= (8b_3 + 4b_2 + 2b_1 + b_0)\Delta v + V_{-ref}\end{aligned}$$

Δv : smallest step size by which voltage can increase



How to Determine Δv ?



$$\Delta v = \frac{V_{+ref} - V_{-ref}}{2^n},$$

where n is the bit# of input digital signal.



DAC Characteristics

Glitch:

A transient spike in the output of a DAC that occurs when more than one bit changes in the input code.

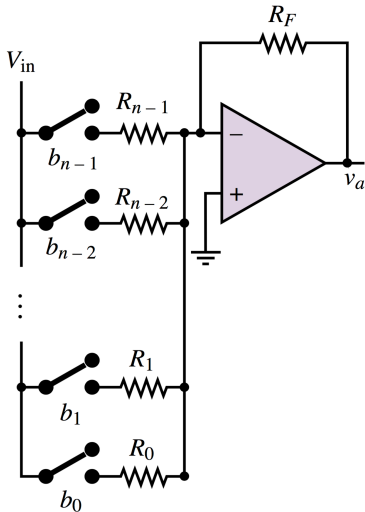
- ▶ Use a low pass filter to reduce the glitch
- ▶ Use **sample-and-hold** circuit to reduce the glitch

Settling time:

Time for the output to settle to typically $1/4$ LSB after a change in DA output.



DAC Type 1: Weighted Adder DAC

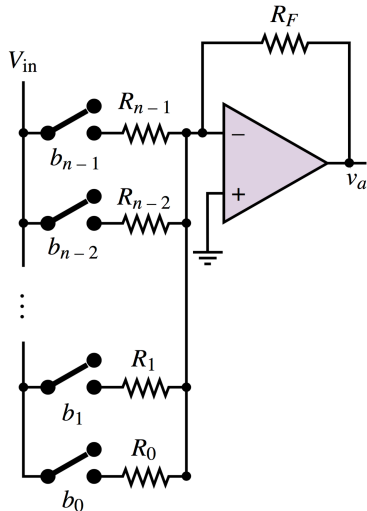


Similar to **summing amplifier**:

$$v_a = - \sum_i \left(\frac{R_F}{R_i} \cdot b_i \cdot v_{in} \right)$$



DAC Type 1: Weighted Adder DAC



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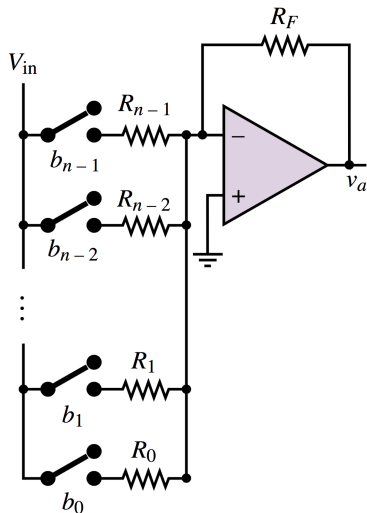
If we select $R_i = \frac{R_0}{2^i}$:

$$v_a = - \frac{R_F}{R_0} (2^{n-1} b_{n-1} + \dots + 2^1 b_1 + 2^0 b_0) \cdot v_{in}$$

Note here V_{-ref} is 0 (ground)



DAC Type 1: Weighted Adder DAC



Limitations:

- Impossible to fabricate a **wide range** of resistor values in the same IC chip

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If we select $R_i = \frac{R_0}{2^i}$:

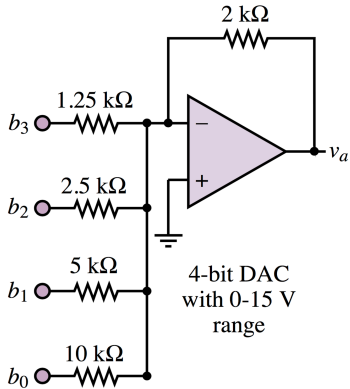
$$v_a = - \frac{R_F}{R_0} (2^{n-1} b_{n-1} + \dots + 2^1 b_1 + 2^0 b_0) \cdot v_{in}$$

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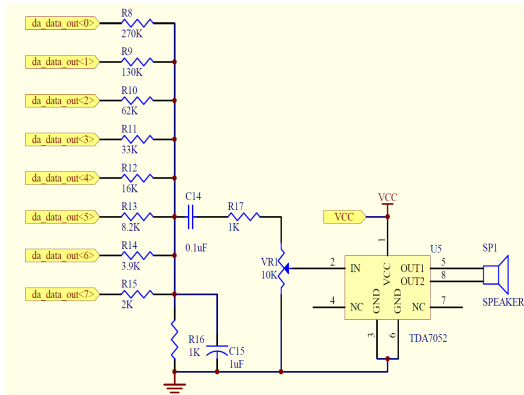


Question: 4-bit DAC

For given $(b_3b_2b_1b_0) = \{(1111), (0000), (1010)\}$, calculate v_a .



Practical Resistor Network DAC and Audio Amplifier

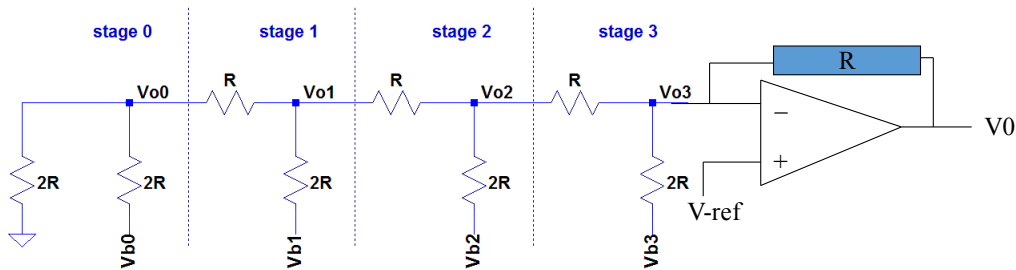


| Data Bit | Ideal R | Real R |
|----------|---------|--------|
| 0 (LSB) | 256K | 270K |
| 1 | 128K | 130K |
| 2 | 64K | 62K |
| 3 | 32K | 33K |
| 4 | 16K | 16K |
| 5 | 8K | 8.2K |
| 6 | 4K | 3.9K |
| 7 (MSB) | 2K | 2K |

► Not perfect, but okay.



DAC Type 2: R-2R DAC

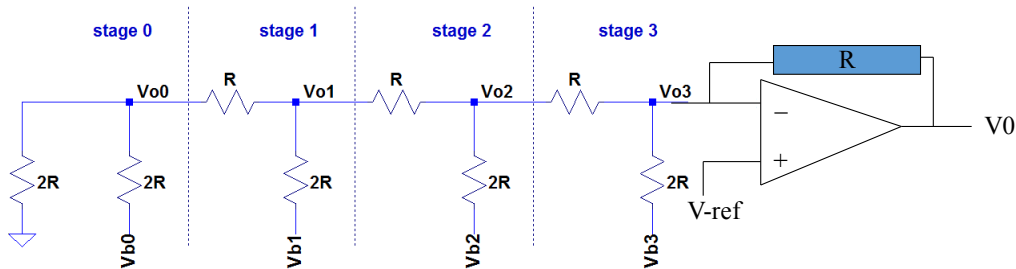


Motivations:

- ▶ Use only **two** values of resistors which make for easy and accurate fabrication and integration
- ▶ At each node, current is split into 2 equal parts
- ▶ The most popular DAC



DAC Type 2: R-2R DAC

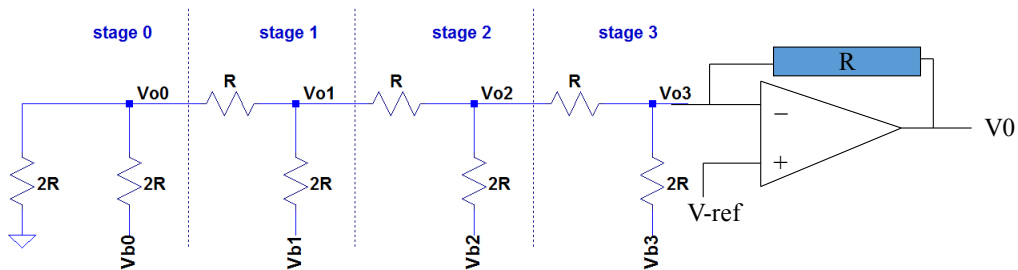


Reference:

<http://www.tek.com/blog/tutorial-digital-analog-conversion—r-2r-dac>



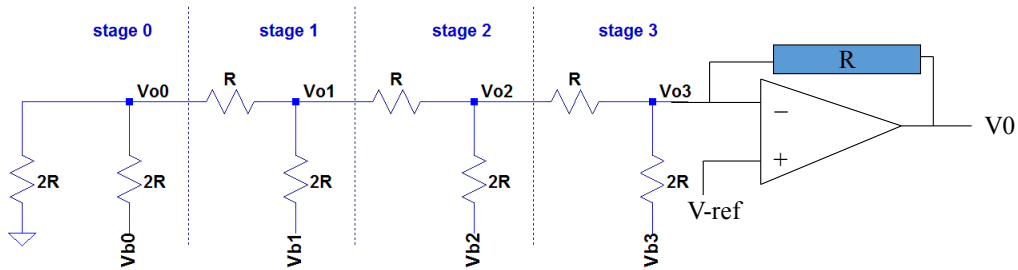
DAC Type 2: R-2R DAC



Given I as input value (n bit):

$$V_{o3} = V_{-ref} + I \cdot \frac{V_{+ref} - V_{-ref}}{2^n},$$





Question: R-2R DAC

For given $(b_3b_2b_1b_0) = \{(1111), (0000), (1010)\}$, calculate v_{o3} .



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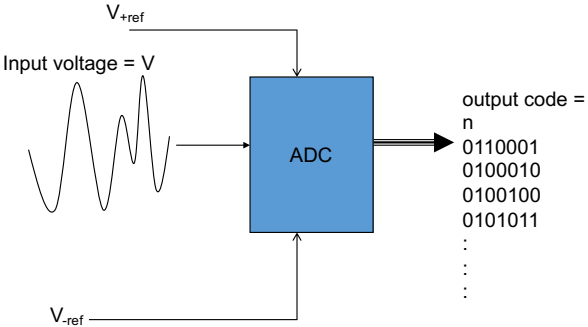
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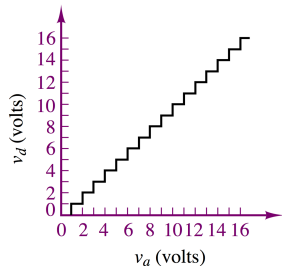
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Analog-to-Digital Converter (ADC)



Quantization

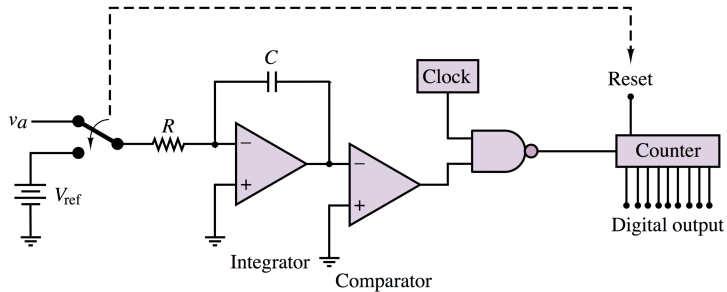


| Quantized voltage | Binary representation | | | | |
|-------------------|-----------------------|-------|-------|-------|-------|
| | v_d | b_3 | b_2 | b_1 | b_0 |
| 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 1 |
| 2 | 0 | 0 | 1 | 0 | 0 |
| 3 | 0 | 0 | 1 | 1 | 1 |
| 4 | 0 | 1 | 0 | 0 | 0 |
| \vdots | | | | | |
| 14 | 1 | 1 | 1 | 1 | 0 |
| 15 | 1 | 1 | 1 | 1 | 1 |

- ▶ Convert an analog level to digital output
- ▶ Employ $2^n - 1$ intervals (n : bit#)
- ▶ v_a : analog voltage
- ▶ v_d : output digital voltage



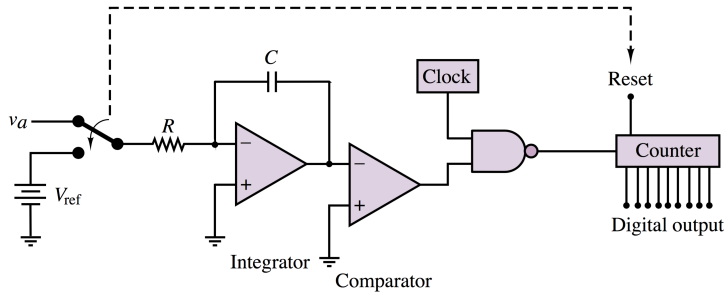
ADC Type 1: Integrating ADC



- ▶ Accumulate the input current on a capacitor for a fixed time
- ▶ Then measure time (T) to discharge the capacitor
- ▶ When cap is discharged to 0 V, comparator will stop the counter



ADC Type 1: Integrating ADC

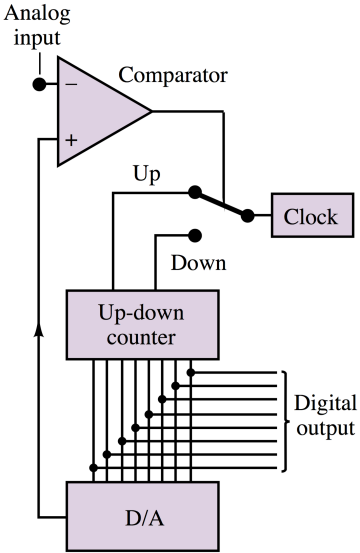


- ▶ Accumulate the input current on a capacitor for a fixed time
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Limination: Slow



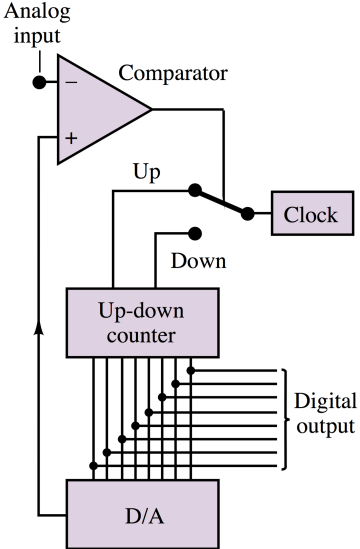
ADC Type 2: Tracking ADC



- ▶ ADC repeatedly compares its input with DAC outputs
- ▶ Up/down count depends on input/DAC output comparison



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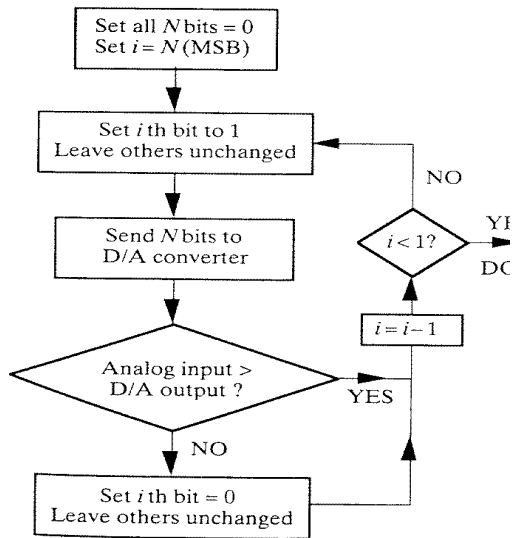


ADC Type 3: Successive Approximation

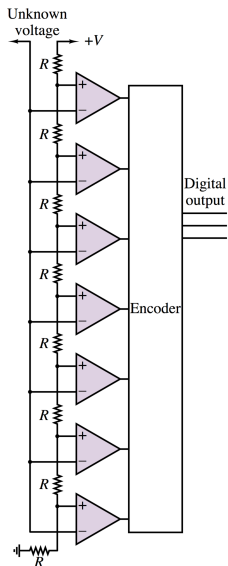
- ▶ Replace “Up-down counter” by “control logic”
- ▶ Binary search to determine the output bits
- ▶ still slow although faster than types 1 & 2



Flow chart of Successive-approximation ADC



ADC Type 4: Flash ADC

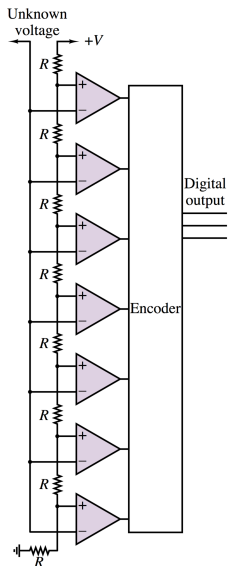


- ▶ Divide the voltage range into $2^n - 1$ levels
- ▶ Use $2^n - 1$ comparators to determine what the voltage level is
- ▶ Fully parallel

Pros:



ADC Type 4: Flash ADC



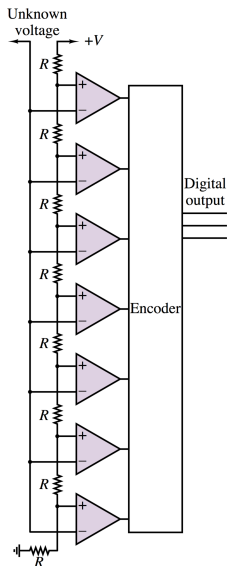
- ▶ Divide the voltage range into $2^n - 1$ levels
- ▶ Use $2^n - 1$ comparators to determine what the voltage level is
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Pros:

- ▶ Very fast for high quality audio and video
- ▶ **Sample and hold** circuit **NOT** required



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- ▶ Divide the voltage range into $2^n - 1$ levels
- ▶ Use $2^n - 1$ comparators to determine what the voltage level is
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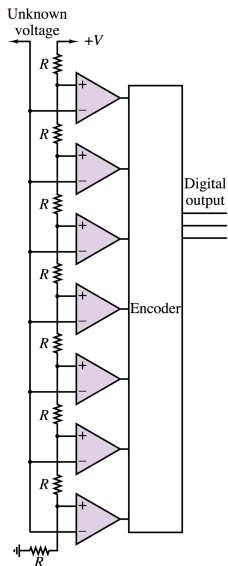
Pros:

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- ▶ **Sample and hold** circuit **NOT** required

Cons:



ADC Type 4: Flash ADC



- ▶ Divide the voltage range into $2^n - 1$ levels
- ▶ Use $2^n - 1$ comparators to determine what the voltage level is
- ▶ Fully parallel

Pros:

- ▶ Very fast for high quality audio and video
- ▶ **Sample and hold** circuit **NOT** required

Cons:

- ▶ Very expensive for wide bits conversion



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Sample-and-Hold Amplifier

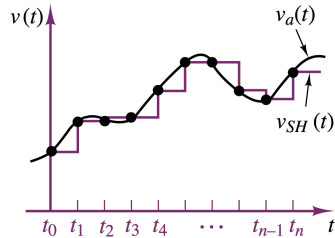
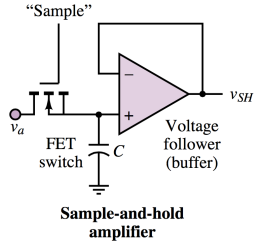
Motivations:

When a slow ADC is used to sample a fast changing signal only a short sampling point can be analyzed

- ▶ To resolve uncertainty during ADC
- ▶ “freeze” the value of analog waveform for a time sufficient for the ADC to complete its task



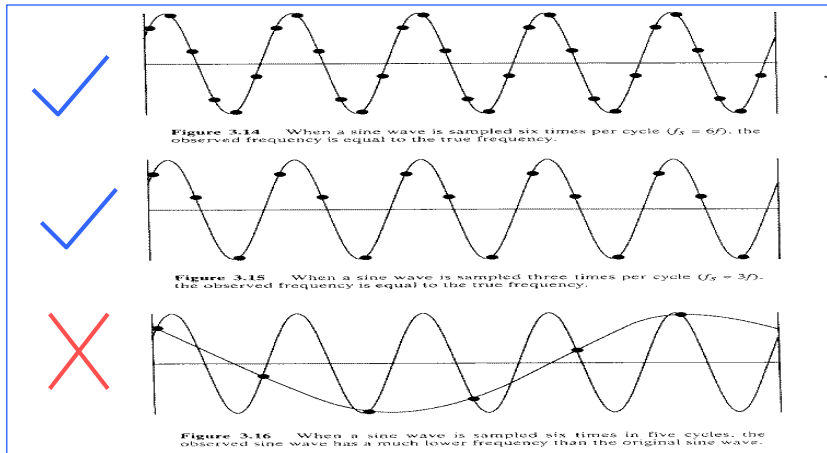
Sample-and-Hold Amplifier



- ▶ A MOSFET analog switch is used to “sample” analog waveform
- ▶ While MOSFET conducts, charge the “hold” capacitor



Good Sample, Bad Sample



- ▶ When sampling 6 times per cycle, close to the original.
- ▶ when sampling 3 times per cycle, less reliable but frequency is equal to original.
- ▶ When sampling 6 times per 5 cycles, frequency is different.

