CUHK-NTHU Jointed Seminar

Friday, April 28, 2017

Attendees

CUHK: Prof. Evangeline Young, Prof. Bei Yu, Prof. Qiang Xu

Students:

Yuzhe Ma, Haoyu Yang, Tinghuan Chen, Gengjie Chen, Chakwa Pui, Haocheng Li, Sirius Cheung, Yannan Liu, Ye Tian (more to come)

NTHU: Prof. Ting-Chi Wang, Prof. Tsung-Yi Ho

Students:

Chia-Chun Lin, Yu-Hsiang Cheng, Wen-Chun Chung, Chia-Cheng Wu, Wan-Sin Kuo

Agenda

10:00--12:00 Group Seminar

Venue: William M.W. Mong Engineering Building 713

Around 12 short seminar talks will be delivered. (Details coming soon)

12:00--14:00 Lunch

Venue: Connextion (雅薈) at S.H. Ho College

14:00--15:00 Seminar Talk by Prof. Tsung-Yi Ho

Venue: William M.W. Mong Engineering Building 1009

Title: Design and Test of Micro-Electrode-Dot-Array Digital Microfluidic Biochips

15:30--18:00 Campus Tour

(Details will be provided soon)

Group Seminar Titles

Simultaneous Layout Decomposition and Mask Optimization

Speaker: Yuzhe Ma

In&Out: Restructuring for Threshold Logic Network Optimization

Speaker: Chia-Chun Lin

Layout Hotspot Detection with Feature Tensor Generation and Deep Biased Learning

Speaker: Haoyu Yang

Robust Algorithms for Layout Pattern Classification

Speaker: Yu-Hsiang Cheng

SALT: Provably Good Routing Topology by a Novel Steiner Shallow-Light Tree Algorithm

Speaker: Gengjie Chen

Minimum Implant Area-Aware Placement and Threshold Voltage Refinement

Speaker: Wan-Sin Kuo

Fault Injection Attack on Deep Neural Network

Speaker: Yannan Liu

Majority Logic Circuits Optimisation by Node Merging

Speaker: Chia-Cheng Wu

Adaptive Memory Allocation for Lookup Table Based Approximate Computing

Speaker: Ye Tian

Module Placement under Completion Time Uncertainty in Micro-Electrode-Dot-Array Digital Microfluidic Biochips

Speaker: Wen-Chun Chung

Clock-aware FPGA Placement

Speaker: Chak-Wa Pui