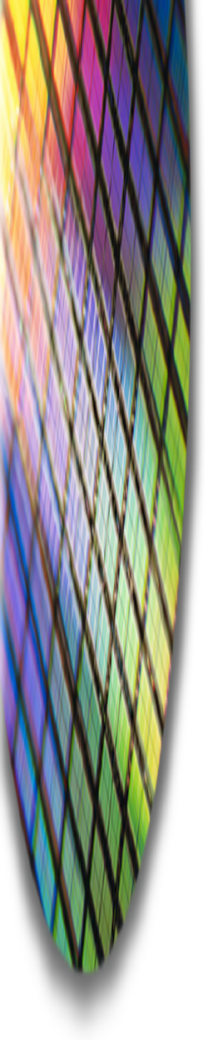

PARR: Pin Access Planning and Regular Routing for Self-Aligned Double Patterning

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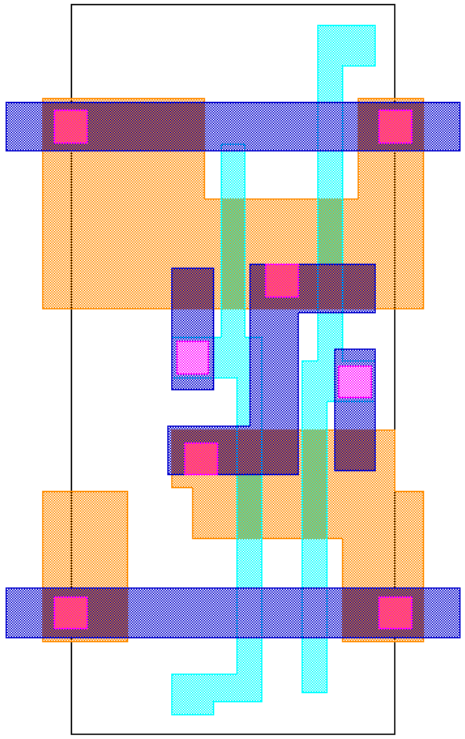
Che-Lun Hsu, David Z. Pan

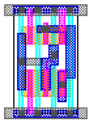
University of Texas at Austin

Detailed Routing in Extreme Scaling

- Moore's Law => Extreme Scaling



130nm NAND



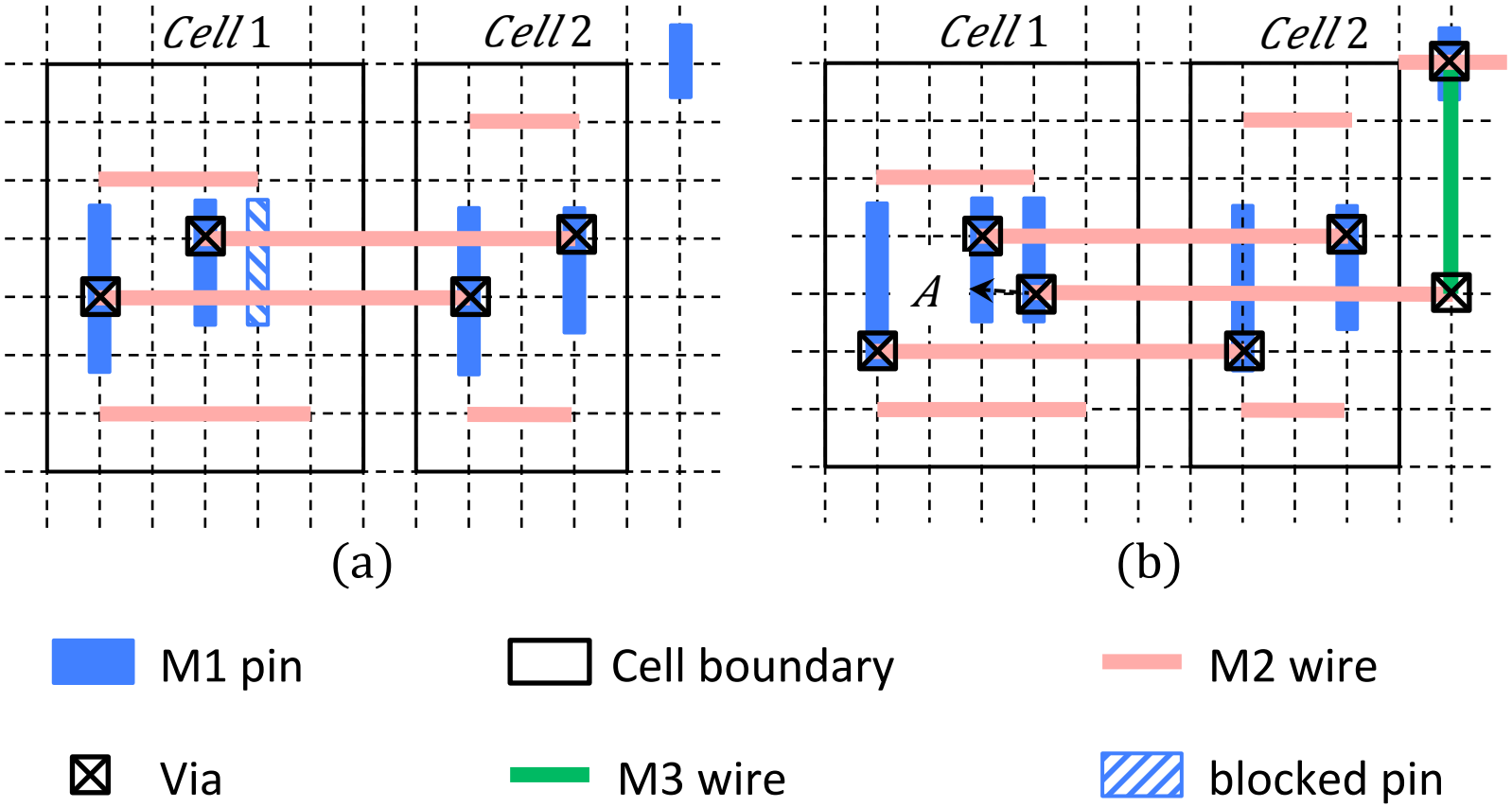
14nm NAND

[Liebmann+,SPIE'13]

- High pin density => Routability
- Less pitch => Printability

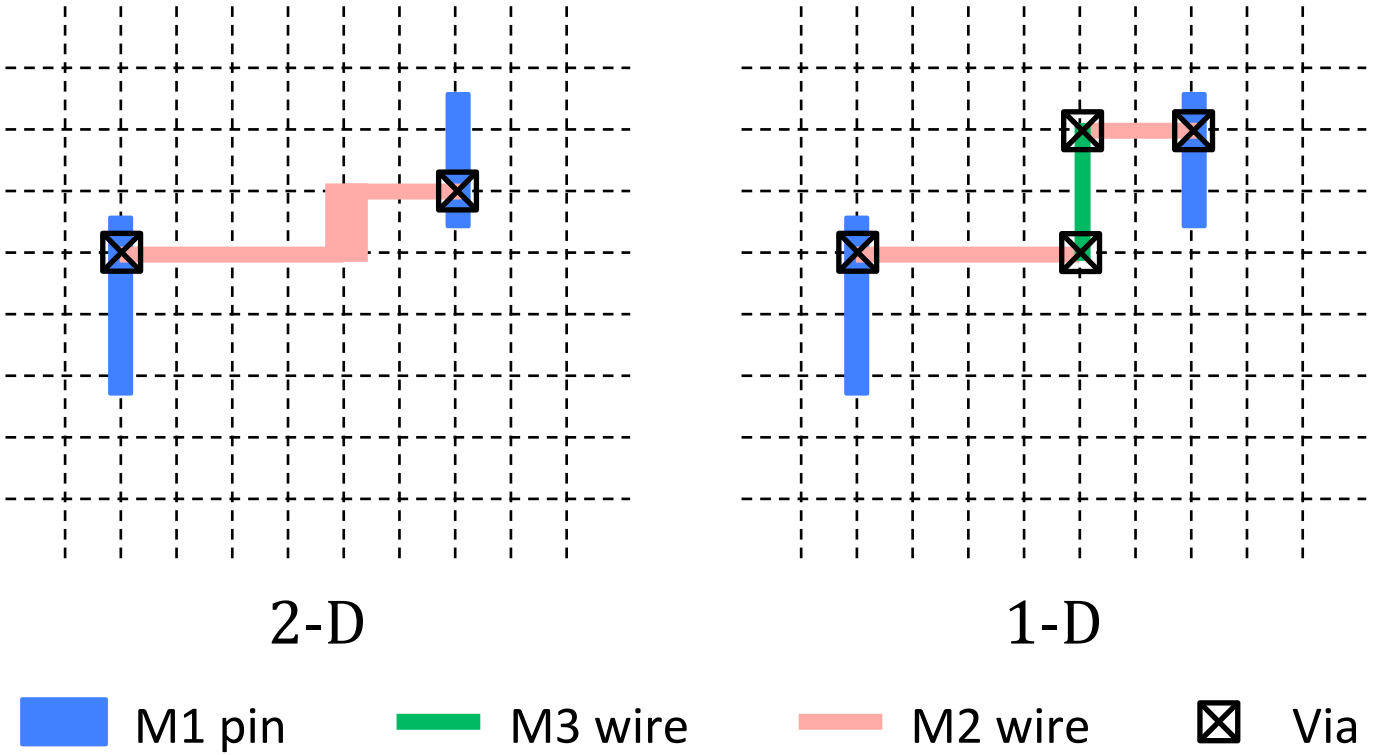
Challenge 1: Pin Accessibility

- Access Point Selection
- Net ordering



Challenge 2: Printability

- 2-D routing vs 1-D routing
  - 2D: Larger design space; but restrictive design rules
  - 1D: better printability; but extra vias



Previous Works

- Standard cell pin access [Xu+,ISPD'14] [Ye+,GLSVLSI'15]
- Pin access for placement [Taghavi+,ICCAD'10]
- Pin access for detailed routing
  [Ozdal,TCAD'09] [Nieberg+,DAC'11] [Qi+,ICCD'14]
- SADP-aware detailed routing
  [Mirsaeedi+,SPIE'11] [Gao+,ISPD'12] [Du+,DAC'13] [Liu+,DAC'14]

- **Our contributions**
  - Pin access planning and SADP-friendly 1-D routing
  - Handshake std-cell pin access with detailed routing to improve pin accessibility

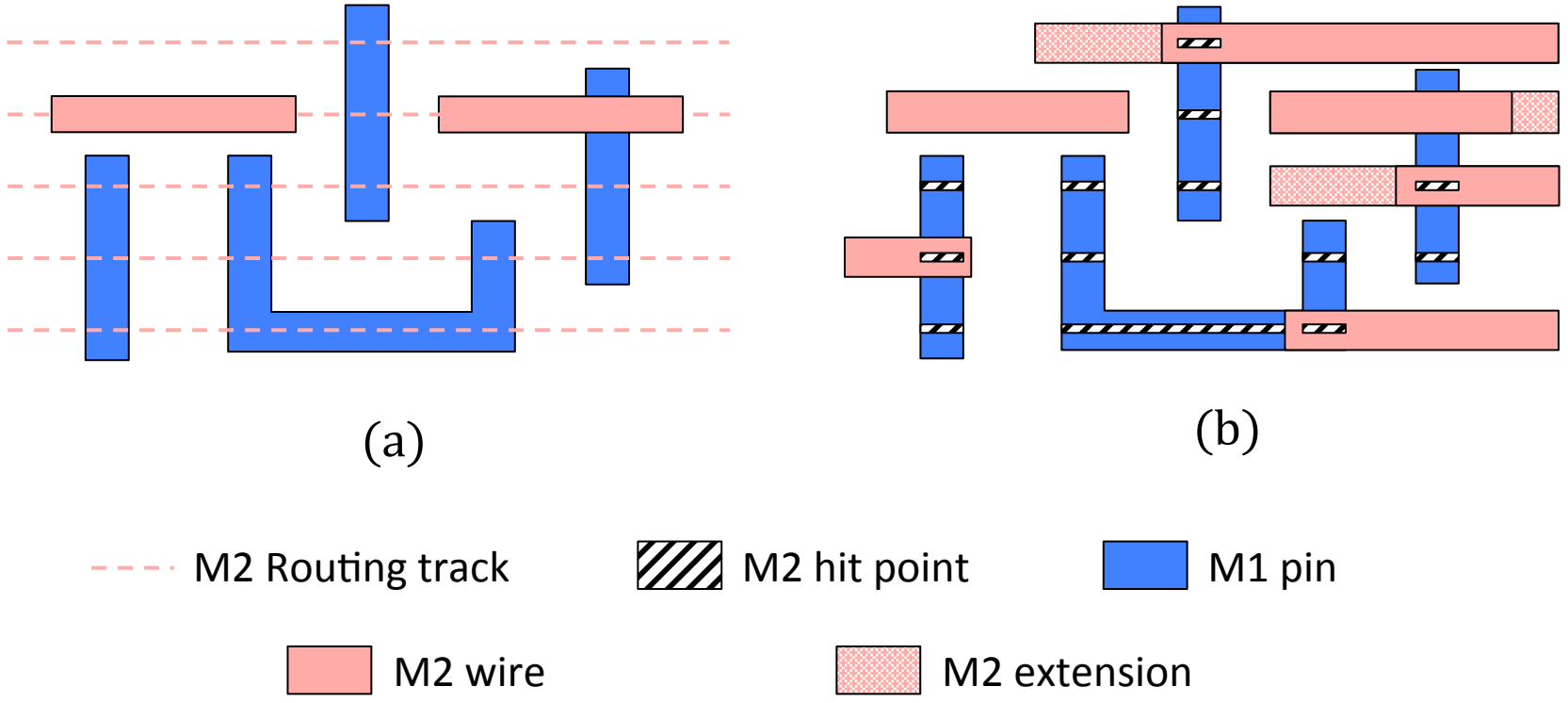
Problem Formulation

- **Input**: a netlist, pin access Look-Up Table (LUT) of the library and a set of design rules
- **Output**: design rule clean routing results

- **Objective**: perform the regular routing and design rule legalization simultaneously to achieve SADP-friendly routing results

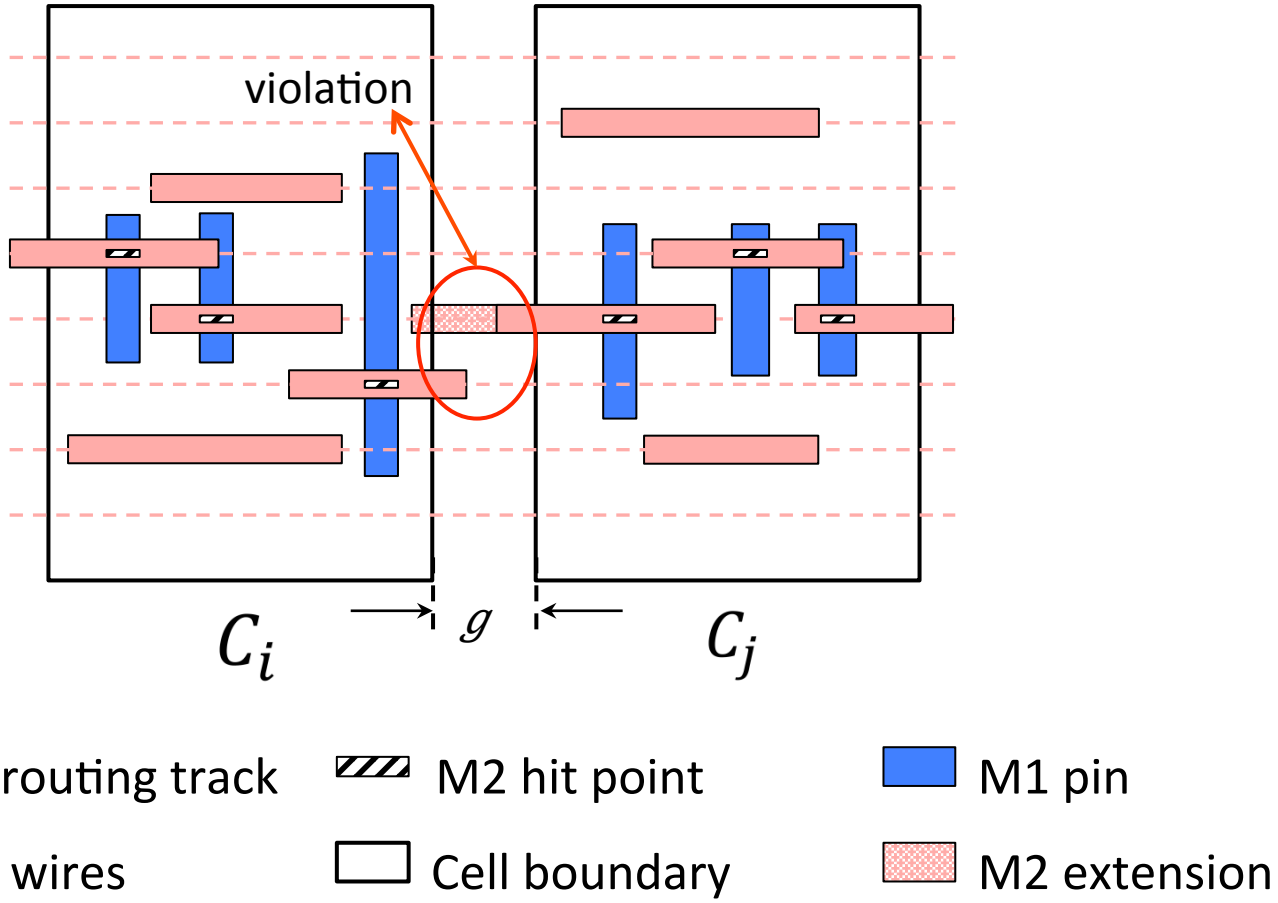
Intra-Cell Pin Access [X. Xu+, ISPD'14]

- Intra-cell pin access design
- Store in look-up table (LUT)



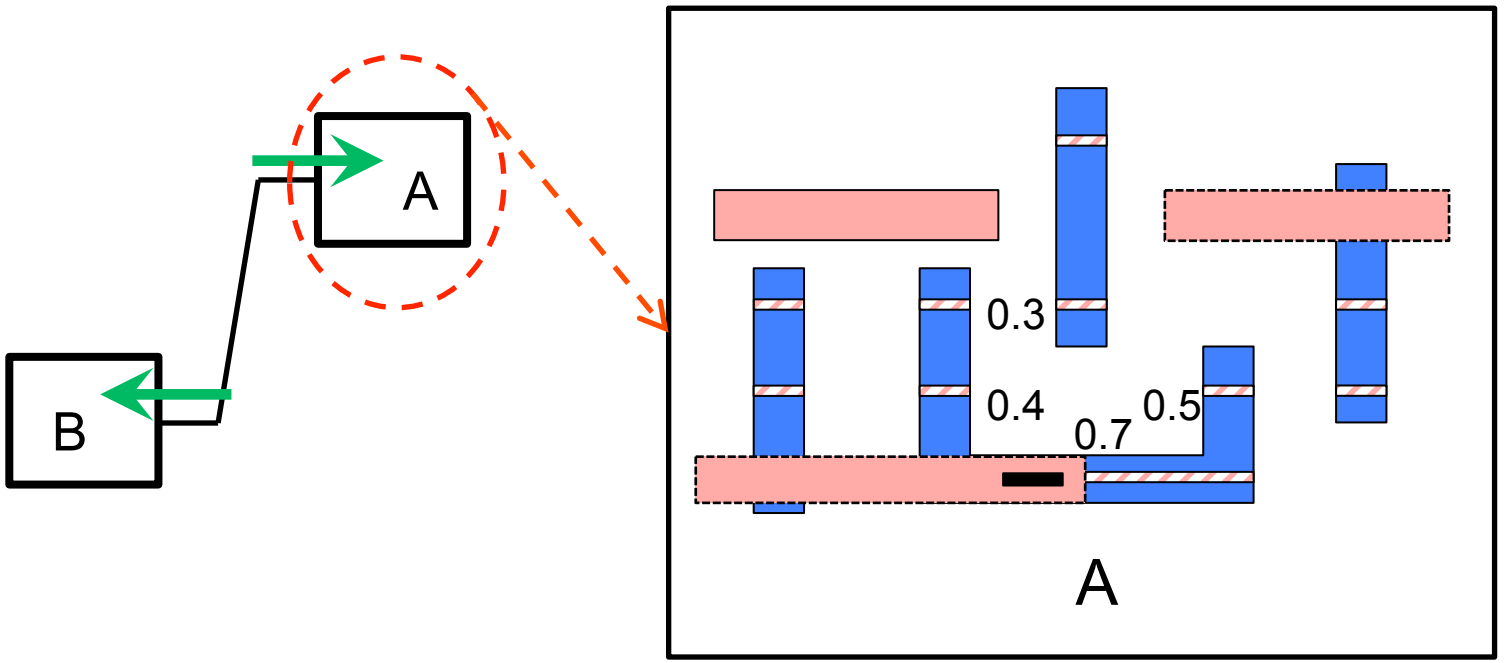
This Work: Inter-Cell Pin Access

- C_i is placed to the left of C_j with the gap as g
- Intra-cell pin access for C_i and C_j interferes



Local Pin Access Planning

- Dynamic hit point scoring
  - Source pin (A) and target pin (B)
  - Assign higher score to the hit point with larger number of intra-cell pin access solutions

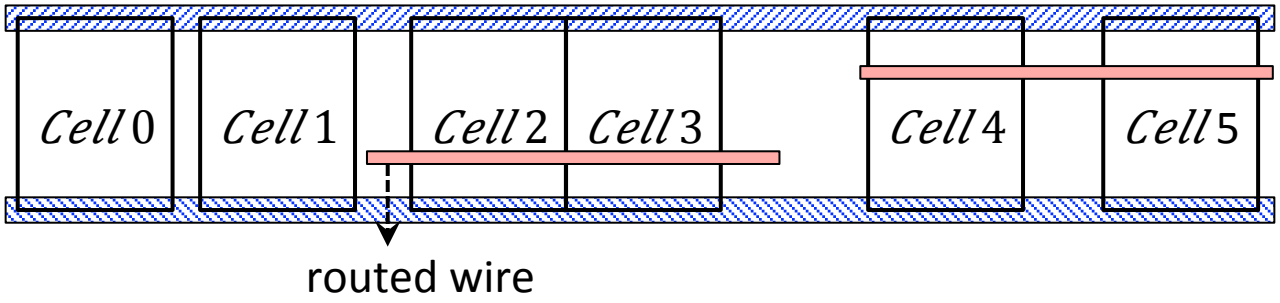


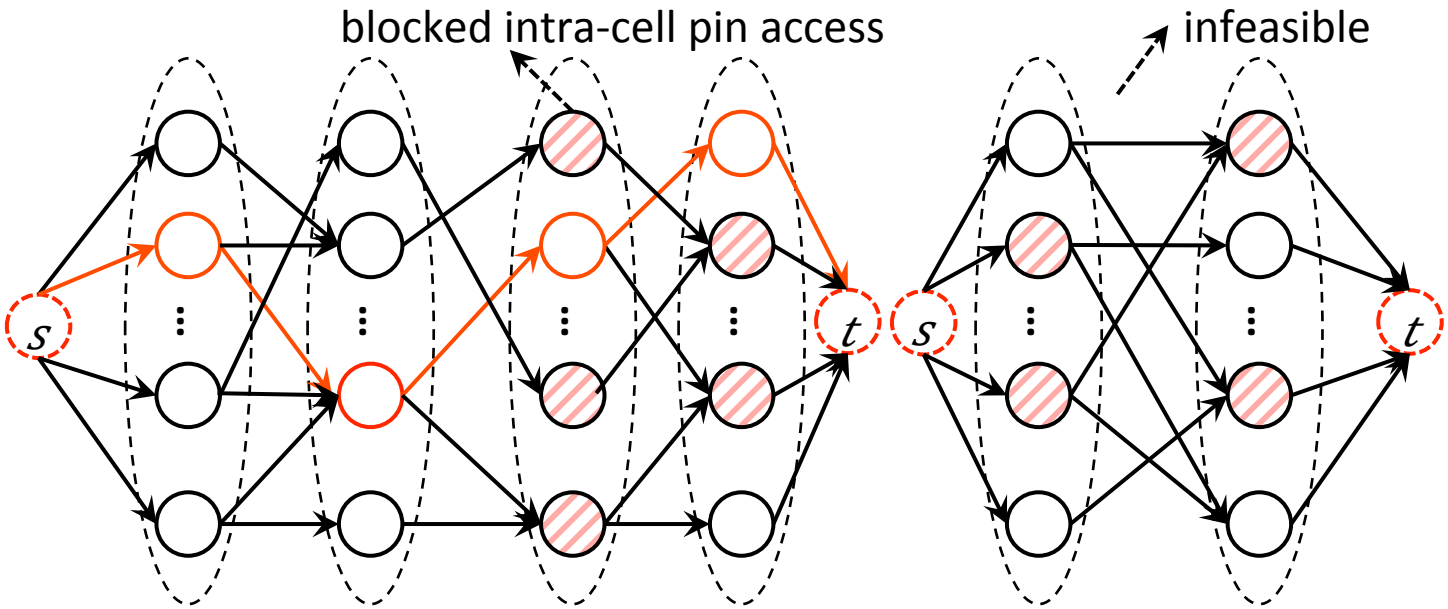
Global Pin Access Planning

- Net weight for ordering – smaller order goes first
  - Order(net) = HPWL(net)*(1+α*min{hp_s, hp_t} + Dcost(net)
- The term: min{hp_s, hp_t}- minimum # of hit points for source/target pins
  - Defer the nets with robust source and target pins
- The term Dcost(net)- deferring cost
  - Maintain the s to t path existence of of PAG
  - Preserve the pin accessibility of the remaining nets

Single Row Pin Access Graph (PAG)

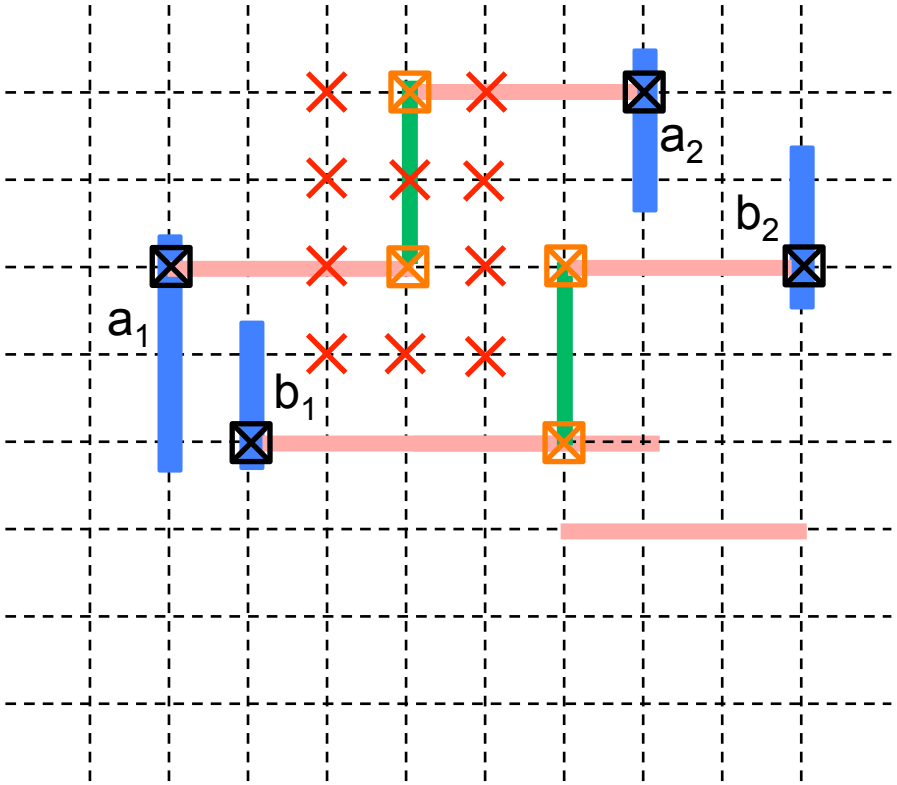
- Routed wires block some intra-cell pin access





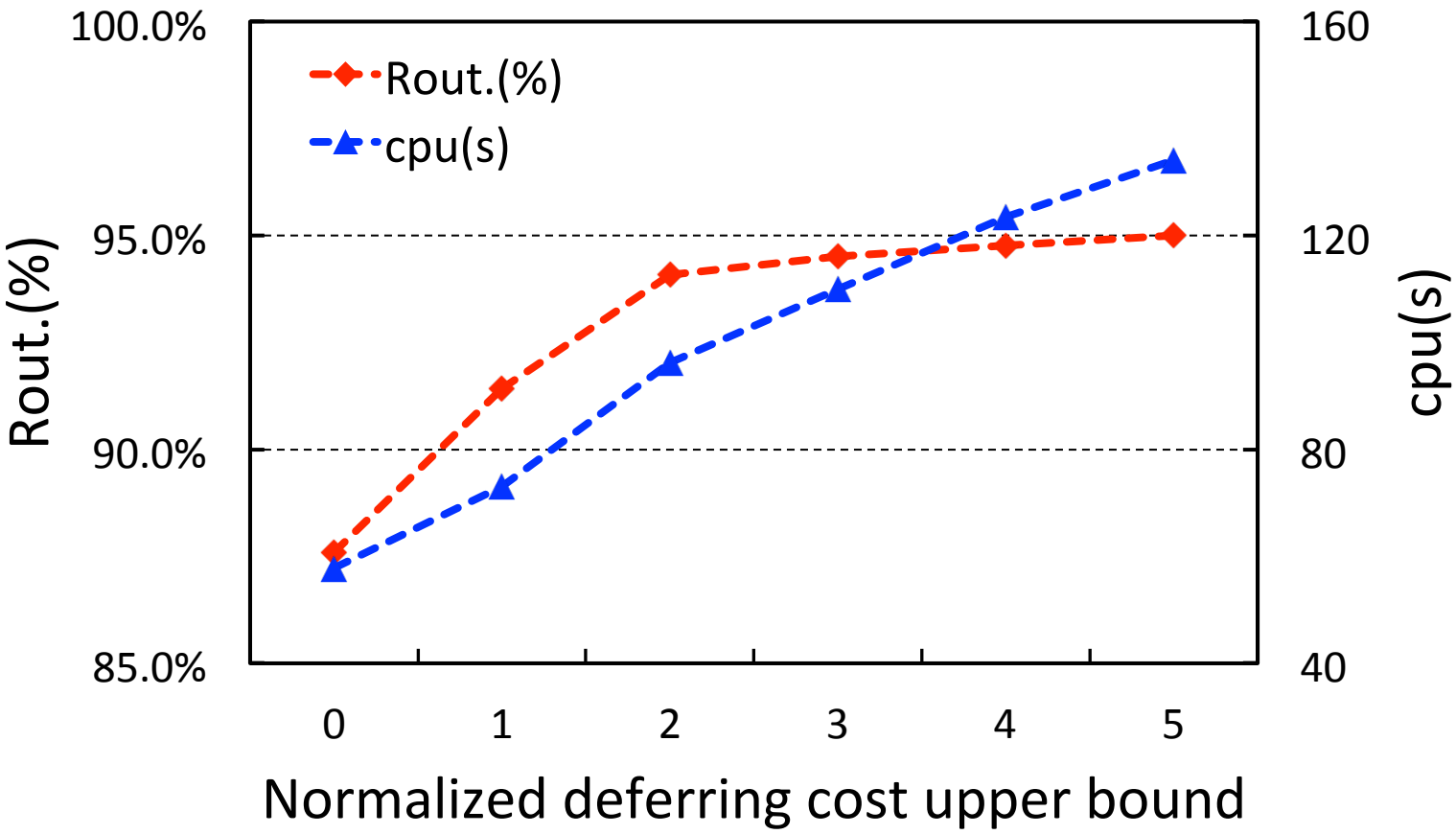
1-D Routing with Rule Legalization

- 1-D A* search
  - Forbidden via positions

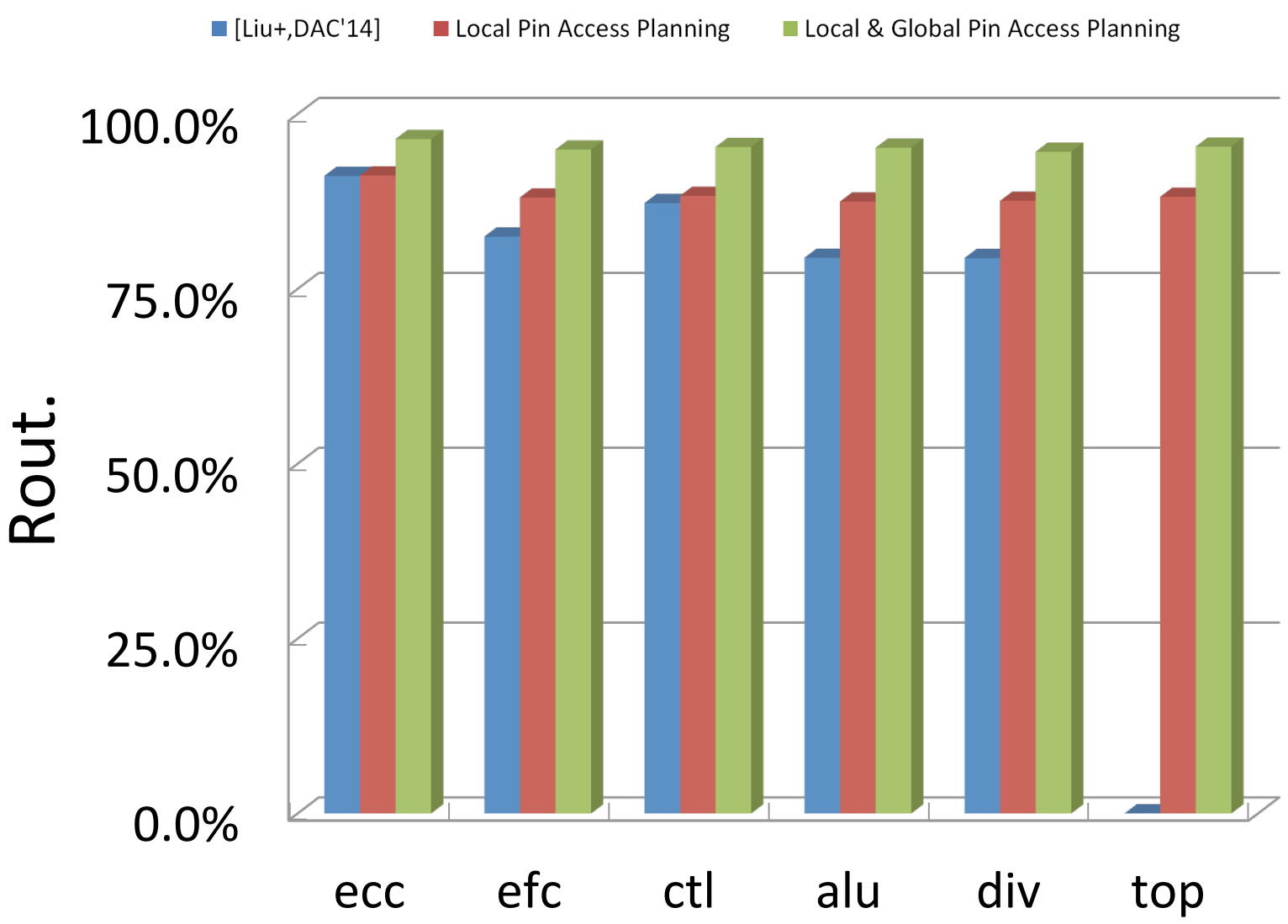


Trade-off

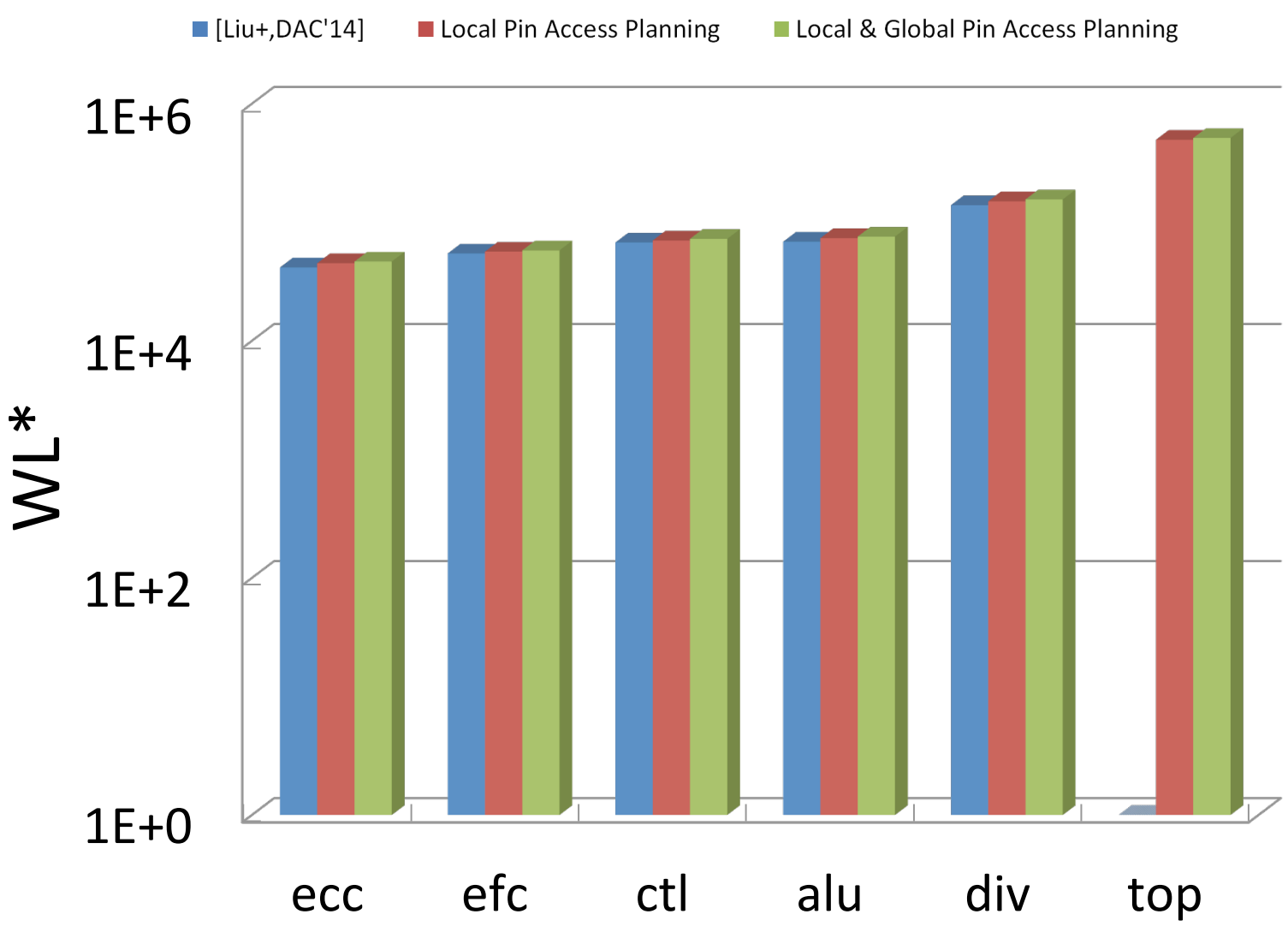
- Vary deferring cost upper bound



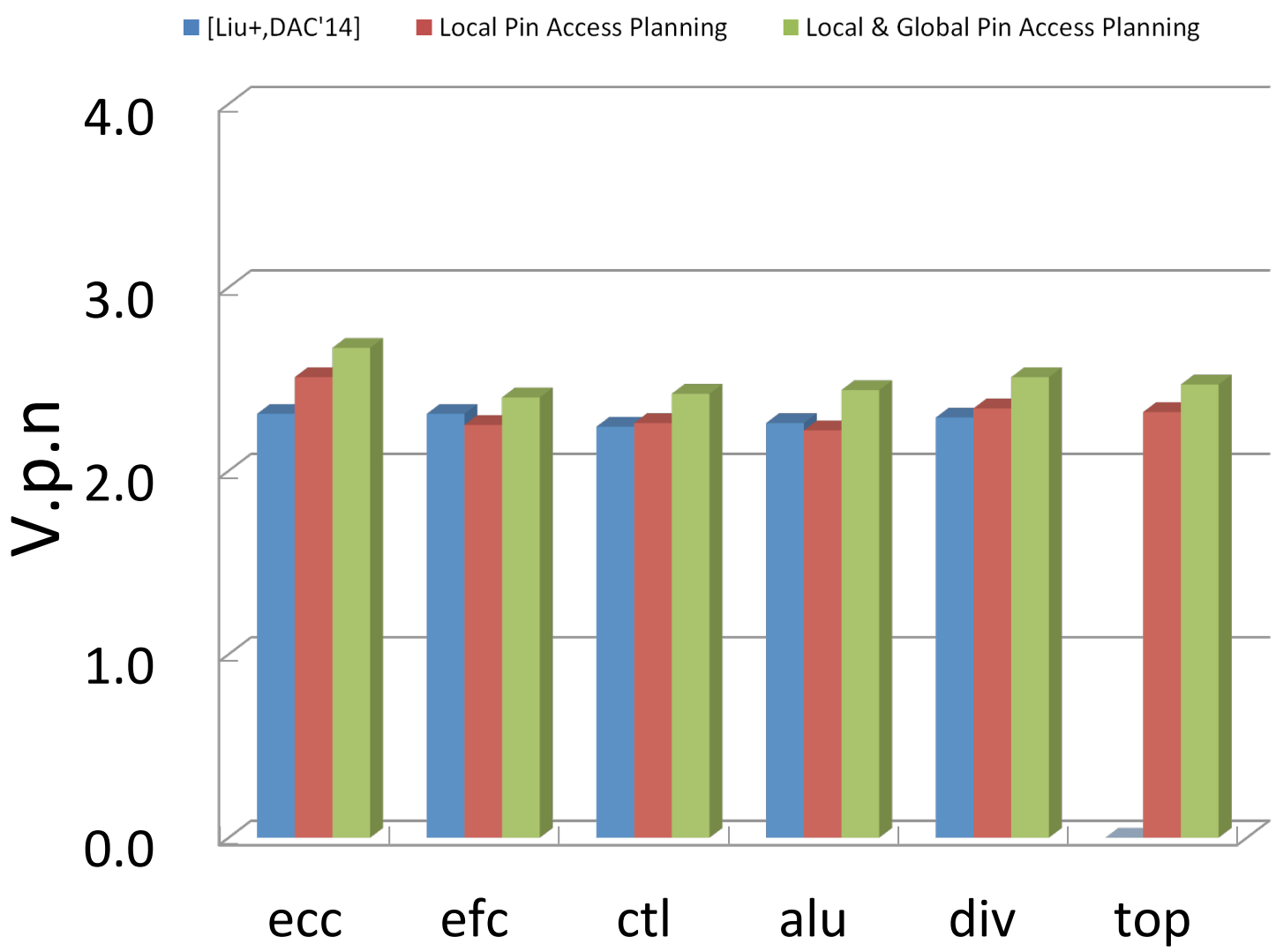
Routability Improvement



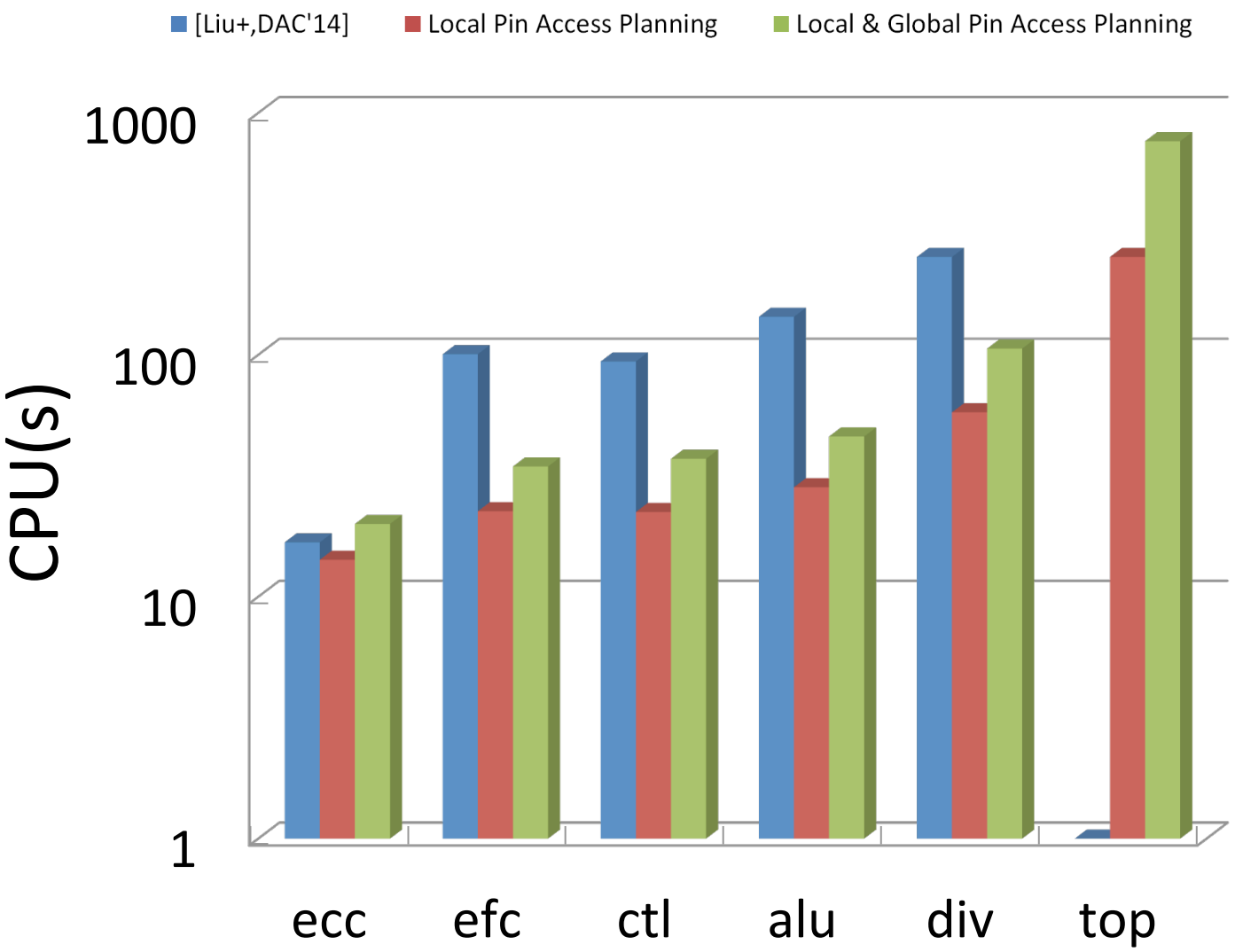
Wirelength Impact



Via Number per Routed Net (V.p.n)



Run Time Reduction



Conclusion

- Pin Accessibility Prediction
  - Intra-cell and inter-cell
- Local and Global Pin Access Planning
- 1-D routing patterns
  - Forbid the non-preferred direction

Thank you!

Q&A