

# ASP-DAC 2023

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## Mixed-Type Wafer Failure Pattern Recognition (Invited Paper)

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Tsung-Yi Ho<sup>2</sup>, Bei Yu<sup>2</sup>

<sup>1</sup>ShanghaiTech University

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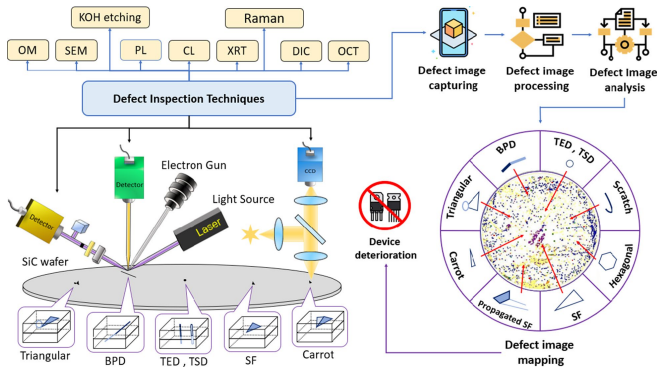
<sup>3</sup>University of Science and Technology of China

Jan. 18, 2023



# Introduction

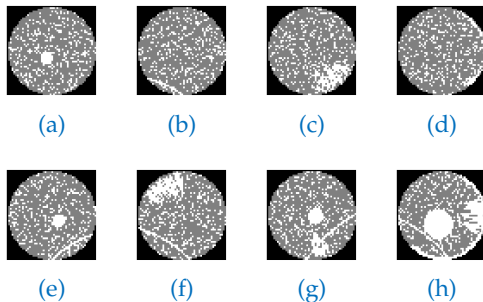
- Technology nodes shrinks, smaller but more complex circuits are etched on wafers
- Recognizing wafer defects is vital



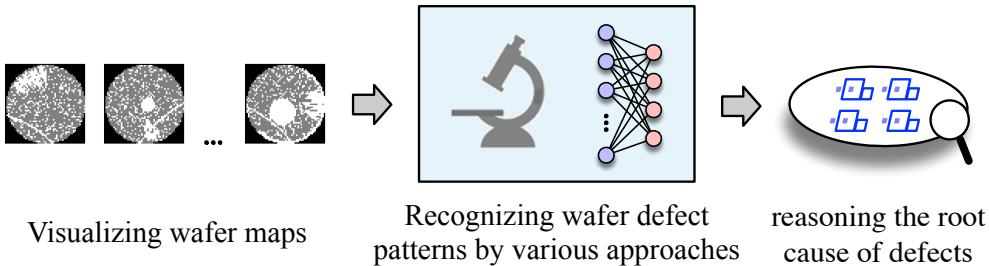
The defect inspection technologies in wafer manufacturing.<sup>1</sup>

<sup>1</sup>P.-C. Chen et al., "Defect Inspection Techniques in SiC," Nanoscale Research Letters, 2022.

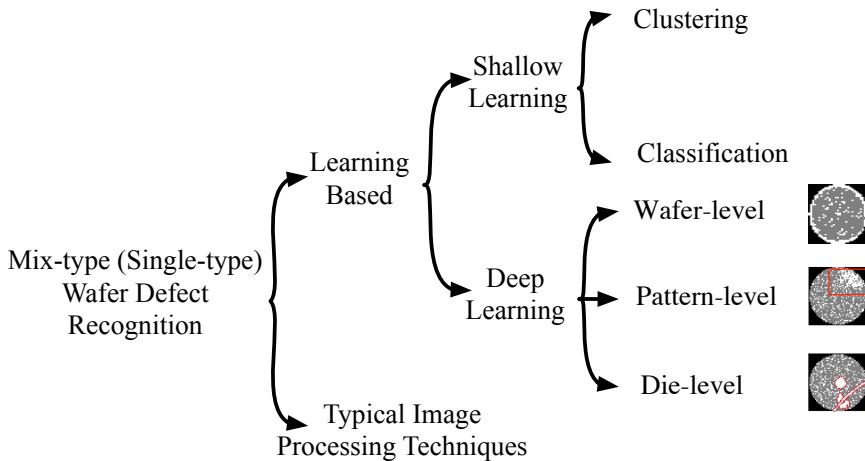
- Single-type defect patterns emerge and are coupled and shaped mixed-type patterns



- Some wafer map patterns in `MixedWM38` benchmark:
- (a) Center; (b) Scratch; (c) Location; (d) Edge-Location;
  - (e) 2 single-type defects mixed (Center, Scratch);
  - (f) 2 single-type defects mixed (Scratch, Location);
  - (g) 3 single-type defects mixed (Center, Scratch, and Location);
  - (h) 4 single-type defects mixed (Center, Scratch, Location, and Edge-Location).

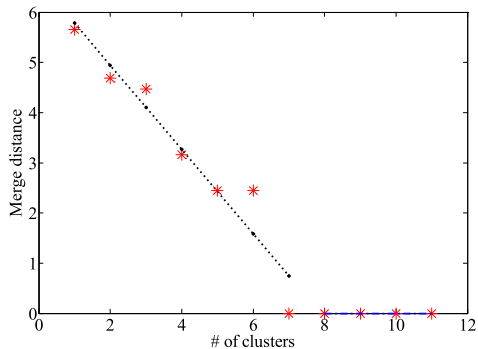


The General Wafer Defect Pattern Recognition Flow.

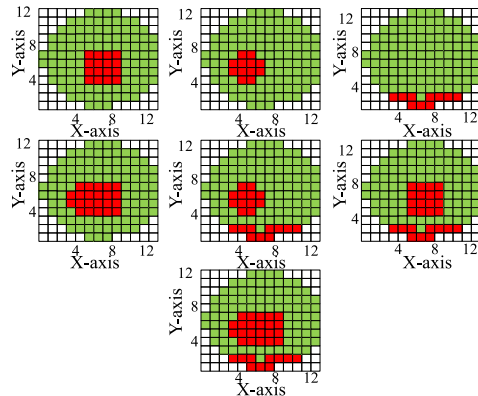


The taxonomy of prior arts.

# Shallow Learning-based Recognition Paradigm



(a)



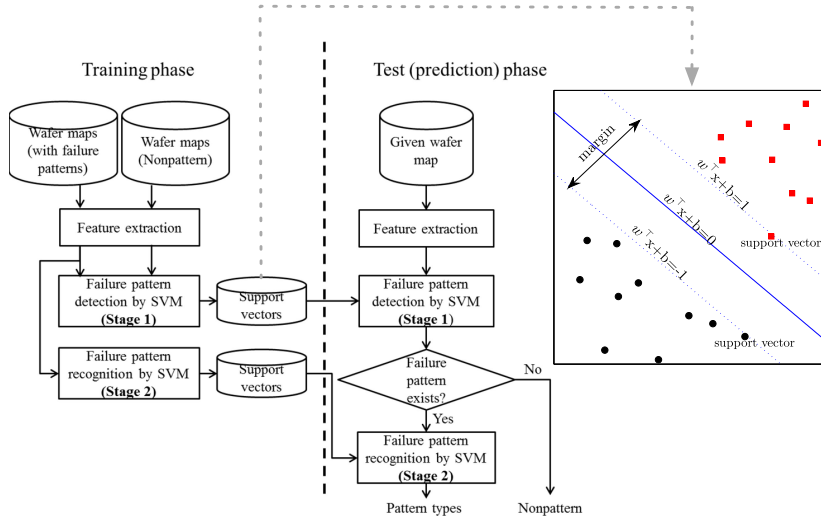
(b)

An example of clustering-based method. <sup>1</sup>

<sup>1</sup>M. B. Alawieh et al., "Identifying wafer-level systematic failure patterns via unsupervised learning," IEEE TCAD, 2017.



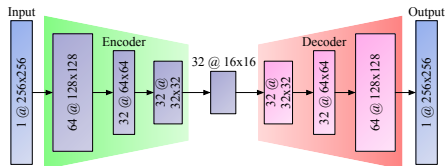
# Typical Classification-based Methods



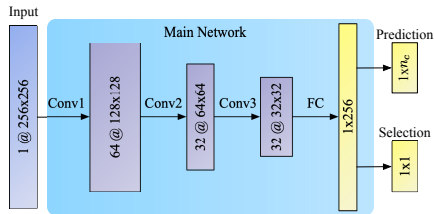
An example of typical classification-based method. <sup>1</sup>

<sup>1</sup>M.-J. Wu et al., "Wafer map failure pattern recognition and similarity ranking for large-scale data sets," IEEE TSM, 2015.

# Deep Learning-based Recognition Paradigm



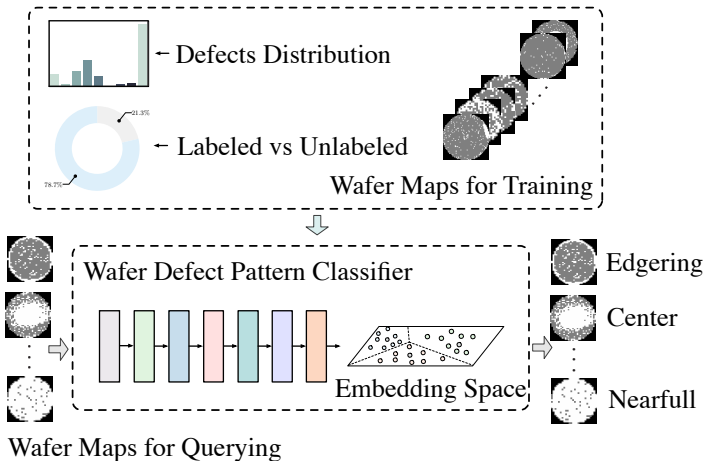
(a)



(b)

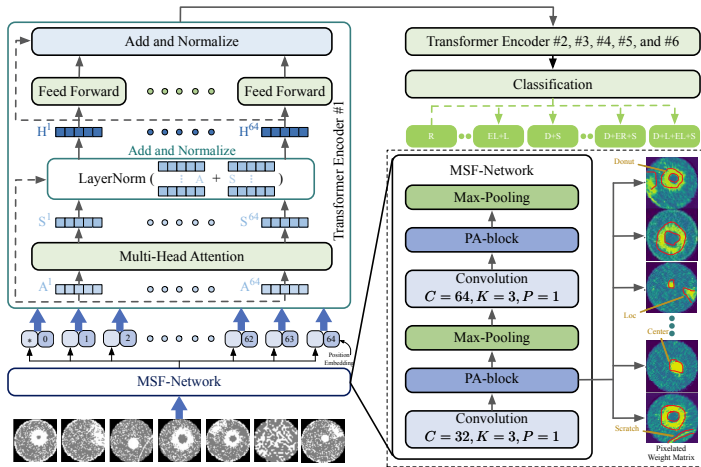
The illustration of the data augmentation and selective wafer defect recognition network. <sup>1</sup>

<sup>1</sup>M. B. Alawieh et al., "Wafer map defect patterns classification using deep selective learning," DAC, 2020.



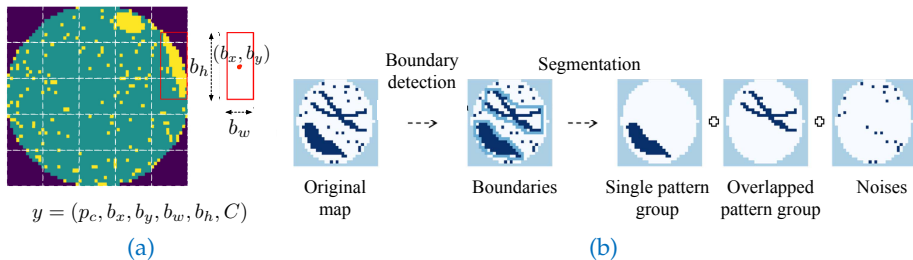
The proposed semi-supervised wafer failure pattern classifier. <sup>1</sup>

<sup>1</sup>H. Geng et al., "When wafer failure pattern classification meets few-shot learning and self-supervised learning," ICCAD, 2021.



The architecture of the transformer-based defect recognition. <sup>1</sup>

<sup>1</sup>Y. Wei et al., "Mixed-type wafer defect recognition with multi-scale information fusion transformer," IEEE TSM, 2022.



(a) An example of pattern-level recognition. <sup>1</sup>

(b) The segmentation example for the wafer defect detection. <sup>2</sup>

<sup>1</sup> P. P. Shinde et al., "Wafer defect localization and classification using deep learning techniques," IEEE Access, 2022.

<sup>2</sup> Y. Kong et al., "Qualitative and quantitative analysis of multi-pattern wafer bin maps," IEEE TSM, 2020.

# Conclusion & Future Directions

- A survey of recent line of arts in wafer failure pattern recognition
- The conflict between the security of wafer information and the development of a learning-based method
- Rethinking deep learning-based algorithms: susceptible to perturbations, prior information incorporation, ...
- Considering extracting and fusing multi-level features from wafer-level to die-level
- ... ..





**THANK YOU!**