CENG4480 Homework 3

Due: Dec. 09, 2018

Q1 Given the 6T-SRAM cell as in Figure 1, discuss the reading behavior (i.e., reading steps) if originally A = 1, A_b = 0.

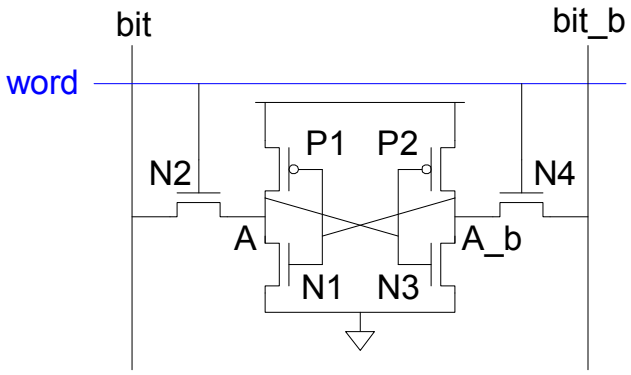


Figure 1: 6T-SRAM cell structure.

Q2 What is the modern memory hierarchy? Analysis the properties of each hierarchy level.

Q3 For the given SR Latch in Figure 2. Assume the initial state of $\bar{Q}$ is 1. Try to draw the waveform of Q if S, R, and E(Clk) have shown in Figure 3.

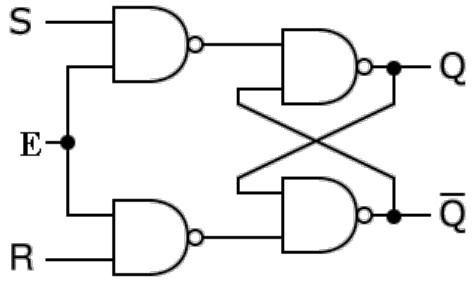


Figure 2: Gated SR Latch.

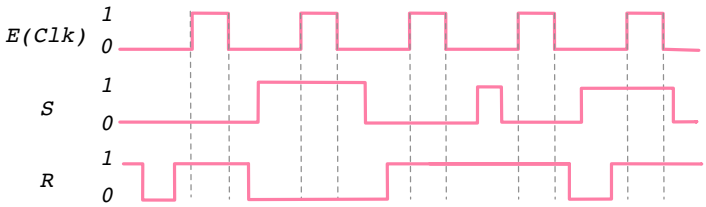
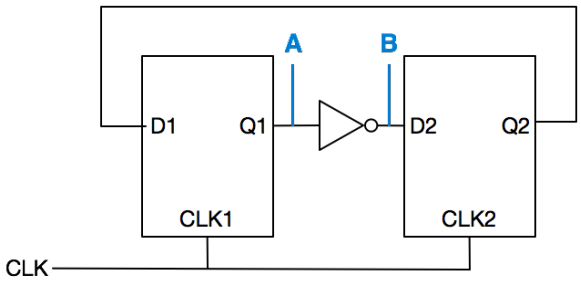


Figure 3: Gated SR Latch.

Q4 Design a finite state machine to detect the pattern of "11001" in the bit stream. How many states are required? Draw the state transition graph.

Q5 A digital clock is important in circuit design. Please answer the following **three** questions.

(a) Given the following circuit, CLK1 = CLK2 = 25MHz; Tff = 5ns; Tsetup = 5ns. The gate delay TG = 10ns. Please calculate the time margin. Note: Tff= delay of a flip flop, Tsetup=setup time of a flip flop, and TG is delay of a gate.



(b) In the above circuit, currently there is already one delay gate with delay TG. How many more similar delay gates can you insert between A and B without creating error?

(c) Sometimes we can take advantage of clock skew. For the above circuit, if the delay from CLK to CLK2 is 4ns, calculate the minimal clock period of the clock CLK.