Binary Sequences for Multiple Access Collision Channel: Identification and Synchronization

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***Abstract*—In this paper we investigate the identification and synchronization problems on a multiple access collision channel. Following Massey's lead, solutions to these problems are addressed by protocol sequences. This paper considers two different levels of user synchroneity: frame-synchronous access and slot-synchronous access. For the identification problem, we study user-detectable sequences. These are sequences with the cross-correlation property that allows each active user be detected within a bounded delay basing only on the channel activity information observed. Furthermore, we investigate the synchronization problem for delay-detectable sequences under the slot-synchronous access assumption. The goal of the synchronization problem is to determine the offset relations among all the active users. Sequences that allow such determination can be viewed as a special subset of user-detectable sequences. For both of these sequence families, it is desirable that the sequence length should be as short as possible. Hence, it is important to derive the minimum sequence lengths for these respective families. This is an extremely difficult open problem. Nevertheless, lower and upper bounds on these minimum lengths are presented in this paper under different levels of synchroneity assumptions. In addition, the performance of these sequences is demonstrated via numerical simulation.**

***Index Terms*—Collision channel without feedback, protocol sequences, superimposed code, user-irrepressible sequences, optical orthogonal code.**

I. Introduction

A. Motivation

MASSEY and Mathys introduced a model of the multiple access collision channel without feedback in [1] and [2]. The model involves T potential users aiming to transmit to a single receiver over a time-slotted channel. It is assumed that at most M ($M \leq T$) users may be active at the same time. The signal transmitted by each user is modeled by a fixed-length packet, which occupies exactly one time slot. If two or more users send simultaneously, a collision occurs and all involved packets are lost. If exactly one user transmits, the packet can be received correctly.

In multiple access transmission, three tasks are commonly encountered [3]–[6]:

(i) to detect active users (identification),
(ii) to determine the sender and value of each successful received packet (decoding), and
(iii) to find their delay offsets (synchronization).

In this paper we investigate the identification problem and the identification-cum-synchronization problem on a collision channel. The latter is also known as *signature coding*. Since this paper does not deal with the coding/decoding issues, we will assume that there is no user payload in a packet. This is not simply a matter of convenience. In fact, in the next subsection we present applications examples which require no user payload and can be modeled as a signature coding problem. In such a model, at each time slot each user either transmits a signal pulse or else remains silent. So the length of a packet in a time slot can be regarded as 1 bit and we can define the channel-activity signal of the collision channel, $c(t)$, as follows:

$$c(t) = \begin{cases} 0 & \text{if no user transmits at slot } t, \\ 1 & \text{if exactly one user transmits at slot } t, \\ * & \text{if more than one user transmit at slot } t. \end{cases}$$

As presented in [3]–[5], the identification and synchronization problems are addressed by assigning each user a distinct deterministic binary sequence rather than random coding. We call it a protocol sequence [2]. An active user transmits if the value "1" is read in the assigned sequence and keeps silent if "0" is read. It is possible for an active user to become inactive and vice versa. However, we assume that an inactive user must remain inactive for at least the length of a protocol sequence before becoming active. It is noted that such solution also applies in the OR channel paper [7] as well as for the signature coding papers [6], [8], [9]. In this paper, we use the word "length" and "period" of a sequence interchangeably.

Furthermore, the following two different levels of synchroneity are studied:

(i) Frame-synchronous access: each active user starts its sequence period at the same slot;
(ii) Slot-synchronous access: each active user starts its sequence period at the beginning of a time slot that is chosen randomly so that the offset delay between any two overlapping active users is uniformly distributed.

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To the authors' knowledge, in the literature there is no study on the minimum length of sequences which can be used to address the identification and synchronization problems of a collision channel. This paper is an attempt to investigate the lower and upper bounds of the minimum length under frame-synchronous or slot-synchronous access assumption. Effects of the assumption on synchroneity are also examined.

B. Applications

The identification problem plays a fundamental role in many practical scenarios, some of which relating to wired communication were mentioned in [8], [9]. More examples can be found in [9] including file retrieval, login in mobile telecommunications systems and non-adaptive hypergeometric group testing.

Sensor alarm. Consider an area monitored by a sensor network which consists of several alarm sensors and one data sink. If one or more intruders enter the area, multiple alarms may be triggered. Solving the identification problem arising from the sensor signature coding problem enables the data sink to determine more precisely the locations where the intrusions have occurred.

Another interesting potential application of the identification problem is multilevel expurgated pulse-position modulation (MEPPM) [10] for visible light communications (VLC).

MEPPM. In MEPPM for VLC, the low-cost LED is exploited. Balanced incomplete block designs (BIBD) are used to construct the symbol alphabet of an LED array. It is assumed that all LEDs are frame-synchronous. The receiver can distinguish multiple power levels of light intensity and its task is to demodulate the received signal to the original BIBD codewords. In a collision channel the receiver can detect three levels of energy: $\{0, 1, *\}$. Thus the identification problem in a frame-synchronous system discussed in this paper can be employed to address the MEPPM decoding.

For the synchronization problem, one application is target tracking by detecting energy pulses coming from multiple distributed sources. This application was introduced in [5].

Tracking. In a multi-static radar system, each transmitting source sends multiple pulses according to its assigned protocol sequence. If the sequences have the synchronization ability, then the detector can capture the exact sending time of each transmitting source's pulse train. The information can be utilized for more accurate tracking of the targets.

C. Related Work

For a collision channel, there is no study focusing merely on the identification and synchronization problems. They are usually investigated together with packet decoding. (See [3]–[5], [11], [12].) L. Györfi and S. Györi presented asymptotic lower and upper bounds on the minimum sequence length for frame-synchronous access in [11]. They further gave the bounds for slot-synchronous access in [12]. However, the proof relies on the random coding rather than deterministic protocol sequences and thus the results only hold for T approaching infinity. References [3]–[5] provided several concrete constructions for slot-synchronous access, but decoding and throughput are the primary objects of investigation.

The notion of identification under frame-synchronous access is also addressed in another context for an OR channel, under the name superimposed code [8] and cover-free families [13]. There are only two values, 0 and 1, in the channel-activity signal of the OR channel considered signifying whether a time slot contains no entry of value "1" or at least one such entry. Interested readers are referred to [9] for a survey of known results in the literature. The same problem has also been extensively studied in the adder channel [14], [15] in which a tight asymptotic lower bound $2M/\log M$ on the minimum sequence length was established. The channel-activity signal of an adder channel includes different $M+1$ integers signifying exactly the number of transmitted users in a time slot. From the channel-activity signal, one sees both of these problems are very different from the identification problem under frame-synchronous access for a collision channel as discussed here. For slot-synchronous access, an asymptotic upper bound for T approaching infinity on minimum sequence length was derived in [6] for both the synchronization and identification problems in an OR channel.

D. Key Contributions

The special case $T = M \geq 2$ is considered in this paper, as adopted in [2]. For the identification problem, our goal is to find protocol sequences that allow any user be detected from the channel-activity signal if and only if it has become active. Such a protocol sequence set is said to be user-detectable (UD). For the synchronization problem, a sequence set is said to be delay-detectable (DD) if it allows the relative delay offset of any active user be detected from the channel-activity signal. We note that the synchronization problem is trivially solved under the frame-synchronous access assumption, since all active users start their sequences at the same slot. In other words, a UD sequence set must be DD in this case.

The following are three major objects of this paper:

(i) $L_{syn}(M)$, the smallest sequence length of a UD sequence set for M users under the frame-synchronous assumption;
(ii) $L_{asyn}(M)$, the smallest length of a UD sequence set for M users under the slot-synchronous assumption;
(iii) and $L^d_{asyn}(M)$, the smallest length of a DD sequence set for M users under the slot-synchronous assumption.

We also summarize the key contributions as follows:

(1) In Section III, we establish a lower bound on $L_{syn}(M)$. An upper bound and its corresponding construction are also given.
(2) Lower and upper bounds on $L_{asyn}(M)$ are presented in Section IV. In addition, we provide a detecting algorithm by which the receiver can detect each active user.
(3) In Section V, we establish an upper bound on $L^d_{asyn}(M)$. We also propose an algorithm for solving the synchronization problem.
(4) Simulation results are presented in Section VI in order to provide information on the performance of the proposed identification algorithm.

II. Definitions and Notations

Given a binary sequence $s(t)$, $t = 0, 1, \ldots, L-1$, of length L, we define its *Hamming weight* as $w(s) := \sum_{t=0}^{L-1} s(t)$. A

TABLE I
KEY NOTATIONS AND DEFINITIONS.

$w(s)$	The Hamming weight of s
$\mathcal{I}_s$	The characteristic set of s
$s^{(\tau)}$	The cyclic shift of s by τ
$s_1 \vee \ldots \vee s_M$	The logical OR of $s_1, s_2, \ldots, s_M$
$s_1 \preceq \bigvee_{i=2}^{M} s_i^{(\tau_i)}$	s_1 is blocked by $s_2, \ldots, s_M$
$s_1 \uplus \ldots \uplus s_M$	The erasure sum of $s_1, s_2, \ldots, s_M$
$H_{s_1 s_2}$	The Hamming crosscorrelation between s_1 and s_2
$H_{s_1 s_1}$	The Hamming autocorrelation of s_1

sequence set is said to be *constant-weight* if all sequences have the same Hamming weight.

Let the *cyclic shift* of a sequence s by relative shift τ be denoted by $s^{(\tau)}(t) := s(t-\tau)$. The subtraction $t-\tau$ is performed modulo L.

A sequence can also be represented by a *characteristic set* $\mathcal{I}$, which is defined as the set of all time indices in a period where the value of the protocol sequence is equal to 1. Cyclic shift of a sequence by integer τ is equivalent to adding τ modulo L to the corresponding characteristic set.

The *logical OR* of M binary sequences of length L is defined as a binary sequence of length L which has 0 in the k-th position where all sequences have 0 in this position, and 1 otherwise, for $k = 0, 1, \ldots, L-1$. We denote the logical OR of $s_1, s_2, \ldots, s_M$ by $s_1 \vee s_2 \vee \ldots \vee s_M$.

We write $s_1 \preceq (s_2 \vee \ldots \vee s_M)$ if $s_1 \vee s_2 \vee \ldots \vee s_M = s_2 \vee \ldots \vee s_M$. The sequence s_1 is said to be *blocked* by $s_2, s_3, \ldots, s_M$, if we can find delay offsets τ_i for $i = 2, \ldots, M$, such that $s_1 \preceq \bigvee_{i=2}^{M} s_i^{(\tau_i)}$.

The *erasure sum* of M binary sequences of length L is defined as a sequence of length L which has 0 in the k-th position where all sequences have 0 in this position, 1 if exactly one sequence has 1 in this position, and erasure symbol * otherwise, for $k = 0, 1, \ldots, L-1$. We denote the erasure sum of $s_1, s_2, \ldots, s_M$ by $s_1 \uplus s_2 \uplus \ldots \uplus s_M$.

Given two sequences $s_1(t)$ and $s_2(t)$, the Hamming crosscorrelation function between s_1 and s_2 is defined by

$$H_{s_1 s_2}(\tau) := \sum_{t=0}^{L-1} s_1(t) s_2(t-\tau).$$

If $s_1(t) = s_2(t)$, the crosscorrelation is reduced to the autocorrelation of s_1 or s_2.

We list the key notations and definitions of this section in Table I. For illustration, consider the following sequence set:

$$s_1 = [10101010]$$
$$s_2 = [11001100]$$
$$s_3 = [10111000].$$

The characteristic set is $\mathcal{I}_{s_1} = \{0, 2, 4, 6\}$, $\mathcal{I}_{s_2} = \{0, 1, 4, 5\}$ and $\mathcal{I}_{s_3} = \{0, 2, 3, 4\}$. We have $w(s_1) = w(s_2) = w(s_3) = 4$. Also $s_2^{(2)} = [00110011]$ and $s_1 \vee s_2^{(2)} = [10111011]$. Then we have $s_3 \preceq s_1 \vee s_2^{(2)}$ and thus s_3 is blocked by s_1 and s_2. One can also check that $s_1 \uplus s_2 = [*110*110]$ and $H_{s_1 s_2}(2) = 2$.

III. FRAME-SYNCHRONOUS ACCESS

We make the following formal definition of a UD sequence set under frame-synchronous access.

Definition 1. A set of M sequences is said to be UD under frame-synchronous access, if all erasure sums of up to M sequences are distinct, i.e.,

$$\biguplus_{i \in \mathcal{A}} s_i \neq \biguplus_{j \in \mathcal{B}} s_j \tag{1}$$

for any subsets $\mathcal{A}, \mathcal{B} \subseteq \{1, 2, \ldots, M\}$ and $\mathcal{A} \neq \mathcal{B}$.

By the above definition, a lower bound on sequence length can be computed simply by using the fact that since each erasure sum of at most M sequences must be distinct, the total number of erasure sums in a UD set cannot exceed the number of L-digit ternary numbers. The total number of erasure sums we need to distinguish is 2^M because all subsets are possible, while the total number of observable channel outputs is 3^L. Thus following $3^L \geq 2^M$ we have

$$L_{syn}(M) \geq \frac{\log 2}{\log 3} M \approx 0.631M.$$

To prove a tighter lower bound on $L_{syn}(M)$, we need the following definition and lemma.

Definition 2. Given a sequence set $\{s_1, s_2, \ldots, s_M\}$, if $s_i(k) = 1$ and the erasure sum of $\{s_1, s_2, ..., s_M\} \setminus \{s_i\}$ at the k-th position is equal to 0 or 1, then we say that the k-th position is *exceptional* for s_i. The collection of all exceptional positions of s_i is denoted by $\mathcal{E}_{s_i}$. Obviously, we have $\mathcal{E}_{s_i} \subseteq \mathcal{I}_{s_i}$.

Lemma 1. *If a sequence set $\mathcal{S} = \{s_1, s_2, \ldots, s_M\}$ is UD under frame-synchronous access, then we have*

(i) $|\mathcal{E}_{s_i}| \geq 1$ for any i;
(ii) $\mathcal{E}_{s_i} \neq \mathcal{E}_{s_j}$ for any $i \neq j$.

Proof: (i) Suppose $|\mathcal{E}_{s_i}| = 0$, i.e., for all t such that $s_i(t) = 1$ the erasure sum of remaining sequences at time t is $*$, then the following result holds:

$$\biguplus_{u \in \{1,2,\ldots,M\} \setminus \{i\}} s_u = \biguplus_{u \in \{1,2,\ldots,M\}} s_u.$$

This contradicts the definition of UD sequences for frame-synchronous access in (1).

(ii) Suppose $\mathcal{E}_{s_i} = \mathcal{E}_{s_j}$ for some $i \neq j$. Let e_i be the erasure sum

$$e_i := \biguplus_{u \in \{1,2,\ldots,M\} \setminus \{i\}} s_u$$

and e_j be the erasure sum

$$e_j := \biguplus_{u \in \{1,2,\ldots,M\} \setminus \{j\}} s_u.$$

We will show that the sequence set $\mathcal{S}$ is not UD by proving $e_i = e_j$. Obviously, we have $e_i(t) = e_j(t)$ if t is not in $\mathcal{I}_{s_i} \cup \mathcal{I}_{s_j}$. For $t \in \mathcal{I}_{s_i} \cup \mathcal{I}_{s_j}$, we have

$$e_i(t) = e_j(t) = \begin{cases} 1 & \text{if } t \in \mathcal{E}_{s_i} = \mathcal{E}_{s_j}, \\ * & \text{if } t \in \mathcal{I}_{s_i} \setminus \mathcal{E}_{s_i} \text{ or } t \in \mathcal{I}_{s_j} \setminus \mathcal{E}_{s_j}. \end{cases}$$

This completes the proof of Lemma 1. ■

Example 1: The following is a UD sequence set under frame-synchronous access with $M = 3, L = 3$.

$$s_1 = [101]$$
$$s_2 = [111]$$
$$s_3 = [011]$$

The first position is exceptional for both s_1 and s_2. The second is exceptional for both s_2 and s_3. The third is not exceptional for any sequence. One can check its structure is in accordance with Lemma 1.

We can establish the next theorem by means of Lemma 1.

Theorem 2. *For any $M \geq 2$,*

$$L_{syn}(M) \geq \frac{2M}{3}.$$

Proof: Denote $|\bigcup_{i\in\{1,2,\ldots,M\}} \mathcal{E}_{s_i}|$ by $n_{\mathcal{E}}$. Let h be the number of the sequences which all have exactly one exceptional position. Then following (i) of Lemma 1 and the definition of exceptional position we have

$$\sum_{i\in\{1,2,\ldots,M\}} |\mathcal{E}_{s_i}| \geq h + 2(M-h). \tag{2}$$

On another hand, we also have

$$\sum_{i\in\{1,2,\ldots,M\}} |\mathcal{E}_{s_i}| \leq 2n_{\mathcal{E}}. \tag{3}$$

This inequality follows from the fact that the exceptional positions of all the sequences are located in $\bigcup_{i\in\{1,2,\ldots,M\}} \mathcal{E}_{s_i}$ and one exceptional position is occupied by at most two sequences simultaneously. After substituting (3) into (2), we further obtain

$$h \geq 2M - 2n_{\mathcal{E}}. \tag{4}$$

Next we derive an upper bound on h. Suppose $h \geq n_{\mathcal{E}} + 1$. By pigeonhole principle we always can find $\mathcal{E}_{s_i} = \mathcal{E}_{s_j}$ for some $i \neq j$. It contradicts (ii) of Lemma 1 and thus we have

$$h \leq n_{\mathcal{E}}. \tag{5}$$

After combining (4) and (5), we obtain $n_{\mathcal{E}} \geq 2M/3$. It implies $L \geq 2M/3$, since the length must be not smaller than $n_{\mathcal{E}}$. ■

For upper bound on $L_{syn}(M)$, we show a trivial construction for M users with length $L = M$: for $i = 1, 2, \ldots, M$, let $s_i(t) = 1$ if and only if $t = i$. This sequence set enjoys the property (1), and thus we have

$$L_{syn}(M) \leq M$$

which is also the tight upper bound in OR channel [16]. To close the gap between $2M/3$ and M for a collision channel is an interesting direction for future works.

IV. Identification for Slot-Synchronous Access

In subsequent discussion, we make use of the following formal definition of UD sequences under slot-synchronous access.

Definition 3. A set which has M sequences of length L is said to be UD under slot-synchronous access, if every erasure sum of up to M sequences of any relative shifts is distinct from every other sum of M or fewer sequences of any relative shifts, i.e.,

$$\biguplus_{i\in\mathcal{A}} s_i^{(\tau_i)} \neq \biguplus_{j\in\mathcal{B}} s_j^{(\tau_j)} \tag{6}$$

for any subsets $\mathcal{A}, \mathcal{B} \subseteq \{1, 2, \ldots, M\}$, $\mathcal{A} \neq \mathcal{B}$, $|\mathcal{A}| \geq |\mathcal{B}|$ and any integer $\tau_1, \tau_2, \ldots, \tau_M$. The defining property (1) under frame-synchronous access is a special case of (6) with $\tau_1 = \tau_2 = \ldots = \tau_M = 0$.

The objective of computing the minimum delay is complicated. In order to provide a deeper understanding of it, we present in this section lower and upper bounds on $L_{asyn}(M)$.

A. Lower Bound on Minimum period

We obtain $L_{asyn}(2) \geq 2$ from Theorem 2 since frame-synchronous access is a special case of slot-synchronous access. The lower bound in this case can be achieved through assigning $s_1 = [11], s_2 = [10]$. Furthermore, we will use the following result from [17] to derive a lower bound on $L_{asym}(M)$ for $M > 2$.

Theorem 3. [17] *Let $\mathcal{S}'$ be a set of M' (not necessarily constant-weight) binary sequences of length L. If $L < 8(M')^2/9$, then there exist the relative delay offsets of the sequences such that the sequence with minimum Hamming weight in $\mathcal{S}'$ is blocked by the other sequences in $\mathcal{S}'$.*

From Theorem 3, we can deduce

Theorem 4. *For any $M \geq 3$, we have*

$$L_{asyn}(M) \geq \frac{8\lceil M/2\rceil^2}{9}.$$

Proof: Let $\mathcal{S}$ be a sequence set consisting of sequences $s_1, s_2, \ldots, \ldots, s_M$, with sequence length strictly less than $8\lceil M/2\rceil^2/9$. After re-labeling the sequences if necessary, we assume without loss of generality that s_1 is a sequence of minimum Hamming weight in $\mathcal{S}$.

Let M' be the the integer $\lceil M/2\rceil$, and consider the sequences $s_1, s_2, \ldots, s_{M'}$. By Theorem 3, we can arrange the relative delay offsets of these M' sequences such that s_1 is blocked by some shifted versions of $s_2, \ldots, s_{M'}$, i.e., there exist $\tau_2, \tau_3, \ldots, \tau_{M'}$ such that

$$s_1 \preceq s_2^{(\tau_2)} \vee s_3^{(\tau_3)} \vee \cdots \vee s_{M'}^{(\tau_{M'})}.$$

Likewise, if we apply Theorem 3 to sequences

$$s_1, s_{M'+1}, s_{M'+2}, \ldots, s_M,$$

we can find relative delay offsets $\tau_{M'+1}, \tau_{M'+2}, \ldots, \tau_M$ such that

$$s_1 \preceq s_{M'+1}^{(\tau_{M'+1})} \vee s_{M'+2}^{(\tau_{M'+2})} \vee \cdots \vee s_M^{(\tau_M)}.$$

Hence, the erasure sum

$$s_1 \uplus s_2^{(\tau_2)} \uplus s_3^{(\tau_3)} \uplus \cdots \uplus s_M^{(\tau_M)}$$

is the same as the erasure sum

$$s_2^{(\tau_2)} \uplus s_3^{(\tau_3)} \uplus \cdots \uplus s_M^{(\tau_M)}.$$

This violates the property (6) and thus proves that the sequence set $\mathcal{S}$ is not UD under slot-synchronous access. ■

Example 2: One can check the following sequence set with $M = 3$, $L = 4$:

$$s_1 = [1100]$$
$$s_2 = [1010]$$
$$s_3 = [1110]$$

is UD under slot-synchronous access, and its sequence length achieves the minimum value for $M = 3$ in Theorem 4.

B. Upper Bound on Minimum period

In this subsection, we will show some special classes of sequence sets that are UD under slot-synchronous access. We need to recall the following definition:

Definition 4. A sequence set is said to be *user-irrepressible* (UI) [18] if each sequence is not blocked by other sequences no matter what the relative offsets are.

Theorem 5. *A sequence set is UD under slot-synchronous access if it is UI.*

Proof: Suppose that a set of M sequences is UI but not UD under slot-synchronous access. Then there exist two subsets $\mathcal{A} = \{s_{i_1}, s_{i_2}, \ldots, s_{i_k}\} \neq \{s_{j_1}, s_{j_2}, \ldots, s_{j_l}\} = \mathcal{B}$ such that

$$s_{i_1}^{(\tau_{i_1})} \uplus s_{i_2}^{(\tau_{i_2})} \uplus \ldots \uplus s_{i_k}^{(\tau_{i_k})} = s_{j_1}^{(\tau_{j_1})} \uplus s_{j_2}^{(\tau_{j_2})} \uplus \ldots \uplus s_{j_l}^{(\tau_{j_l})}$$

for some $\{\tau_{i_1}, \tau_{i_2}, \ldots, \tau_{i_k}\}$ and $\{\tau_{j_1}, \tau_{j_2}, \ldots, \tau_{j_l}\}$. It implies

$$s_{i_1}^{(\tau_{i_1})} \vee s_{i_2}^{(\tau_{i_2})} \vee \ldots \vee s_{i_k}^{(\tau_{i_k})} \preceq s_{j_1}^{(\tau_{j_1})} \vee s_{j_2}^{(\tau_{j_2})} \vee \ldots \vee s_{j_l}^{(\tau_{j_l})}.$$

Due to $\mathcal{A} \neq \mathcal{B}$ and $|\mathcal{A}| \geq |\mathcal{B}|$, we can always find a sequence, say s_u, $s_u \in \mathcal{A}$ but $s_u \notin \mathcal{B}$, such that

$$s_u^{(\tau_u)} \preceq s_{j_1}^{(\tau_{j_1})} \vee s_{j_2}^{(\tau_{j_2})} \vee \ldots \vee s_{j_l}^{(\tau_{j_l})}.$$

This contradicts the definition of UI sequence set. Thus a UI sequence set must be UD under slot-synchronous access. ■

By means of Theorem 5, UD sequences under slot-synchronous access can be designed relying on the UI property. We introduce the shortest known general constructions below, which are both based on the Chinese remainder theorem (CRT). The mapping $f : \mathbb{Z}_{pq} \to \mathbb{Z}_p \oplus \mathbb{Z}_q$ defined by $f(a) := (a \bmod p, a \bmod q)$ is a bijection from $\mathbb{Z}_{pq}$ to $\mathbb{Z}_p \oplus \mathbb{Z}_q$ when p and q are relatively prime [19], and preserves addition and multiplication by integers.

CRT Construction [20]: Given M, we set q to be $2M-1$, and p any prime larger than or equal to M and relatively prime to $2M-1$. For $j = 0, 1, \ldots, M-1$, we let $\mathcal{I}'_{s_j} := \{(jy, y) \in \mathbb{Z}_p \oplus \mathbb{Z}_{2M-1} : y = 0, 1, \ldots, M-1\}$ and obtain the characteristic sets $\mathcal{I}_{s_j}$, by taking the inverse image $f^{-1}(\mathcal{I}'_{s_j})$ for $j = 0, \ldots, M-1$. These M sequences compose a constant-weight UI sequence set.

CRT$_p$ Construction [17]: This construction is a variation of CRT construction. We set p any prime larger than or equal to M and q to be $2p-2$. We let $\mathcal{I}'_{s_0} := \{(y, 0) \in \mathbb{Z}_p \oplus \mathbb{Z}_{2p-2} : y = 0, 1, \ldots, p-1\}$ and $\mathcal{I}'_{s_j} := \{(jy, y) \in \mathbb{Z}_p \oplus \mathbb{Z}_{2p-2} : y = 0, 1, \ldots, p\}$ for $j = 1, \ldots, M-1$. These M sequences form a UI sequence set, but not constant-weight.

TABLE II
THE SHORTEST KNOWN PERIOD OF UI SEQUENCES

M	Shortest known period
$2 \leq M \leq 6$	2^M
$M = 7$	84
$M = 8$	153
$M \geq 9$, non-prime M	$p_M(2M-1)$
$M \geq 9$, prime M	$p_M(2p_M-2)$

The following upper bound is guaranteed by the CRT and CRT$_p$ constructions.

Theorem 6. *Let p_M denote the smallest prime larger than or equal to M. For any $M \geq 3$, we have*

$$L_{asyn}(M) \leq \min\big(p_M(2M-1), p_M(2p_M-2)\big).$$

For $2 \leq M \leq 6$, the shift-invariant property [21] produces the shortest known UI set of the period 2^M. For $M = 8$, the shortest known period is obtained by computer searching. However, in the other cases, CRT and CRT$_p$ constructions yield the shortest known sequence length for non-prime M and prime M, respectively. We list them in Table II.

We have proved in [17] that the period of UI sequence set with M sequences is at least $8M^2/9$. Thus UD sequence sets under slot-synchronous access which are not UI with sequence length between $8\lceil M/2 \rceil^2/9$ and $8M^2/9$ may be a potential direction for seeking sequence sets with shorter period. One can check the sequence set in Example 2 is UD under slot-synchronous access, but not UI.

C. Detecting Algorithm

Definition 5. We say that $c(t)$ is *matched* to s_i at time t_0 if $\forall t = 0, 1, \ldots, L-1$, $s_i(t) = 1 \Rightarrow c(t_0 + t) = 1$ or $*$. Let α_i be the smallest integer such that $s_i(t) = 0$ if $\alpha_i < t \leq L-1$. The *starting time* t_i^s is used to denote the time index when user i becomes active, i.e., begins to send its sequence. The *ending time* $t_i^s + \alpha_i$ represents the time index of the last bit 1 in a sequence period of user i. The *alarming time* t_i^a ($t_i^a \geq t_i^s$) is the time index when the first matching of user i is detected by the receiver.

We now introduce the detecting algorithm used for a UI sequence set. The receiver observes the channel all the time and tracks the set of active users by M Boolean variables $active_i$ for $i = 1, 2, \ldots, M$. The values are set to `FALSE` initially. In each slot, the receiver checks whether $c(t)$ is matched to s_i or not. To determine whether $c(t)$ is matched to s_i at some time index t_0, it is necessary for the receiver to know all values of $c(t_0), c(t_0+1), \ldots, c(t_0+\alpha_i)$. The receiver would make the decision at $t_0+\alpha_i$. If there is a matching at t_0, then $active_i$ is set to `TRUE`. Otherwise, we would set $active_i$ as `FALSE`. In other words, whether there is a matching with $s_i(t)$ is determined slot by slot through a sliding window of $\alpha_i + 1$ slots. We summarize the procedure in Algorithm 1.

Theorem 7. *Assign a UI sequence set of M sequences to user 1 to M. Then under slot-synchronous access Algorithm 1 can*

Algorithm 1 Detecting algorithm for a UI sequence set

```
for i = 1, 2, ..., M do
  for t_0 = 0, 1, 2, ... do
    if c(t) is matched to s_i(t) at t_0 then
      active_i ← TRUE
    else
      active_i ← FALSE
    end if
  end for
end for
```

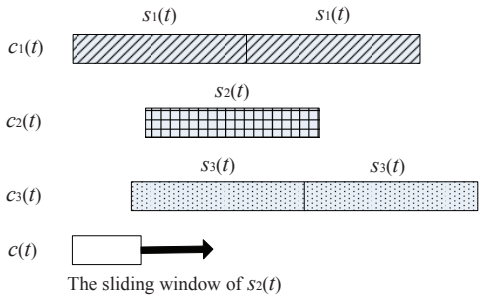

Fig. 1. The receiver tries to match $c(t)$ with s_2.

successfully identify user i not later than $t_i^s + \alpha_i$ if and only if user i becomes active at t_i^s.

Proof: Consider user i and its assigned sequence s_i. Let it become active at t_i^s. Suppose there exists a matching of s_i at t_0 with $t_0 > t_i^s + \alpha_i$ or $t_0 < t_i^s - \alpha_i$. By the condition of t_0, we know user i actually does not transmit in the time interval $[t_0, t_0 + \alpha_i]$. Hence we find all non-zeros in $[t_0, t_0 + \alpha_i]$ are contributed by some other users. By the definition of matching, we further obtain that s_i can be blocked by other sequences, which contradicts the condition that the assigned sequence set is UI. Thus the matching of s_i can only possibly exist in $[t_i^s - \alpha_i, t_i^s + \alpha_i]$. This suffices to show that user i would be identified by Algorithm 1 only if it has become active. On another hand, the receiver can always find $c(t)$ is matched to $s_i(t)$ at t_i^s, i.e., identify user i at $t_i^s + \alpha_i$. Therefore we can conclude that Algorithm 1 can successfully identify the active user i with α_i slots delay in the worst case. ∎

Example 3: By the CRT construction, for $M = 3$ we can design the UD sequence set under slot-synchronous access with $L = 15$ below:

$$s_1 = [100000100000100]$$
$$s_2 = [111000000000000]$$
$$s_3 = [100010001000000].$$

If the starting time of these users are $0, 6$ and 5, respectively, we have the following case to make the user-detection. Sequence periods are indicated by underbrace.

User 1: $\underbrace{100000100000100100000100000100}000000$

User 2: $000000\underbrace{111000000000000}000000000000000$

User 3: $00000\underbrace{100010001000000100010001000000}$

$c(t)$: $100001\overline{\underline{*111}}00110100001100100110000000$

One can check $c(t)$ is matched to $s_2(t)$ at $t = 5, 6, 7$, respectively, which are indicated by underline. Since $\alpha_2 = 2$, the receiver would set $active_2$ as TRUE when $t = 7, 8, 9$, which are indicated by overline. Thus the receiver cannot know the exact starting time of user 2. The detecting procedure is presented in Fig. 1.

V. Synchronization for Slot-Synchronous Access

We present the formal definition of DD sequence set under slot-synchronous access as follows.

Definition 6. A set which has M sequences of length L is said to be DD under slot-synchronous access, if every erasure sum of up to M sequences of some relative shift is distinct from (i) the same sequence set with any other relative shift and (ii) every other sum of M or fewer sequences of any relative shifts, respectively, i.e.,

$$\biguplus_{i\in\mathcal{A}} s_i^{(\tau_i)} \neq \biguplus_{j\in\mathcal{B}} s_j^{(\tau_j')} \tag{7}$$

for any subsets $\mathcal{A}, \mathcal{B} \subseteq \{1, 2, \ldots, M\}$ with $|\mathcal{A}| \geq |\mathcal{B}|$ and any integer τ_1, τ_1', τ_2, τ_2', …, τ_M, τ_M', such that $\mathcal{A} \neq \mathcal{B}$ or $\mathcal{A} = \mathcal{B}$ with $\{\tau_i : \forall i \in \mathcal{A}\} \neq \{\tau_j' : \forall j \in \mathcal{B}\}$. Obviously, the UD property under slot-synchronous access is a special case here by setting $\mathcal{A} \neq \mathcal{B}$ in (7).

As a DD sequence set must be UD under slot-synchronous access, Theorem 4 gives us a lower bound on $L_{asyn}^d(M)$ too. In this section we focus on its upper bound.

A. Upper Bound on Minimum Period

In order to obtain an upper bound on $L_{asyn}^d(M)$, a sufficient condition for the DD property is presented below.

Theorem 8. *A sequence set is DD under slot-synchronous access if any sequence is not blocked by other sequences and its non-zero shifted version, i.e.,*

$$s_i \not\preceq \bigvee_{j\in\{1,2,\ldots,M\}} s_j^{(\tau_j)} \tag{8}$$

for any i and any τ_j with $\tau_i \neq 0$.

Proof: We prove this theorem by contradiction. Suppose a sequence set satisfying (8) is not DD. Then for some $\mathcal{A} \neq \mathcal{B}$ or $\mathcal{A} = \mathcal{B}$ with $\{\tau_i : \forall i \in \mathcal{A}\} \neq \{\tau_j' : \forall j \in \mathcal{B}\}$ we can find

$$\biguplus_{i\in\mathcal{A}} s_i^{(\tau_i)} = \biguplus_{j\in\mathcal{B}} s_j^{(\tau_j')}. \tag{9}$$

In the case of $\mathcal{A} \neq \mathcal{B}$, the equation (9) implies we can find one sequence, labeled as s_g, $g \in \mathcal{A}$, $g \notin \mathcal{B}$, such that $s_g^{(\tau_g)} \preceq \bigvee_{j\in\mathcal{B}} s_j^{(\tau_j')}$ since $s_g^{(\tau_g)} \preceq \bigvee_{i\in\mathcal{A}} s_i^{(\tau_i)} \preceq \bigvee_{j\in\mathcal{B}} s_j^{(\tau_j')}$. This further implies

$$s_g \preceq \bigvee_{j\in\mathcal{B}} s_j^{(\tau_j'-\tau_g)}.$$

In the case of $\mathcal{A} = \mathcal{B}$, by the same reason we can also find a sequence, labeled as s_h, $h \in \mathcal{A}, \mathcal{B}$, such that

$$s_h \preceq \bigvee_{j\in\mathcal{B}} s_j^{(\tau_j'-\tau_h)}$$

with $\tau_h \neq \tau'_h$.

The above two results both violate (8). Thus we conclude that any sequence set satisfying (8) must be DD. ■

Definition 7. A family of binary sequences of length L and Hamming weight w that satisfies the following two properties:

(i) the value of Hamming autocorrelation function of any sequence is not bigger than λ_a for any non-zero τ performed modulo L;

(ii) the value of Hamming crosscorrelation between any distinct two sequences is not bigger than λ_c for any τ,

is said to be an *optical orthogonal code* (OOC) $(L, w, \lambda_a, \lambda_c)$ [22].

Following Theorem 8, some known constructions of OOCs can be applied to design DD sequences if $w > (M-1)\lambda_c + \lambda_a$. We show here one example due to [23].

Theorem 9. [23] *Let p be any prime number and m any positive integer. Then there exists an $OOC(p^{2m}-1, p^m+1, 2, 2)$ with $p^m - 2$ codewords.*

Example 4: For $M = 4$, by setting $p = 2$ and $m = 3$ in Theorem 9, we obtain the following sequence set with $L = 63$:

$$\mathcal{I}_{s_1} = \{0, 4, 7, 17, 27, 30, 34, 39, 58\}$$
$$\mathcal{I}_{s_2} = \{0, 5, 8, 14, 15, 34, 53, 54, 60\}$$
$$\mathcal{I}_{s_3} = \{0, 8, 21, 22, 24, 26, 27, 40, 48\}$$
$$\mathcal{I}_{s_4} = \{0, 5, 10, 16, 28, 30, 43, 45, 57\}$$

which can be found DD under slot-synchronous access since $w = 2^3 + 1 > 3 \times 2 + 2$.

Next we single out a special case of Theorem 9 for general M and give an upper bound on $L^d_{asyn}(M)$ which is roughly equal to $4M^2$.

Theorem 10. *Let p_{2M} denote the smallest prime larger than or equal to $2M$. For any $M \geq 2$, we have*

$$L^d_{asyn}(M) \leq p^2_{2M} - 1.$$

Proof: By setting $m = 1$ in Theorem 9, we know there exists an $OOC(p^2_{2M}-1, p_{2M}+1, 2, 2)$ with M codewords as $p_{2M} - 2 \geq M$. Then we have $w = p_{2M} + 1 > (M-1)\lambda_c + \lambda_a$ by $\lambda_a = \lambda_c = 2$. Following Theorem 8, we thus obtain this OOC is DD under slot-synchronous access. The sequence length $p^2_{2M} - 1$ gives the upper bound in Theorem 10. ■

B. Detecting Algorithm

The following algorithm was proposed in [3], [5], but indeed can be applied for any sequence sets satisfying Theorem 8. The procedure is basically the same as that in Algorithm 1: sliding a window of $\alpha_i + 1$ slots until there is a matching with s_i. Let the integral variable $start_i$ represent the detection result when user i starts its new sequence period. If $c(t)$ is matched to s_i at t_0, then we have $start_i = t_0$. We summarize the procedure in Algorithm 2 below.

Algorithm 2 Detecting algorithm for DD sequence sets under slot-synchronous access satisfying Theorem 8

```
for i = 1, 2, ..., M do
    for t_0 = 0, 1, 2, ... do
        if c(t) is matched to s_i(t) at t_0 then
            start_i = t_0
        end if
    end for
end for
```

Theorem 11. *Assign a DD sequence set satisfying Theorem 8 to user 1 to M. Then under slot-synchronous access Algorithm 2 can determine the starting time of active user i at $t^s_i + \alpha_i$ if it becomes active at t^s_i.*

Proof: Consider that the starting time of active user i is t^s_i, and is calculated as t_0 by Algorithm 2. This implies the matching of s_i occurs at t_0. Suppose $t_0 \neq t^s_i$. Then we know all non-zeros in $c(t_0), \ldots, c(t_0 + \alpha_i)$ are contributed by other active sequences and a non-zero shifted version of s_i. Thus, we find s_i can be blocked by other sequences and its non-zero shifted version, which contradicts Theorem 8. We obtain that $t^s_i = t_0$, i.e., the exact starting time of user i can be determined by Algorithm 2. Furthermore, by the definition of matching, the matching of s_i at t^s_i can only be detected at $t^s_i + \alpha_i$. ■

Example 4 continued: Let the four users in Example 4 begin to transmit their sequences, respectively, at $t = 3, 7, 12, 25$. Then following Theorem 11, we know the receiver at the time index $3 + \alpha_1 = 61$ would detect the event that $c(t)$ is matched to s_1 at $t = 3$, i.e., $start_1 = 3$ by Algorithm 2.

VI. Performance Study

We are interested in the *latency* which is measured as the time duration from the starting time of an active user to its alarming time. Obviously, the latency is upper bounded by the sequence period, which has been investigated extensively in Section III-V. Recall that α_i is the smallest integer such that $s_i(t) = 0$ for all t if $\alpha_i < t \leq L-1$. Under frame-synchronous access, it is easy to see that the receiver knows that user i has become active exactly at $t^s_i + \alpha_i$. For synchronization under slot-synchronous access, by Theorem 11 we also obtain that the latency of user i is exactly α_i. However, for identification under slot-synchronous access, the alarming time of user i may be earlier than $t^s_i + \alpha_i$ following Algorithm 1 and Theorem 7. In order to explore the performance fluctuations of Algorithm 1, we thus investigate the latency in this case by simulation.

In the simulation study, we assume that there are M users and the CRT protocol sequences are used to specify their channel access permission time. Since users are not frame-synchronized, there will be various combinations of starting time. In the simulation, we assume that the relative time shift between two users is uniformly distributed in their encountered minimum period $L = p_M(2M-1)$.

Fig. 2 shows the starting time, alarming time and ending time of each user for $M = 10$ in a simulation running. It is observed that for most users the alarming time is equal to the ending time, i.e., the latency is equal to α_i. Here, we have $\{\alpha_i\}^{10}_{i=1} = \{198, 9, 193, 197, 191, 199, 195, 196, 192, 180\}$ from the CRT construction.

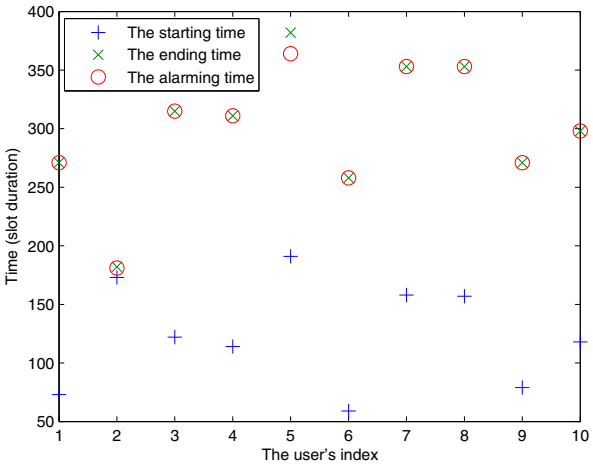

Fig. 2. The starting time, alarming time and ending time of each user in a simulation running for an identification problem with $M = 10$ under slot-synchronous access.

TABLE III
THE AVERAGE PERFORMANCE OF IDENTIFICATION UNDER SLOT-SYNCHRONOUS ACCESS.

M	ρ	$\overline{\delta}$	$\overline{\alpha}$	L
9	5.6%	150.5	151.4	187
10	5.7%	173.8	175.0	209
11	5.6%	195.6	196.8	231
12	4.9%	256.8	258.0	299
13	5.1%	282.6	283.8	325
14	3.8%	398.9	399.8	459
15	3.9%	435.1	436.3	493
16	3.9%	470.6	472.0	527
17	3.9%	504.5	505.9	561
18	3.6%	601.6	603.0	665
19	3.6%	639.5	640.9	703
20	3.0%	815.9	817.3	897

Furthermore, we study the mean latency: $\frac{1}{M}\sum_{i=1}^{M}(t_i^a - t_i^s)$ of Algorithm 1 with respect to the user number. For each M between 9 and 20, 100000 delay offset combinations are randomly generated. $\overline{\delta}$, the average mean latency over all these samples, is recorded in Table III compared with $\overline{\alpha} := \frac{1}{M}\sum_{i=1}^{M}\alpha_i$ and the sequence period L. Results obtained show that $\overline{\delta} < \overline{\alpha} < L$ for any M and $\overline{\delta}, \overline{\alpha}, L$ all become larger when M increases, as expected. We also compute the proportion ρ for each M: the ratio between the number of cases in which the latency of user i is strictly smaller than α_i and that of all simulated cases: $100000M$. Roughly speaking, it becomes smaller when M increases as tabulated in Table III.

VII. CONCLUSION

This paper has investigated UD and DD sequences to accordingly address the identification and synchronization problems on a collision channel. In order to study how deterministic guarantees can be offered, lower and upper bounds on their minimum periods are both presented for frame-synchronous and slot-synchronous access, respectively. We summarize these bounds for large M in Table IV.

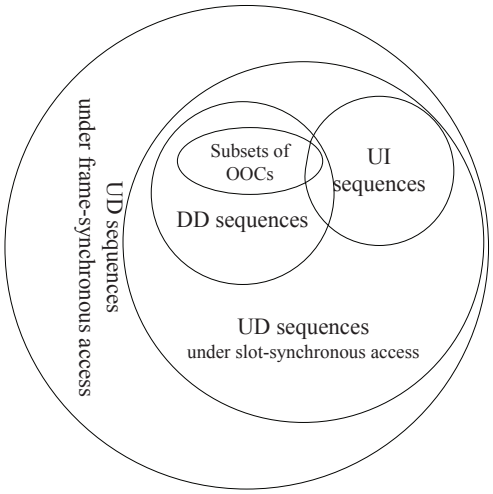

Fig. 3. Relationships among UD, DD sequences and other sequence designs.

TABLE IV
LOWER AND UPPER BOUNDS ON THE MINIMUM PERIOD OF UD AND DD SEQUENCES.

	Lower bound	Upper bound
UD seq. under frame-syn. access	$2M/3$ (Thm. 2)	M
UD seq. under slot-syn. access	$2M^2/9$ (Thm. 4)	$2M^2$ (Thm. 6)
DD seq. under slot-syn. access	$2M^2/9$ (Thm. 4)	$4M^2$ (Thm. 10)

As illustrated in Fig. 3, we establish some interconnections among UD, DD sequences and some other families of binary sequences. A UD sequence set under slot-synchronous access must be UD under frame-synchronous access by (1) and (6), and meanwhile a DD sequence set must be UD by (6) and (7). Furthermore, a UI sequence set is found UD from Theorem 6 and the OOCs with $w > (M-1)\lambda_c + \lambda_a$ can be used to construct DD sequences from Theorem 8. These reported results open up many interesting directions for future research, for example, a construction of shorter UD sequences under slot-asynchronous access which is not UI.

In addition, we propose Algorithm 1 and Algorithm 2 that allow a receiver to solve the identification and synchronization problems within some bounded delay by employing UD and DD sequences, respectively. Simulation results are also provided to help readers come to a better understanding of their performance fluctuations.

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