CENG 4480 Midterm (2016 Fall)

Name: _____
ID: _____

Solutions

Q1 (30%) Check or fill the correct answer:

1. A circuit where the input signal power is greater than the output signal power is called **amplifier/attenuator**.
2. A amplifier with input voltage of 10mv and output voltage 1V has gain ___ dB.
3. In ideal op amplifier, V_{in+} **$>$ / $=$ / $<$** V_{in-} and has **infinite/finite** closed-loop gain.
4. Impedance of a capacitor C is **jwC/$\frac{1}{jwC}$**.
5. Which of the following sensor is usually used to measure rotation angle?
   Accelerometer/ Gyroscopes/Strain Gauge
6. Light-to-voltage optical sensors contains **photodiode/amplifier** to sense light intensity change.
7. In Sample-and-Hold Amplifier, when MOSFET conducts, "hold" capacitor **charge/discharge**.
8. Op-Amp Comparator is worked in **open/closed** loop mode.
9. For high quality audio and video, **Flash/Successive/Tracking** ADC is applied.
10. In PID control, we will get **faster/slower** response when increase proportional gain, **faster/slower** elimination of steady state error and **increase/decrease** overshot for larger derivative gain.
11. In typical loss pass filter, $\frac{1}{R_F C_F}$ is called **4-dB/3-dB/2-dB** frequency.
12. **Voltage/Current** can be expressed as $\frac{dQ}{dt}$.

Q2 (15%)

The integrator of Fig. 1 senses an input signal given by $V_{in} = V_0 \sin \omega t$. Determine the output signal amplitude if $A_0 = \infty$.

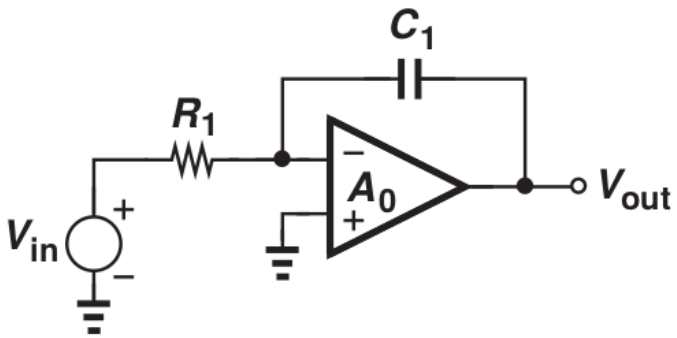

Figure 1: Figure of Q2

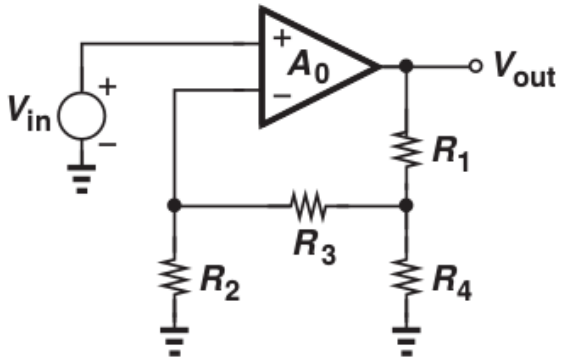

Figure 2: Figure of Q3

Q3 **(20%)** Calculate the closed-loop gain of the non- inverting amplifier shown in Fig. 2 if $A_0 = \infty$. Verify that the result reduces to expected values if $R_1 \to 0$ or $R3 \to 0$.

Q4 **(15%)** Explain the condition when glitch occurs at DAC. Provide two approaches to eliminate glitch.

Q5 **(20%)** For the 4-bit R-2R DAC (Fig. 3), calculate V_0 for the digital input of (1,0,0,0) if V-ref is grounded.

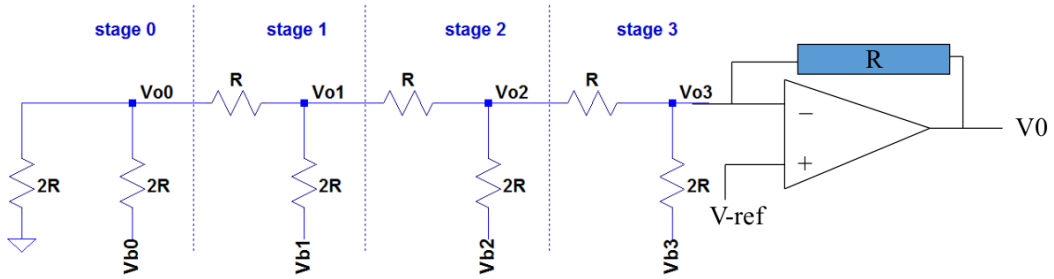

Figure 3: Figure of Q5

A1

1. amplifier
2. 2
3. =, finite
4. *jwC*
5. Gyroscopes
6. photodiode
7. charge
8. open
9. Flash
10. faster, faster, decrease
11. 3-dB
12. Current

A2 It is easy to know,

$$V_{out} = -\frac{1}{R_1 C_1}\int V_{in} dt \tag{1}$$

i.e.,

$$V_{out} = \frac{V_0}{R_1 C_1 \omega}\cos \omega t \tag{2}$$

Output signal amplitude is $\frac{V_0}{R_1 C_1 \omega}$

A3 if $A_0 = \infty$,

$$V_+ = V_- = V_{in} \tag{3}$$

then we have,

$$V_- = \frac{R_2}{R_2 + R_3}\frac{R_4||(R_2+R_3)}{R_1 + R_4||(R_2+R_3}V_{out} \tag{4}$$

therefore, closed-loop gain is,

$$G = \frac{V_{out}}{V_{in}} = \frac{R_2}{R_2 + R_3}\frac{R_4||(R_2+R_3)}{R_1 + R_4||(R_2+R_3} \tag{5}$$

if $R_1 = 0$,

$$G|_{R_1=0} = 1 + \frac{R_3}{R_2} \tag{6}$$

if $R_3 = 0$,

$$G|_{R_1=0} = 1 + \frac{R_1}{R_2||R_4} \tag{7}$$

A4 A transient spike in the output of a DAC that occurs when more than one bit changes in the input code.
Glitch can be eliminated by: (1)Use a low pass filter to reduce the glitch; (2)Use sample-and-hold circuit to reduce the glitch.

A5 **To be elaborated**. First calculate Thevenin equivalent if stage 1, we get a voltage source of $\frac{V_{b0}}{2}$ in series with resistor R. And then, we can determine equivalent circuit of stage 1 and 2. Repeat above step, the contribution of V_{b0} at V_{o3} is $\frac{V_{b0}}{16}$ in series with resistor R. Using the properties of op amp, $V_0 = \frac{V_{b0}}{16} = \frac{1}{16}$