CENG 4480

Lecture 11: PCB

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Reference:

- Chapter 5 of Ground Planes and Layer Stacking
- **High speed digital design**
- by Johnson and Graham

香港中文大學
The Chinese University of Hong Kong

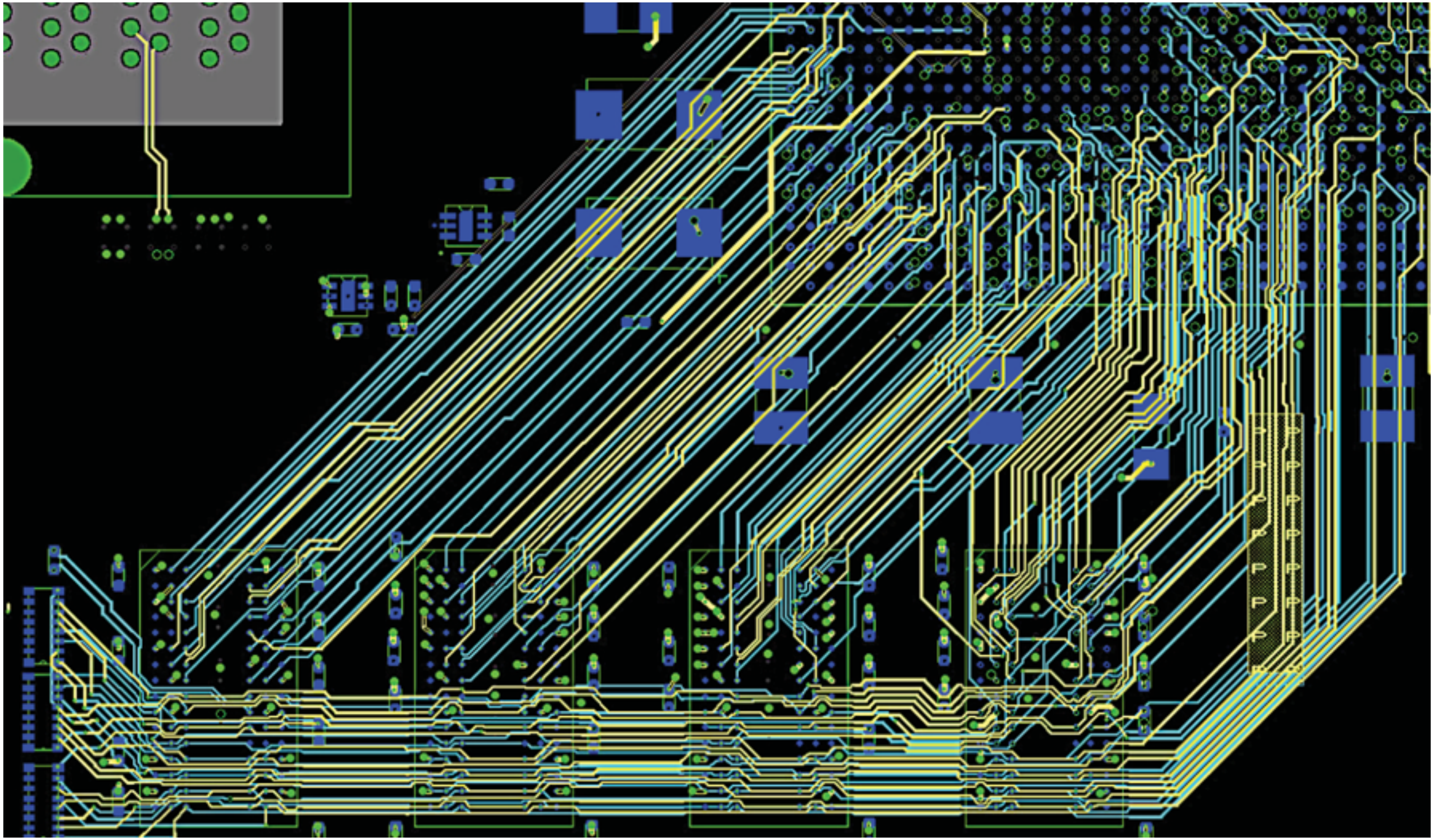
Introduction

- What is a PCB
- Why we need one?
  - For large scale production/repeatable fabrication
  - Reliable: much better than ad hoc bread board
  - Controlled Electrical characteristics
- Many videos showing you how to make one on You Tube
  - https://www.youtube.com/watch?v=e-gMsABCRTI
- Our lecture:
  - Not on how to make one (you will try one later)
  - More concern about issues on reliability; electrical characteristics

How to Make a PCB

1. Cut the board
2. Toner transferring
3. Removing the paper
4. Etching using acid
5. Clean the board
6. Drilling the holes

Modern PCB Design — 1



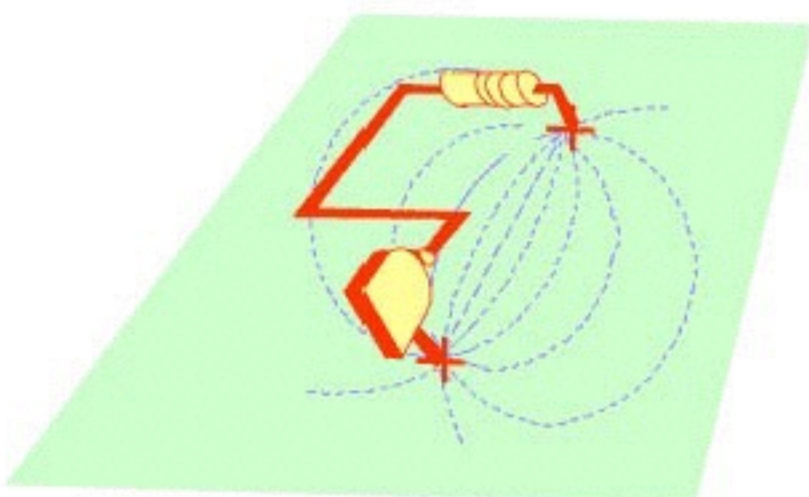
DDR3 Layout on Layers 2 and 3 [www.mentor.com]

Functions of Ground and Power Planes

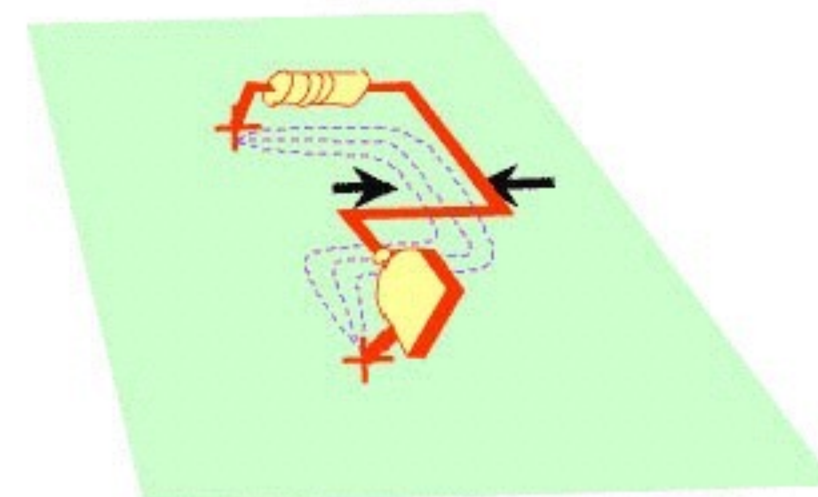
- Provide stable reference voltage for digital signal
- Exchange Distribute power
- Control crosstalk between signals
- Note:
  - All formula are approximations
  - In this book, signal trace = tracks on PCB

Current Path

- At low speed: => Follow Least Resistance
- At high speed: Follow Least Inductance



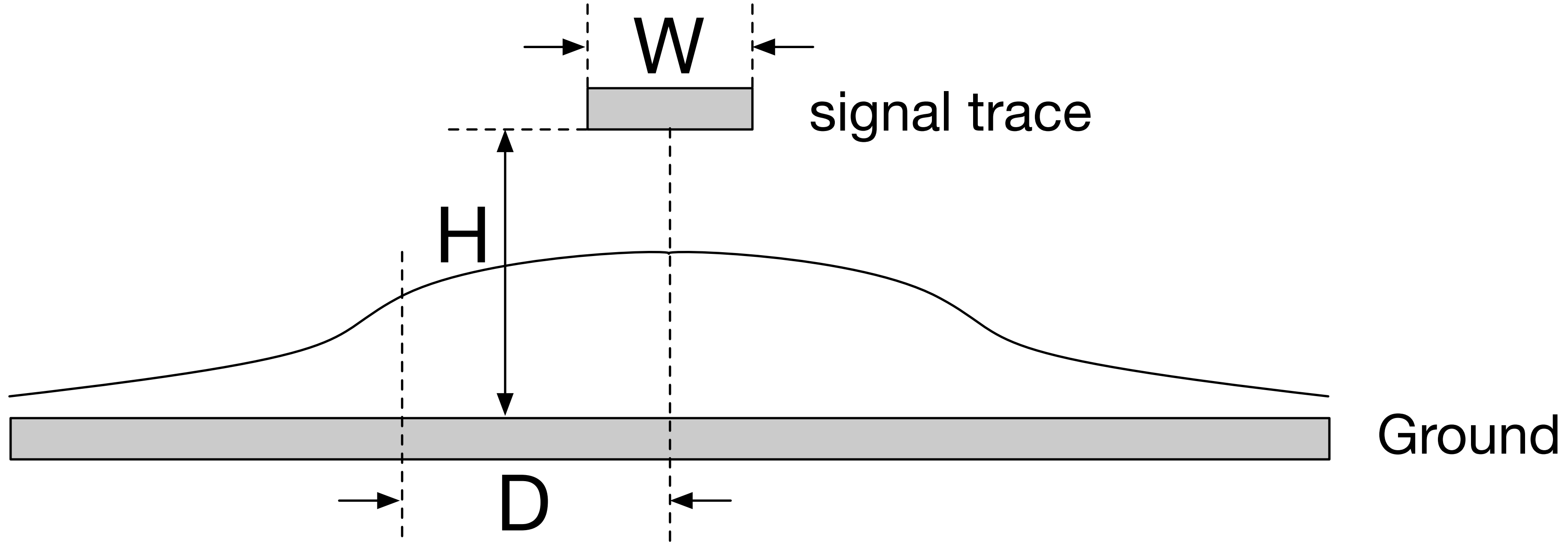
At low speeds, current flows the path of least resistance



At high speeds, current flows the path of least inductance

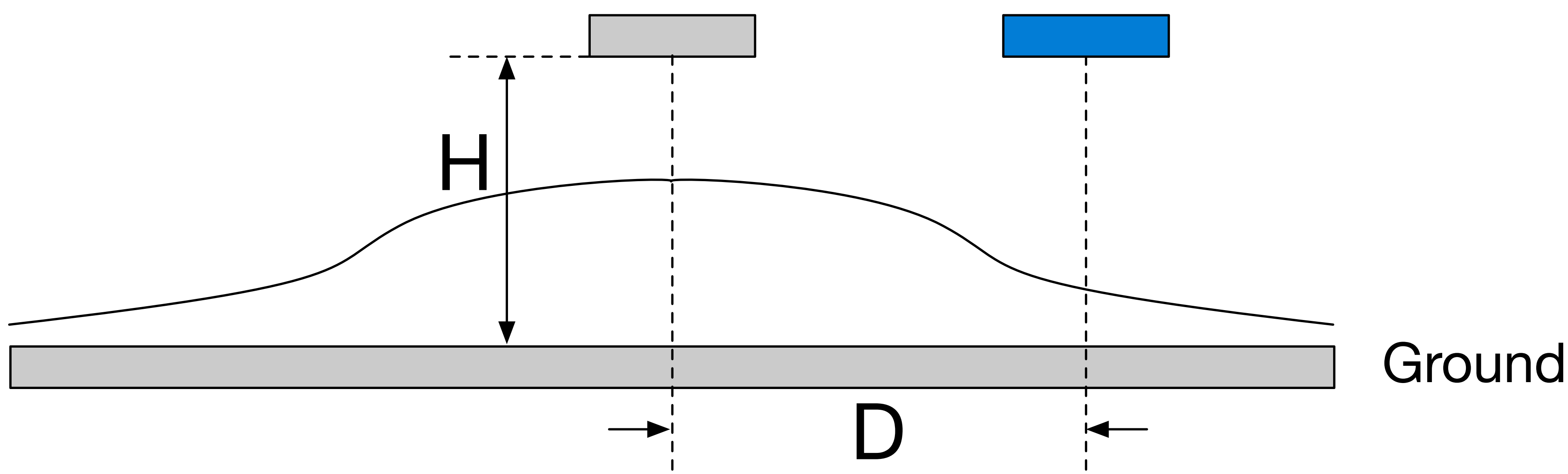
Return-current density

- A function of H and D:
  - H: hight of trace above PCB
  - D: perpendicular distance
- Current density at D is: $$\frac{I_o}{\pi H} \cdot \frac{1}{1+(D/H)^2}$$
- Current density at D is proportional to : $$\frac{1}{1+(D/H)^2}$$



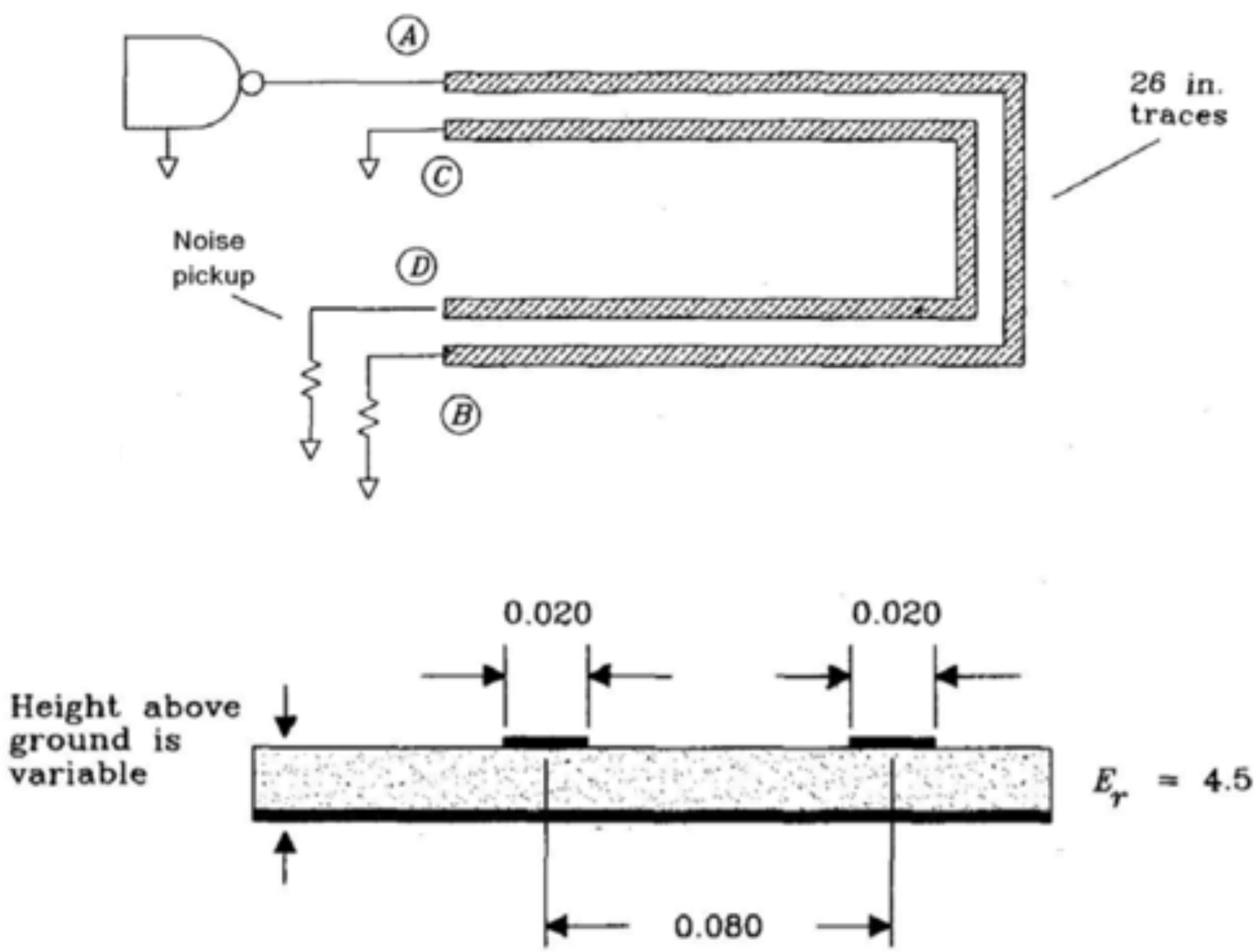
Crosstalk in Solid Ground Planes

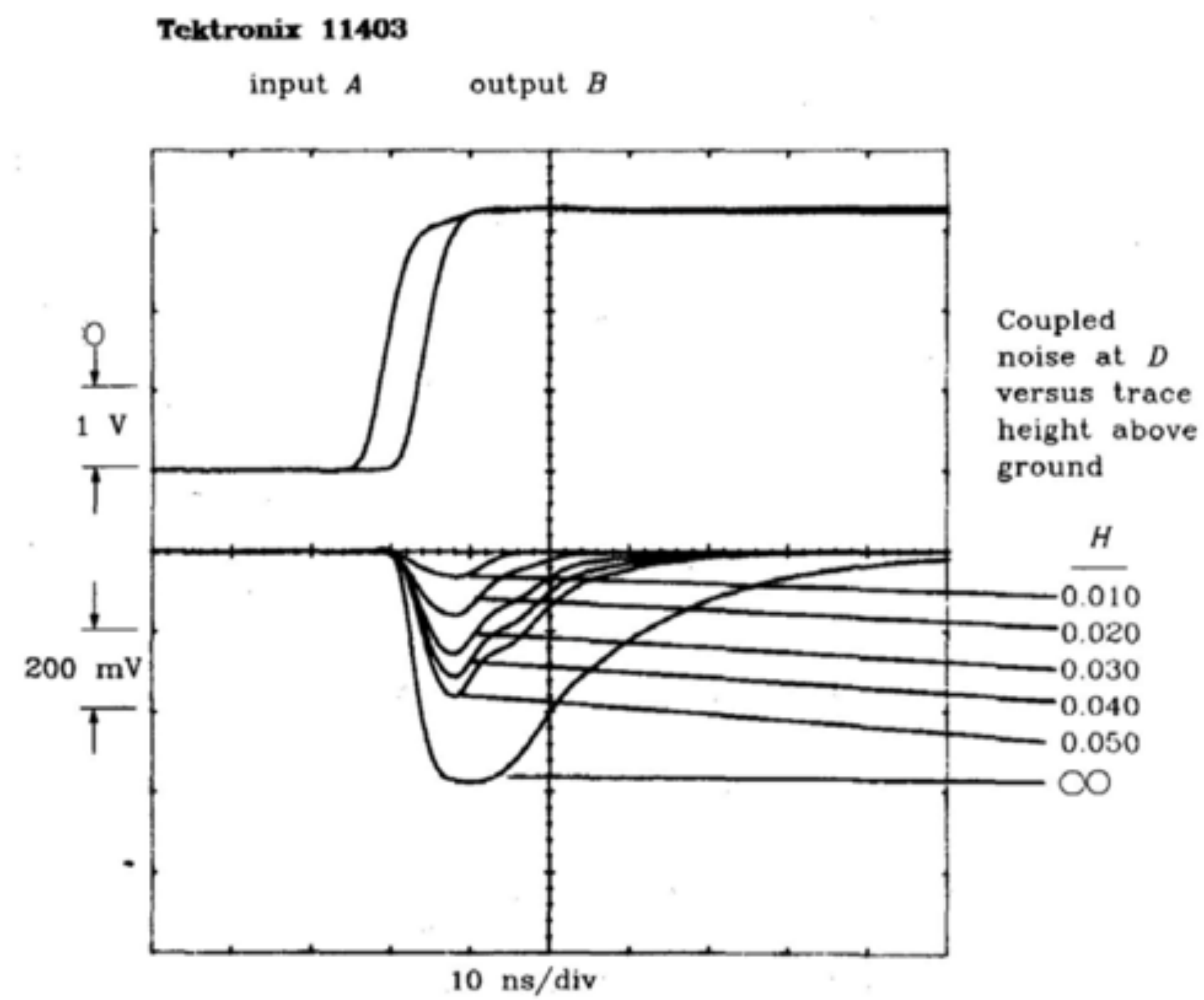
- Magnetic fields => induce voltages in other circuit traces
- Mutual Inductance & Mutual Capacitance
  - inductance effects dominates
- Crosstalk $\simeq \frac{K}{1+(D/H)^2}$
  - K <= rise time & length of trace
  - Faster rise time, higher K



Simple Crosstalk Experiment

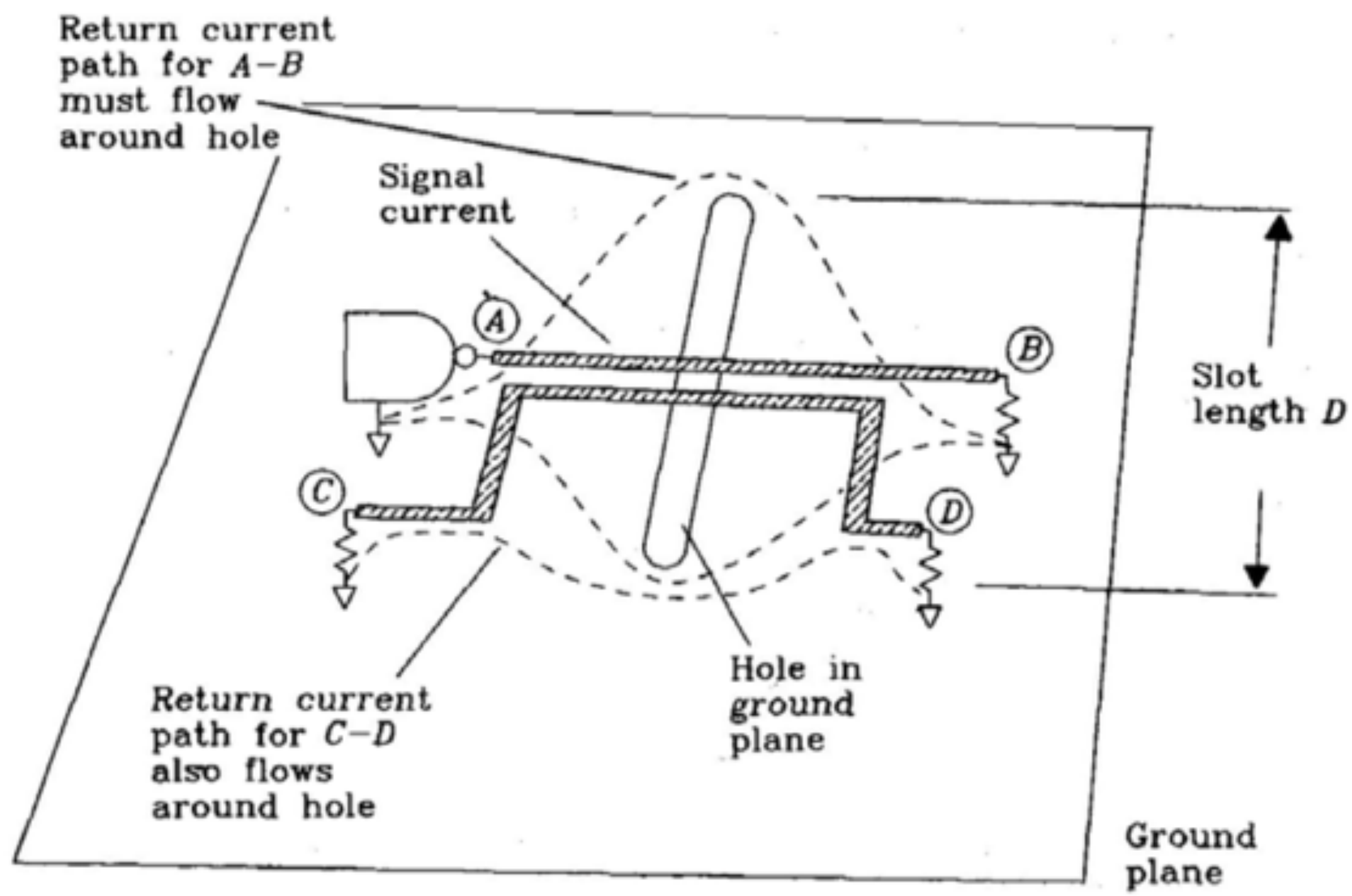
- 26 in Cu track separated by 0.08 in centre to centre
- Ground plane is a solid Cu sheet





Crosstalk in Slotted Ground Planes

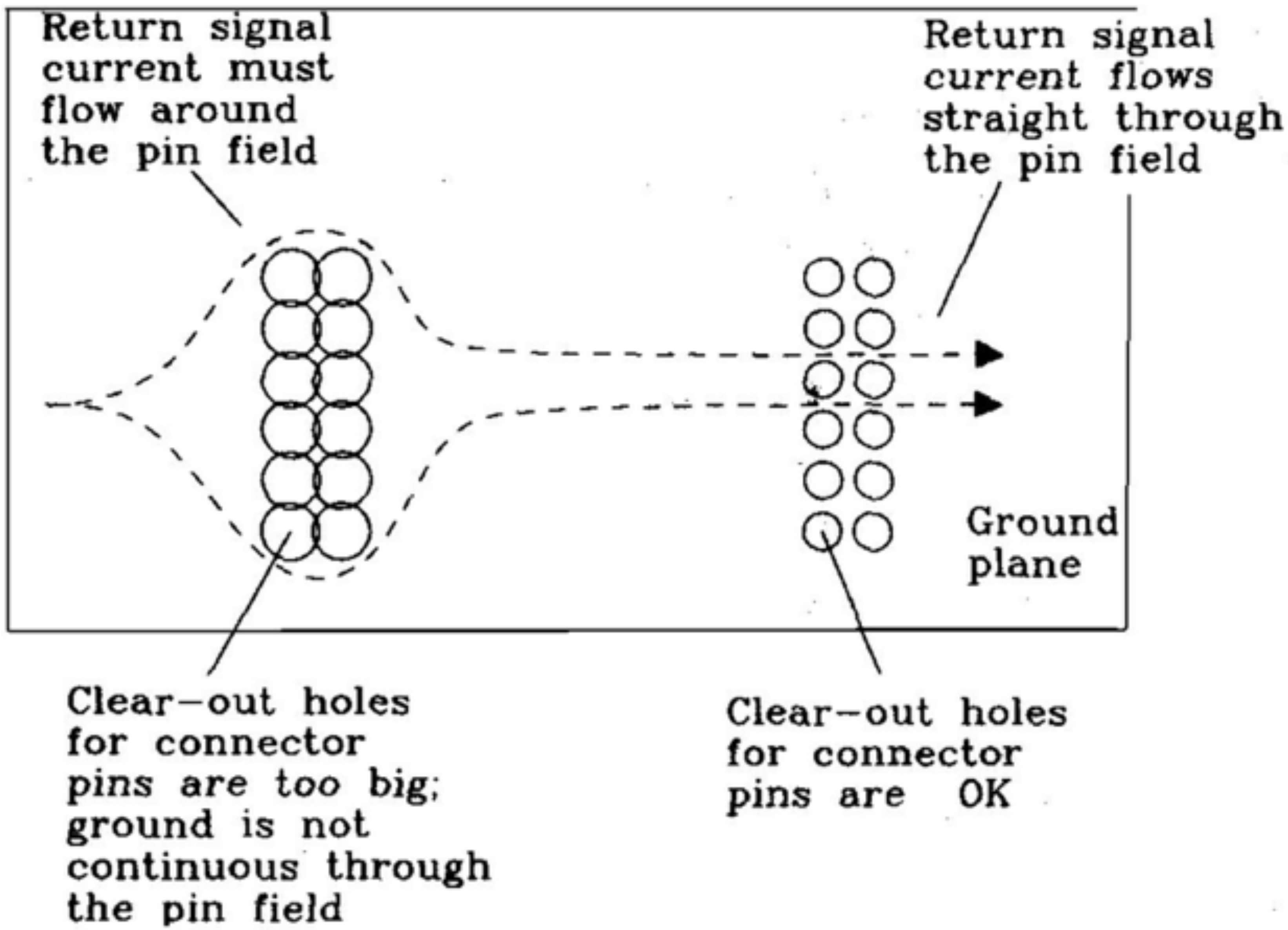
- Ground slots increases crosstalk:
  - large loop => higher inductance
  - Overlaps with other signals
- Must not tolerate



Crosstalk in a slotted ground plane.

Crosstalk on Dense Connection Holes (Vias)

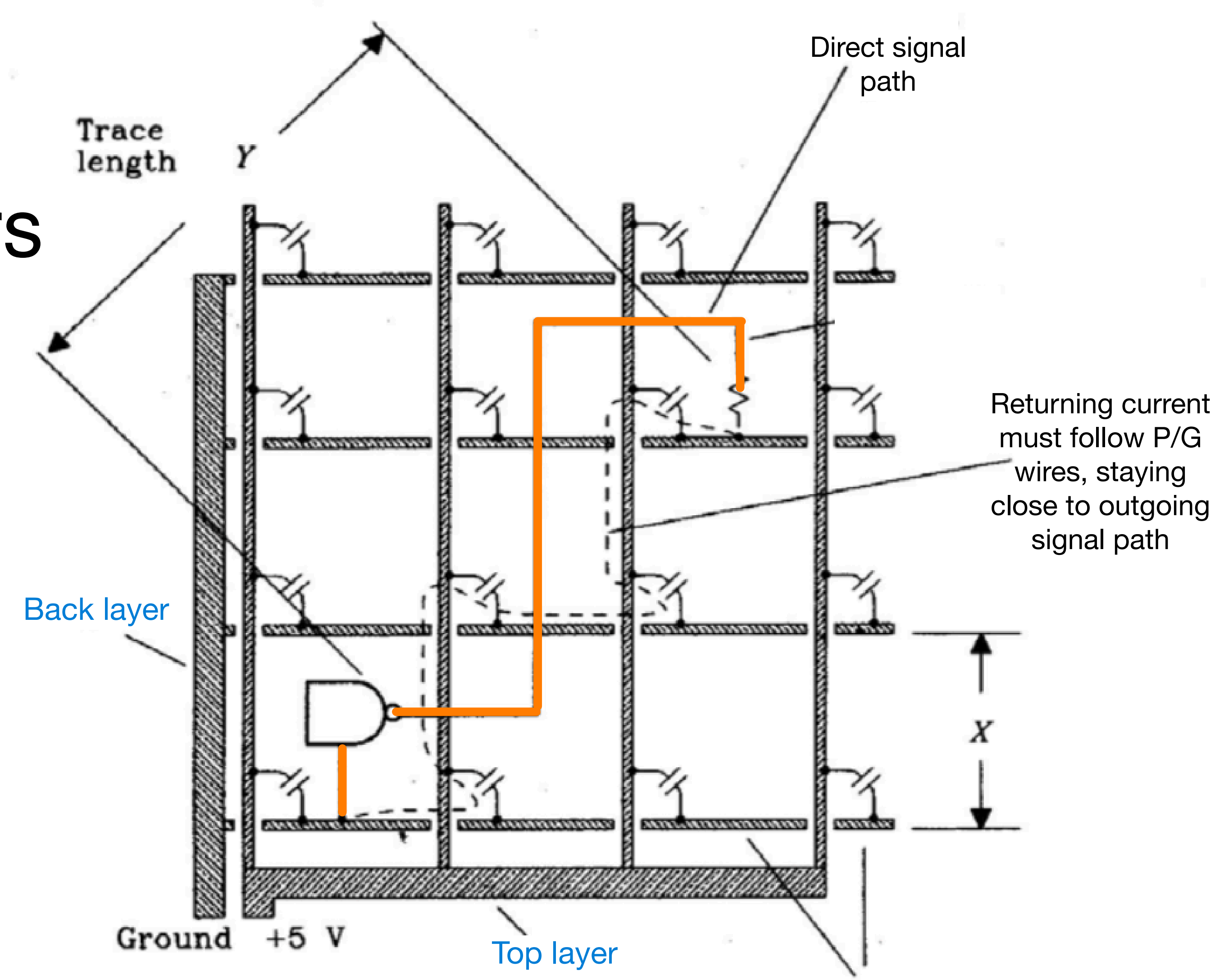
- Slots in ground plane creates unwanted inductance
- Slots inductances slows down rising edges
- Slot inductance creates mutual inductive crosstalk



Crosstalk in Cross-Hatched Ground Plane

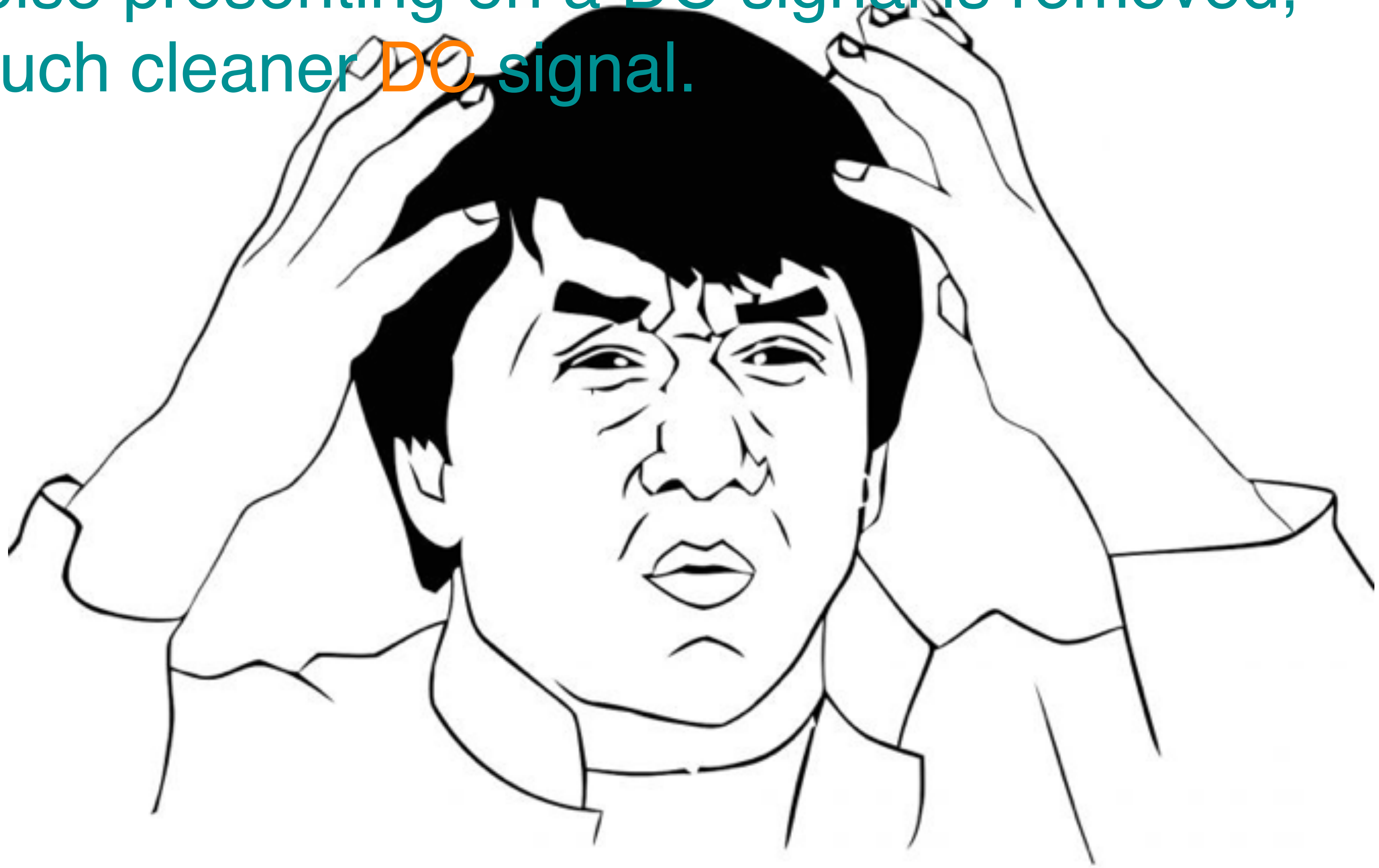
- 2-Layer board design
  - (+) Separate power & ground planes
  - (-) At the expense of increased mutual inductance
  - NOT good enough for high speed system

- Need good bypass capacitors
  - Since signals traverse several capacitors



Bypass

- A bypass is a capacitor that shorts AC signals to ground, so that any AC noise presenting on a DC signal is removed, producing a much cleaner DC signal.

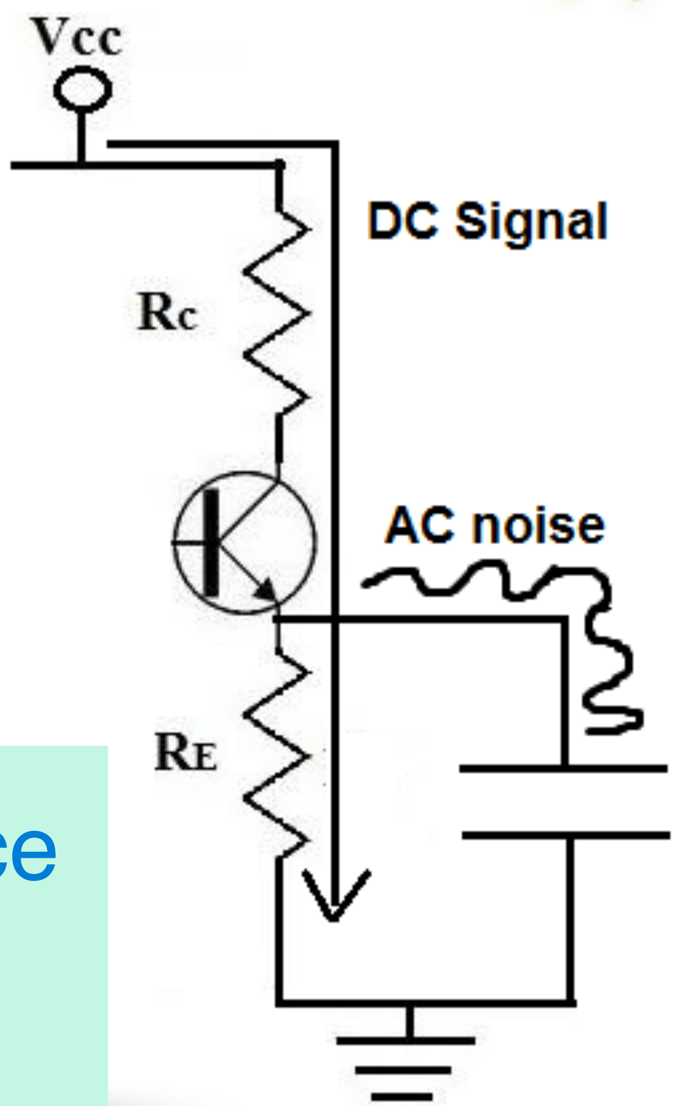


Bypass (cont.)

- Ideal DC Signal

- Practical DC Signal

- A Capacitor



- At low speed: => Follow Least Resistance
- At high speed: Follow Least Inductance

Crosstalk in Cross-Hatched Ground Plane

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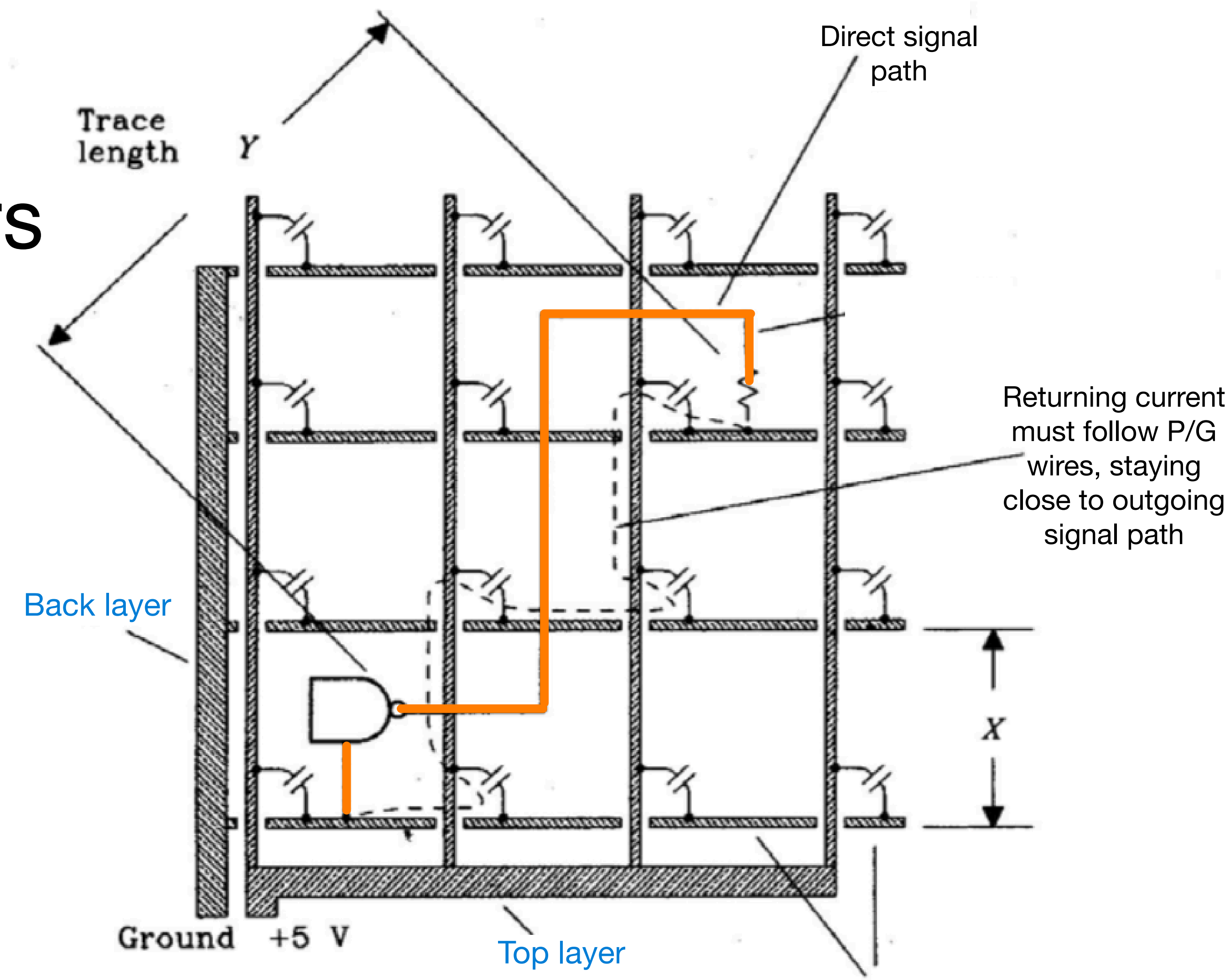
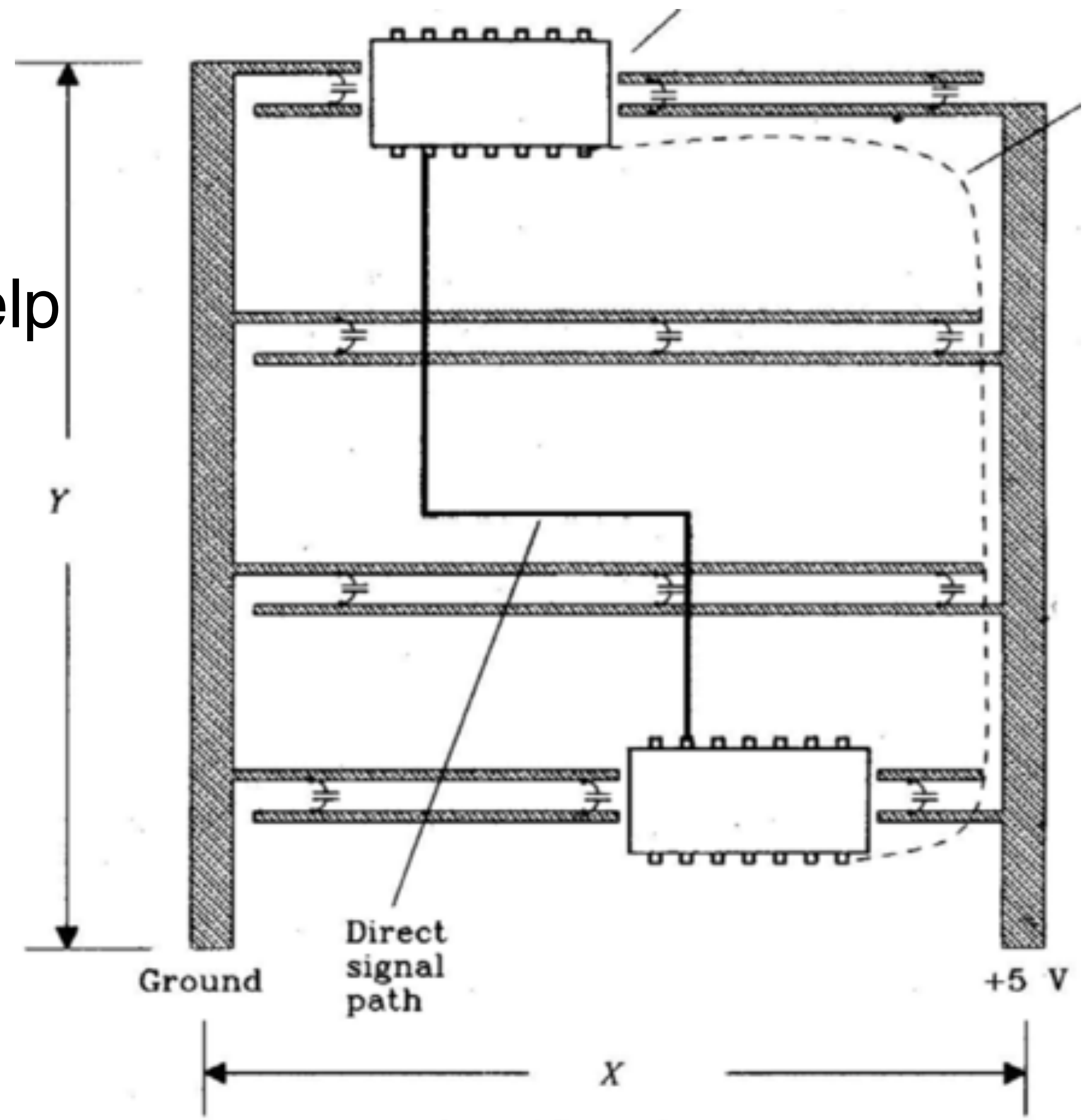


Crosstalk with Power & Ground Fingers

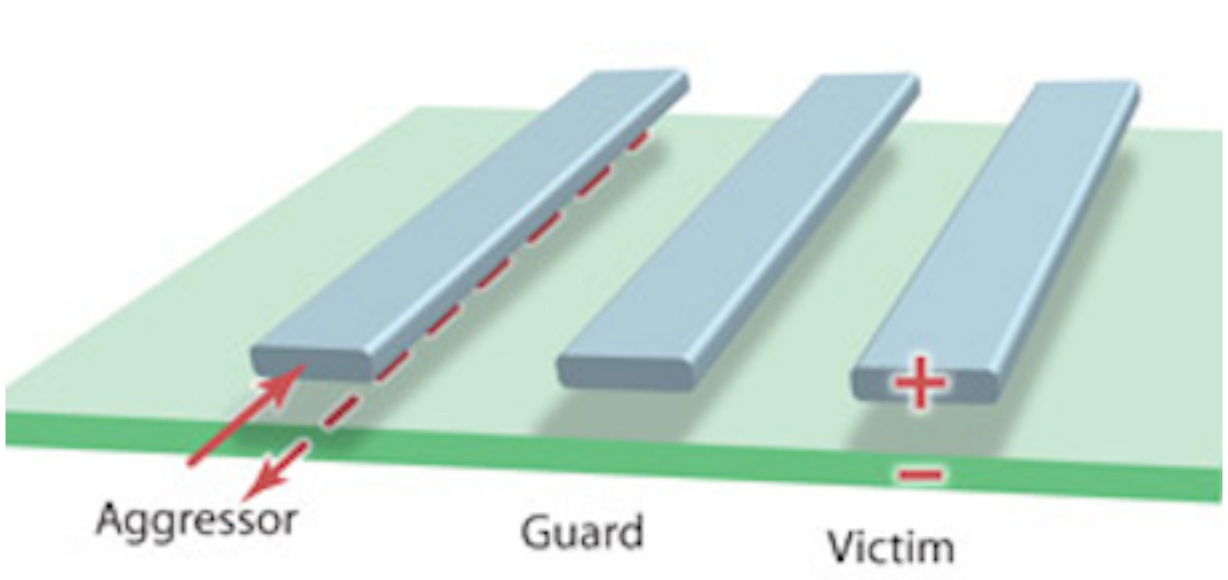
- 1 power & ground layer; and 1 signal layer
- (+) Save even more board area
- (-) Worse mutual inductance
  - only for very slow circuit
  - Fatten the ground fingers will not help



Ground fingers layout.

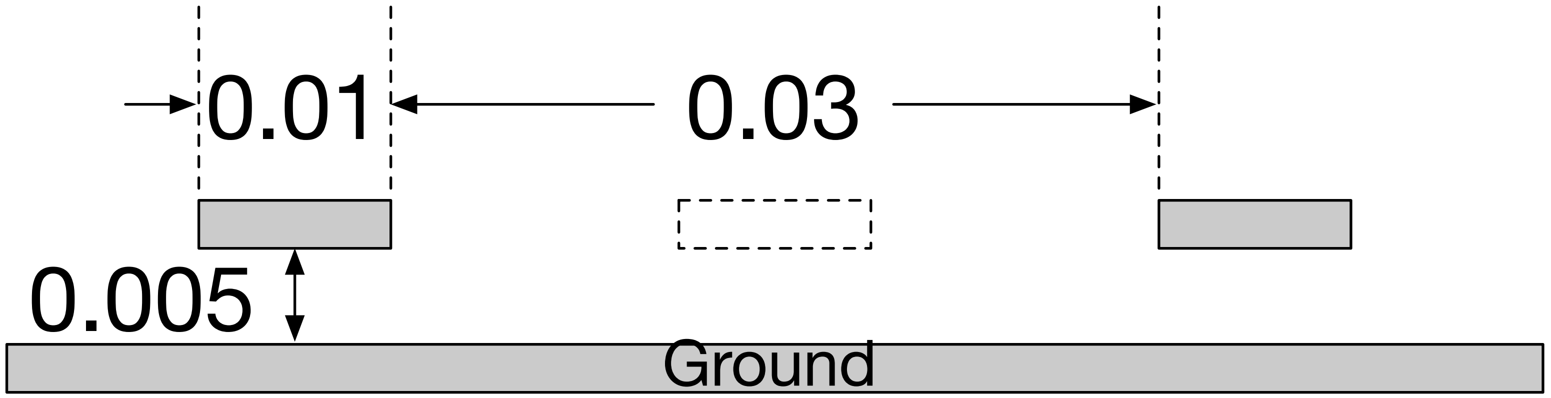
Guard Traces

- Appear extensively in Analogue Systems
  - On a two layer board w/o. solid ground plane
  - A pair of guard traces can reduce crosstalk by an order of magnitude
- In general, a trace grounded at both ends will half coupling
- In general, reduce crosstalk to 1-3% is good enough



Ex. Guard Trace Calculations

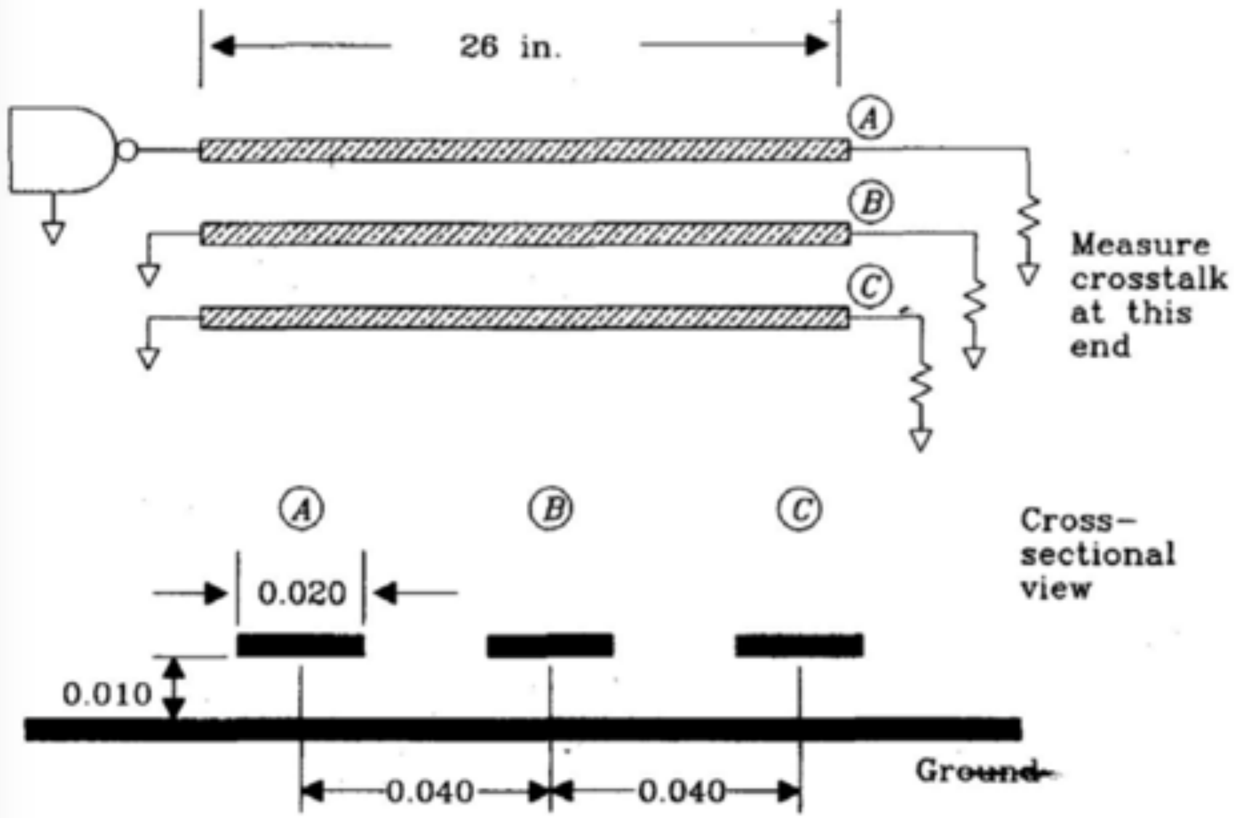
- Question: what's the estimated crosstalk?



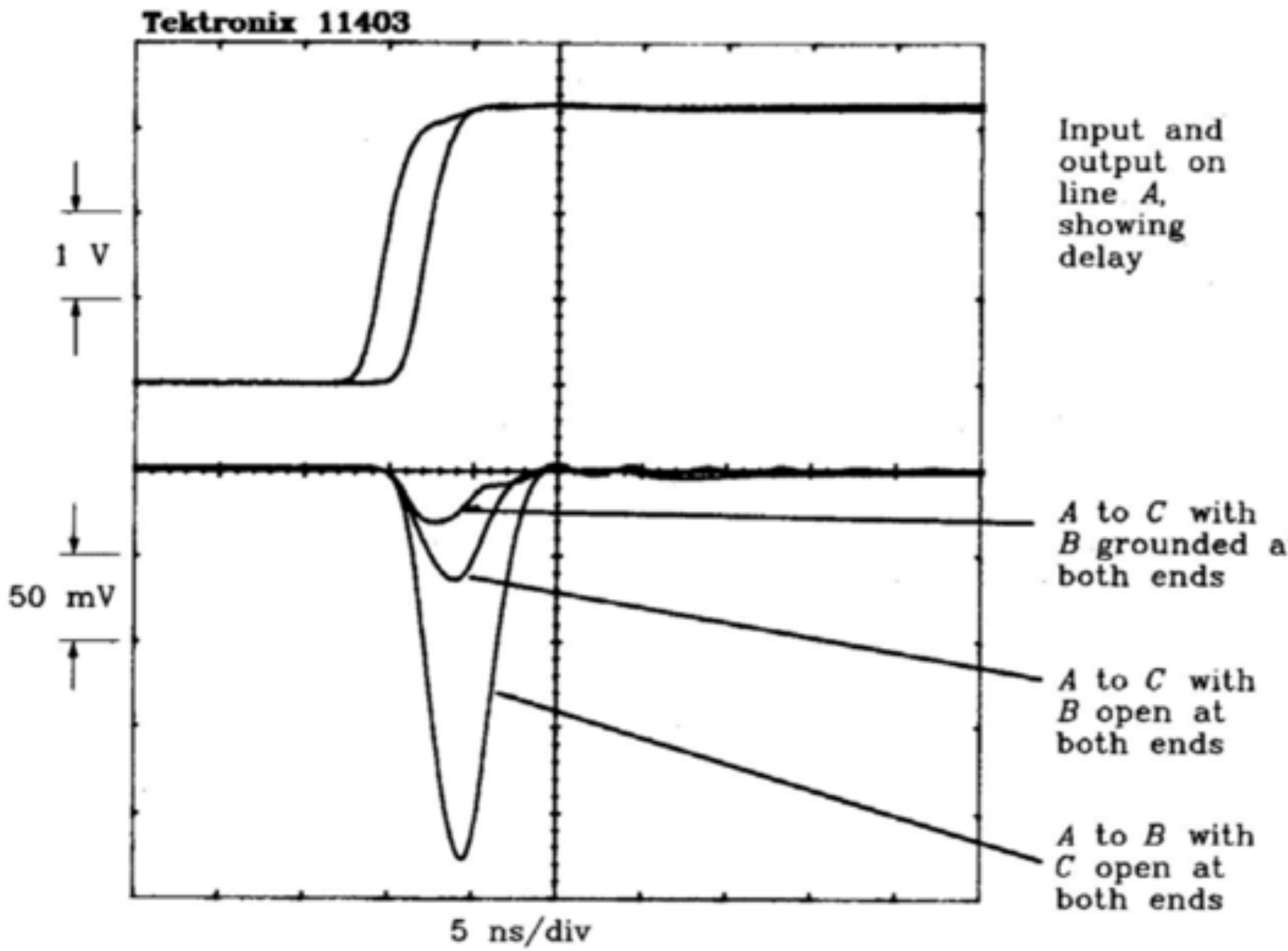
- Answer:

since K < 1, crosstalk < $\frac{1}{1+(D/H)^2} = \frac{1}{1+8^2} = 0.015$

Experiment Measuring Guard Trace Efficiencies



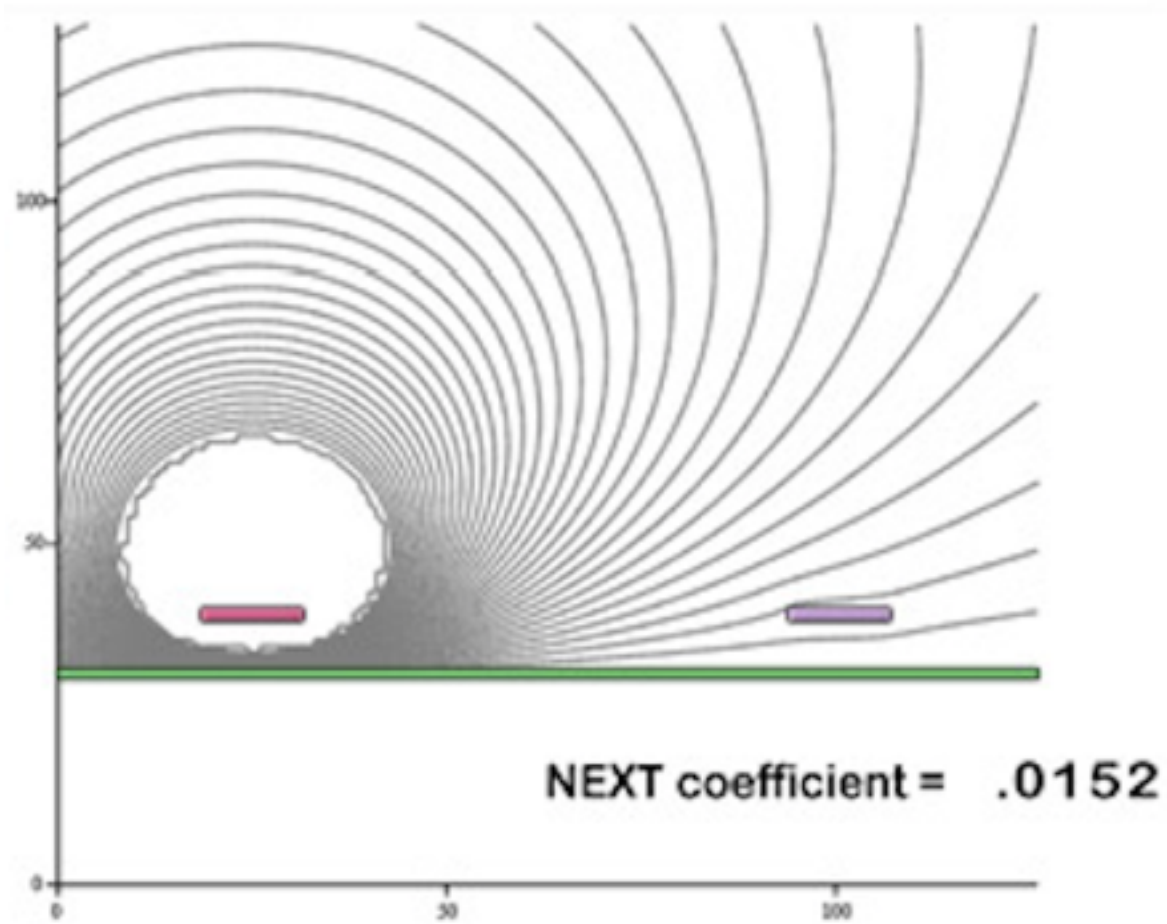
Guard trace demonstration.

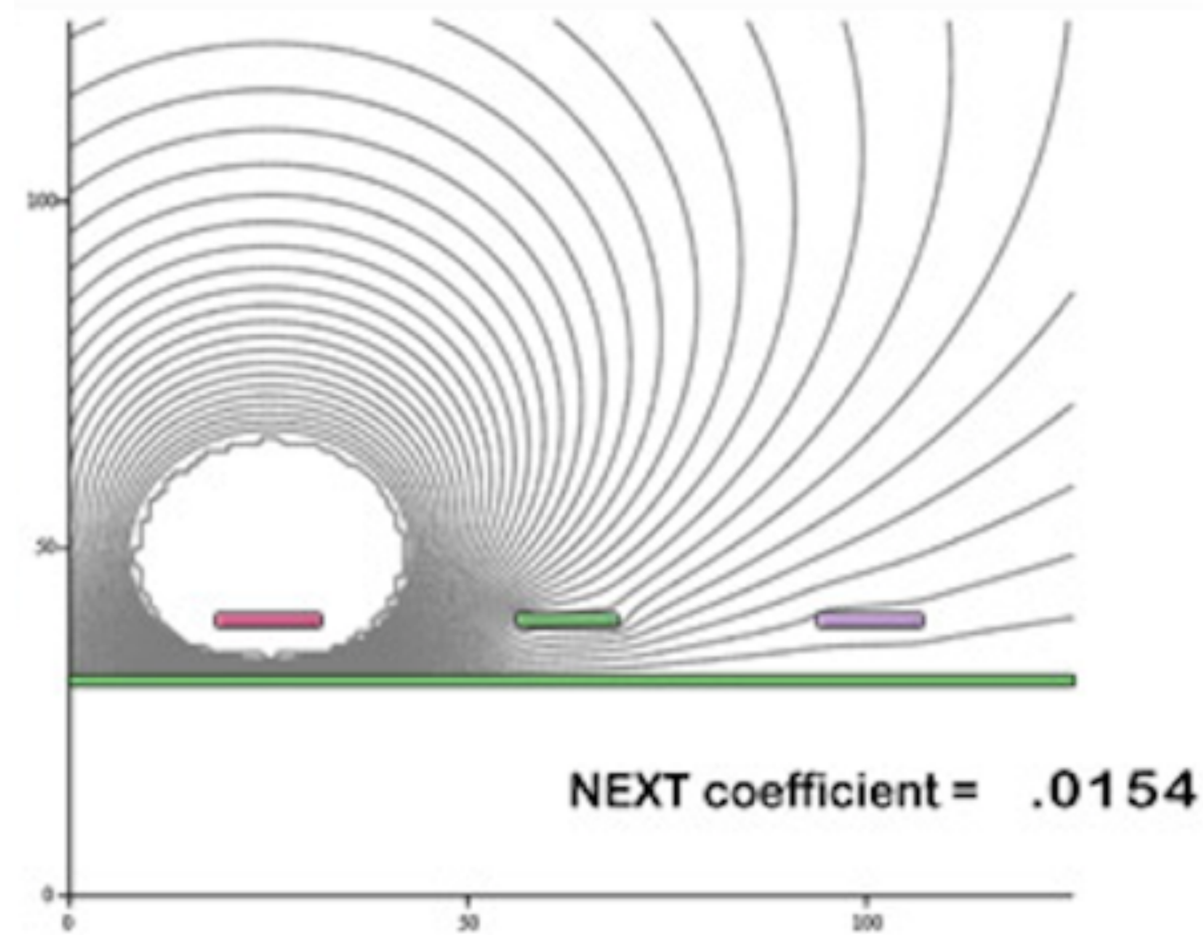


Example showing guard trace effect on coupling.

More on Guard Traces

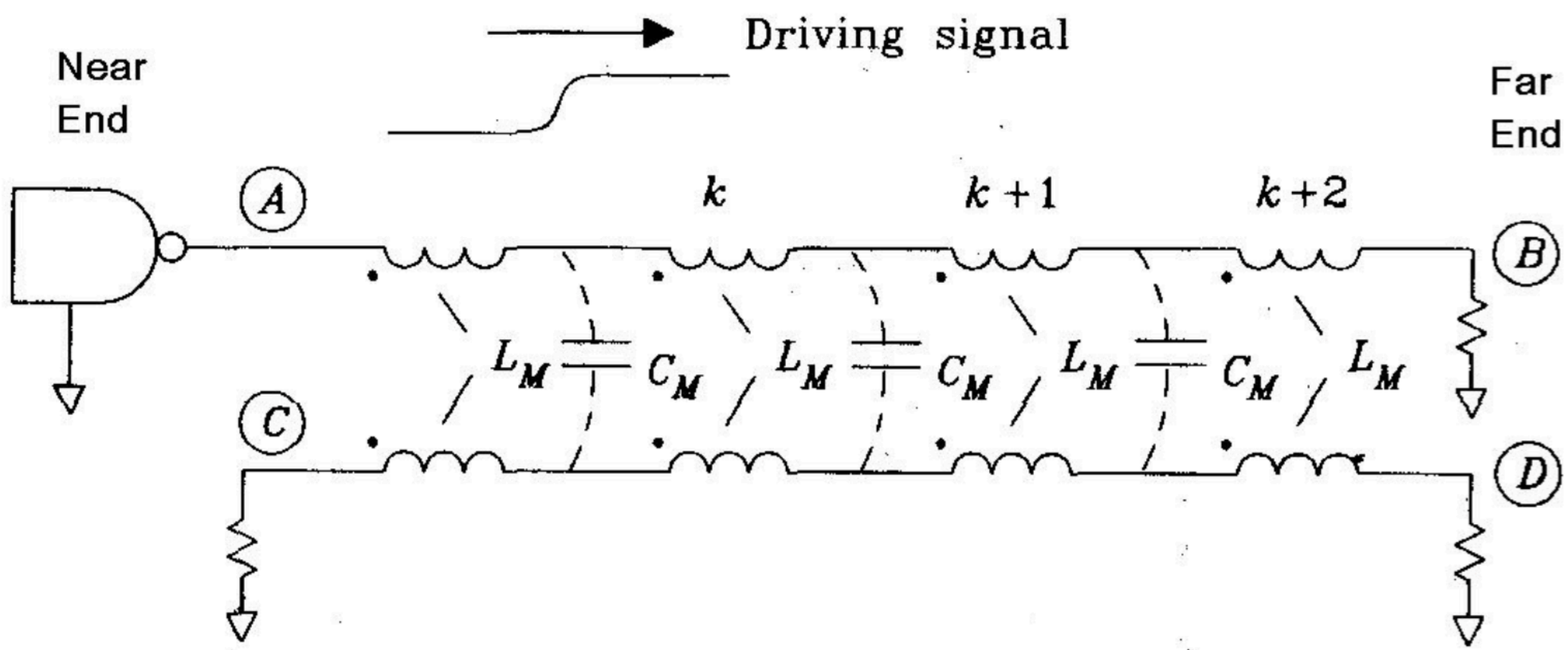
- In Digital System
  - Solid ground plane is preferred
  - No extra benefit using guard trace





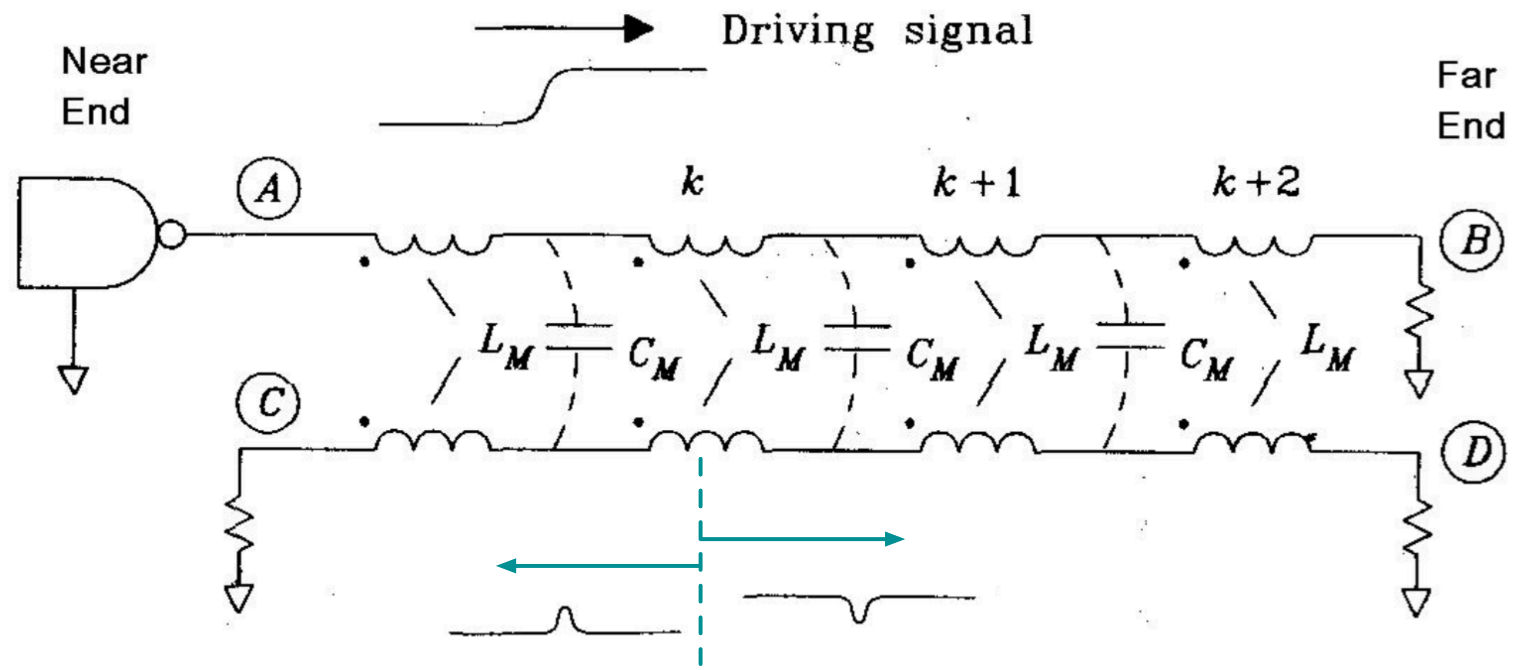
Near-end & Far-end Crosstalk

- Descriptions so far based on lumped-circuit analysis
  - No good for long transmission lines

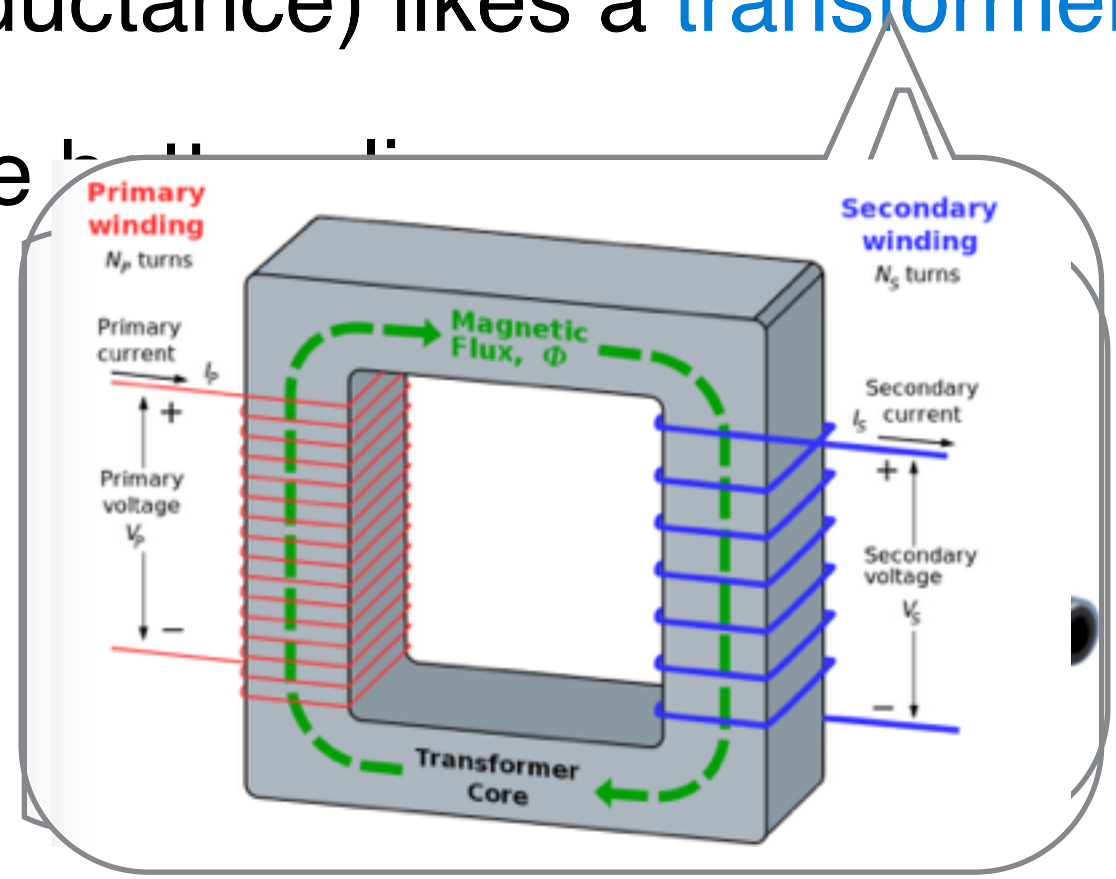


- Inductive Coupling Mechanism
- Capacitance Coupling Mechanism

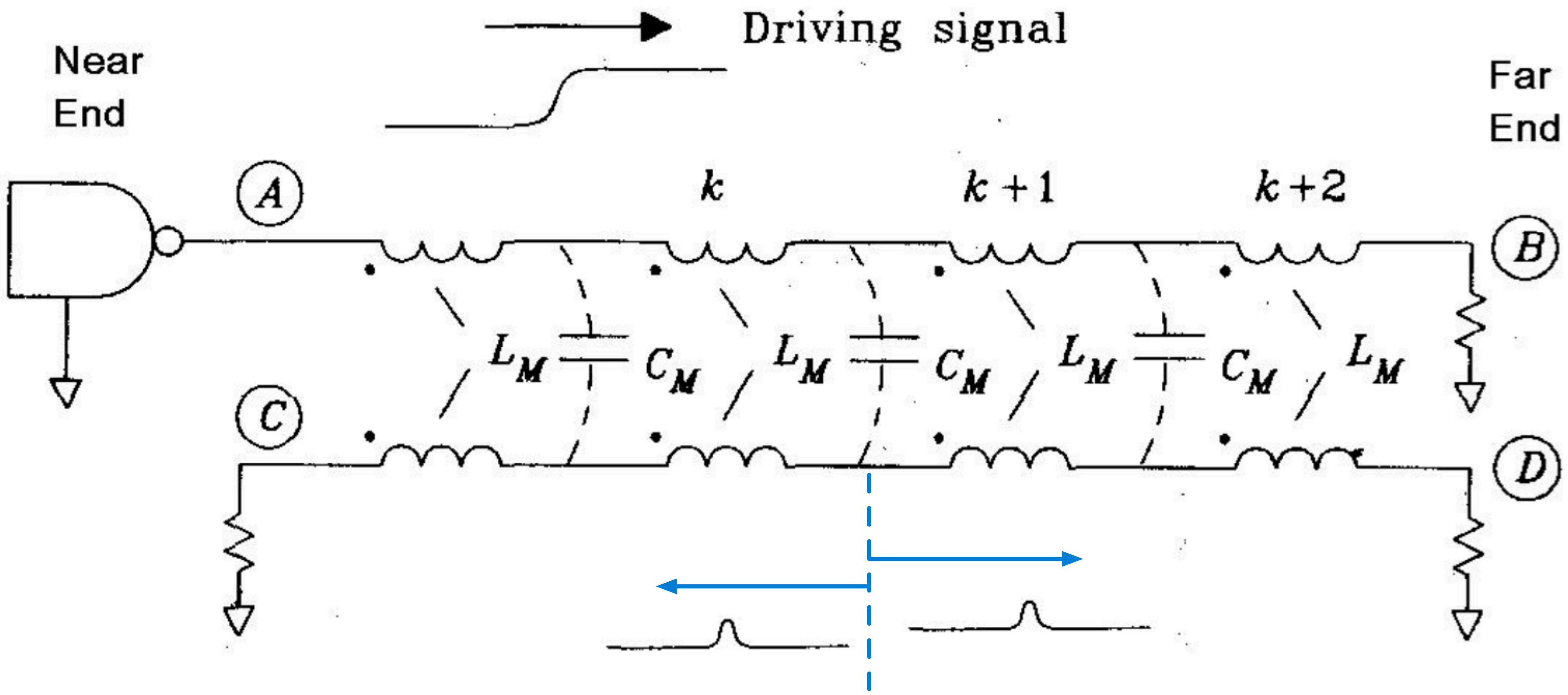
Inductive Coupling Mechanism



- Magnetic coupling (mutual inductance) likes a transformer
- A series of blips appear on the
  - Negative forward blips
  - Positive reverse blips

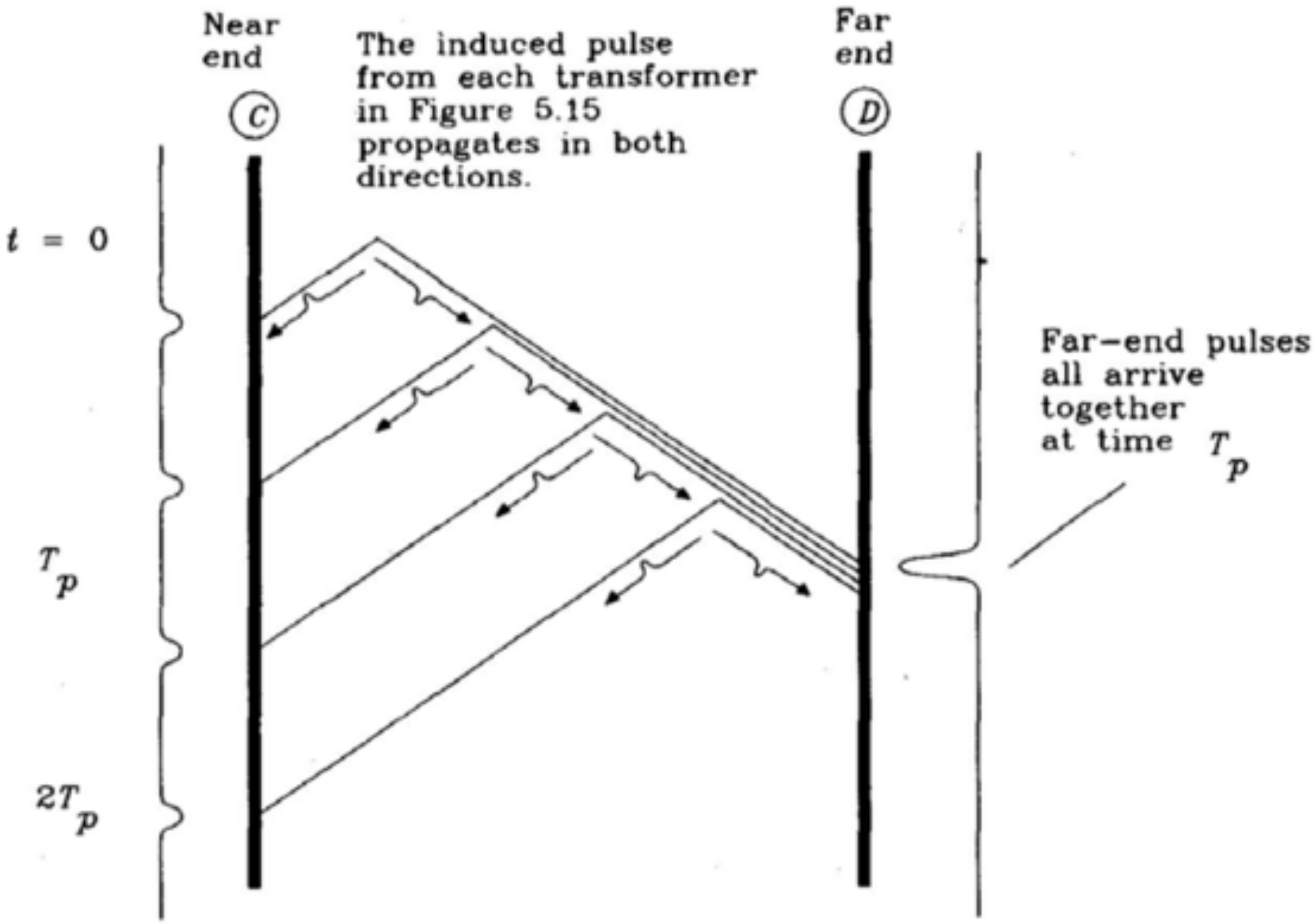


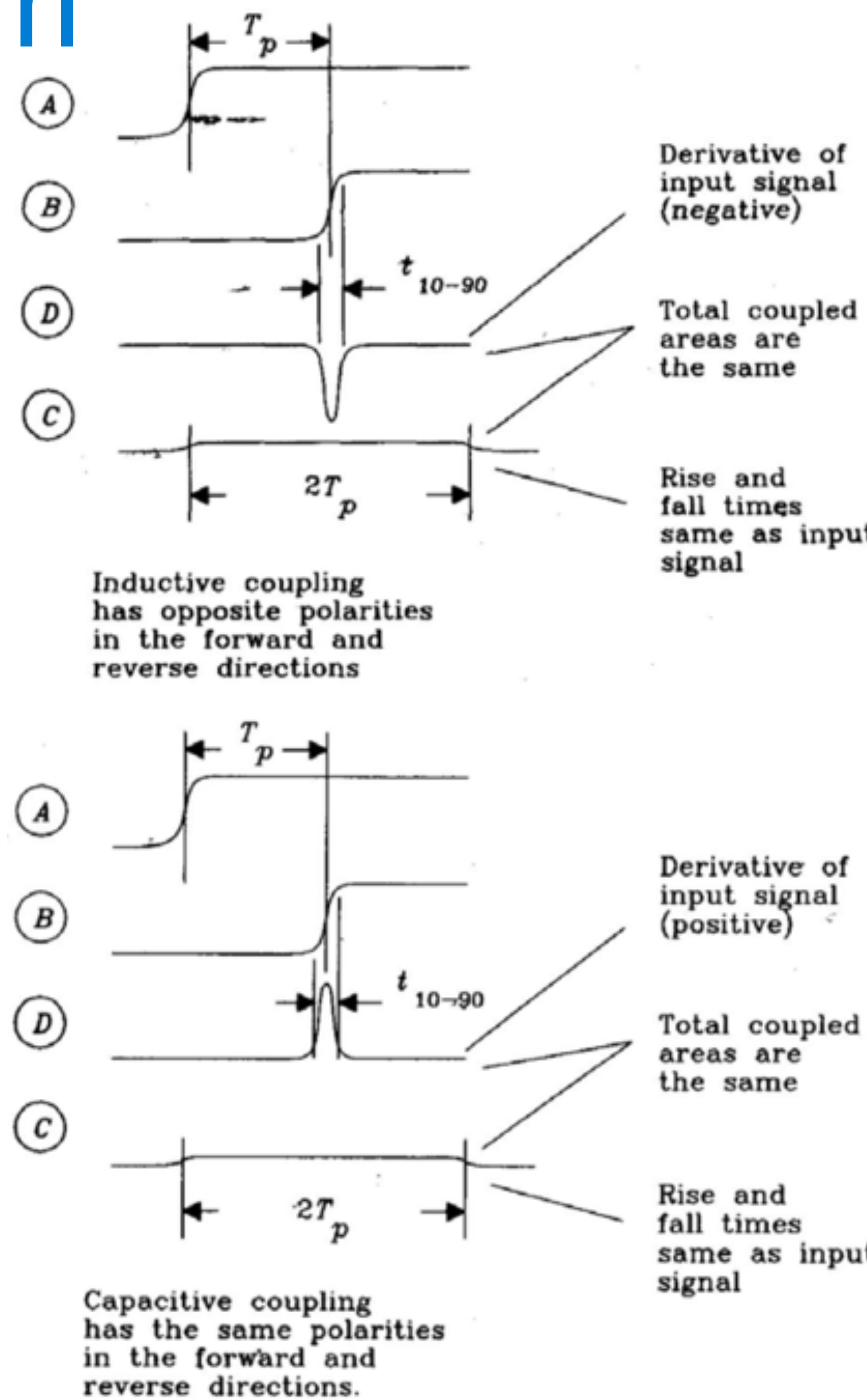
Capacitance Coupling Mechanism



- Positive for both forward and reverse blips

Reflection Diagram



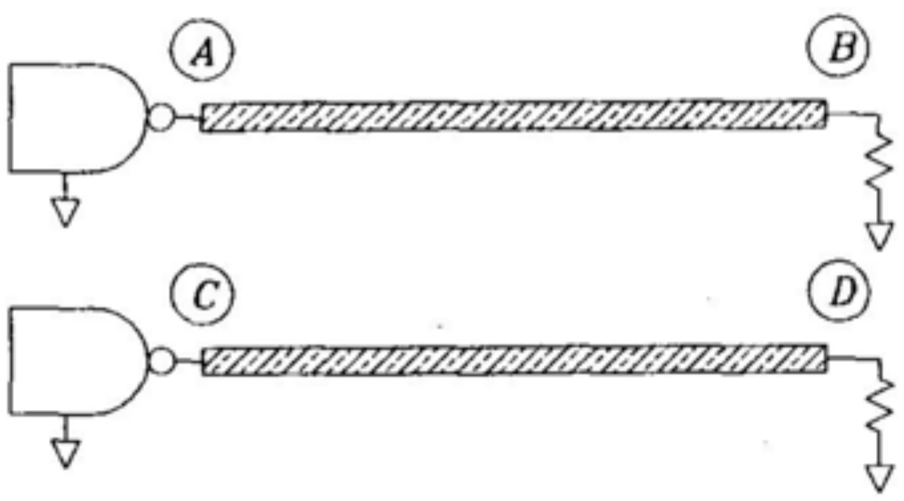


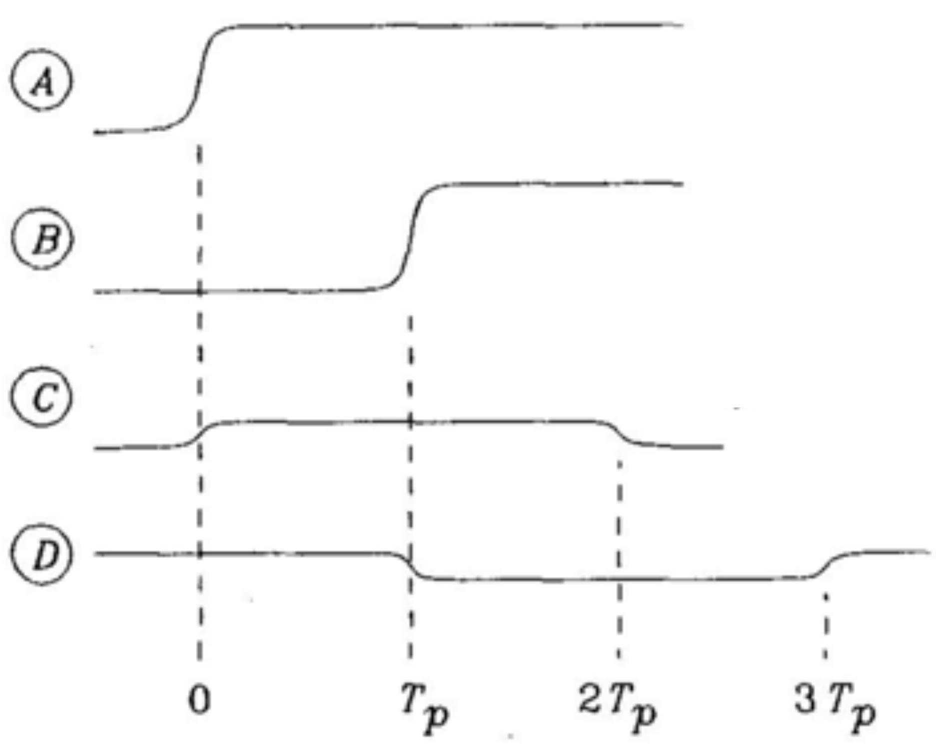
Combining Mutual Inductive & Capacitive Coupling

- Generally, over a solid ground plane, inductive and capacitive crosstalk voltages are roughly equal
- Over slotted, hatched or imperfect ground plane
  - Inductive component is much larger
  - Forward cross talk is large & negative

Near-end Crosstalk => Far-end Problem

- In practical applications without source terminators
  - Source is a low impedance driver
  - Reverse crosstalk reflects when it hits the near-end
  - Reflection coefficient = -1
  - Signal seen at the far-end is a copy of the reverse coupling signal at C, delayed by one propagation delay and inverted

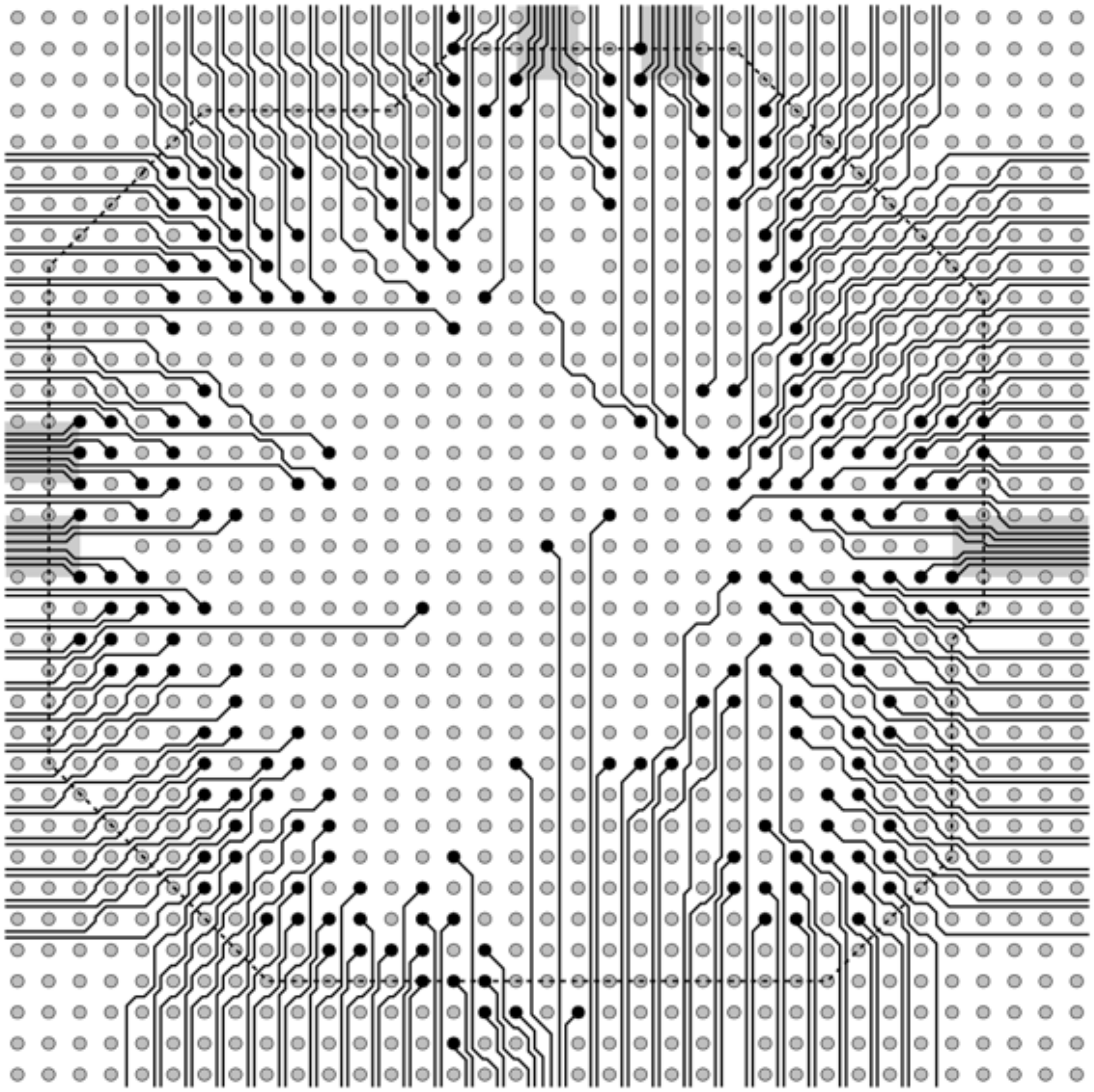




Summary (for long transmission line)

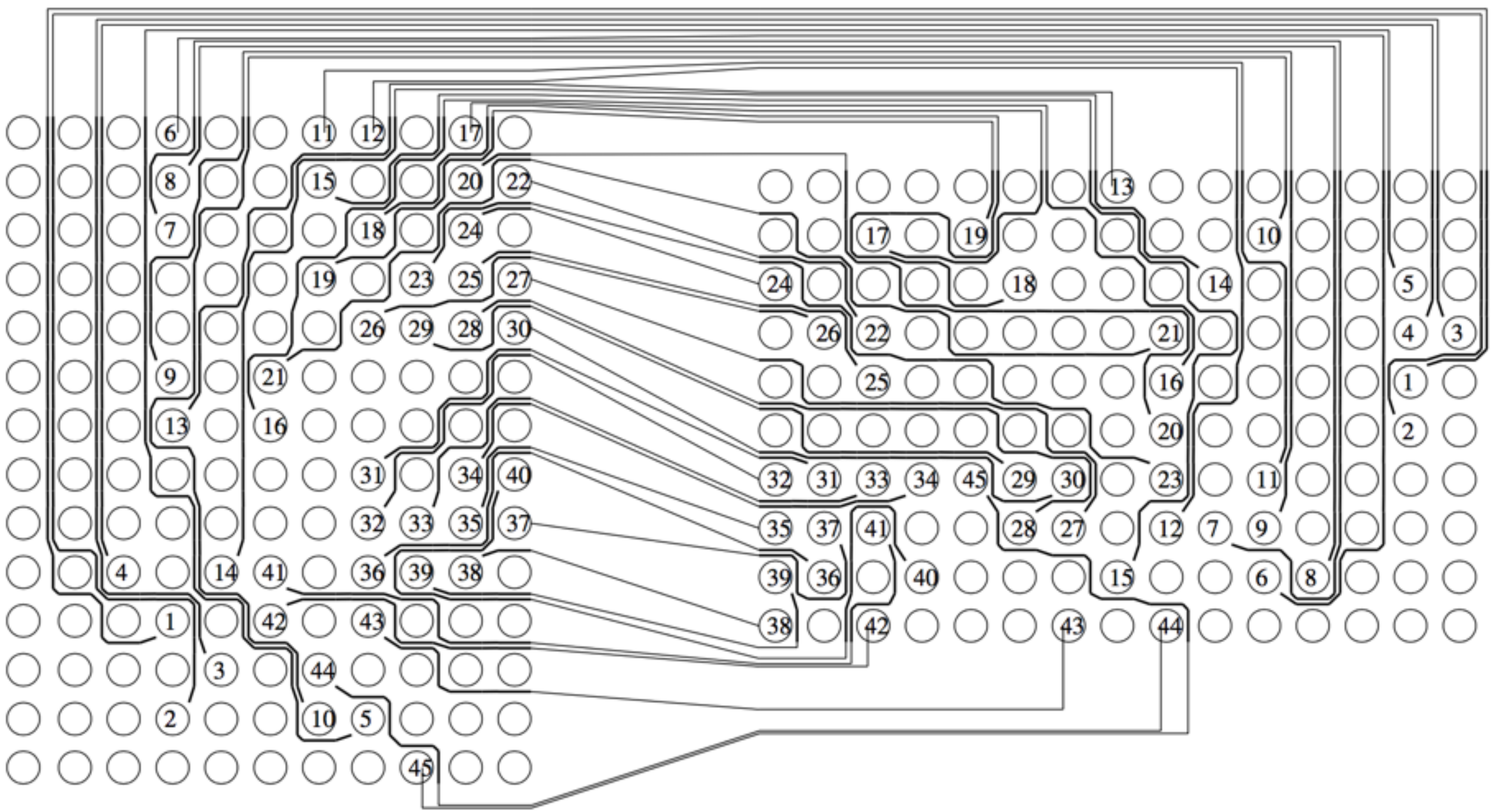
- Over solid ground, inductive & capacitive crosstalk are qual
  - Forward crosstalk cancel
  - Reverse crosstalk reinforce
- Over a slotted or imperfect ground plane, inductive coupling exceeds capacitive coupling
  - Forward crosstalk large and negative
- Forward crosstalk is like a square pulse
  - constant height & duration 2Tp
- Reverse crosstalk when it hits a low impedance driver, reflects towards the far-end

Modern PCB Design — 2



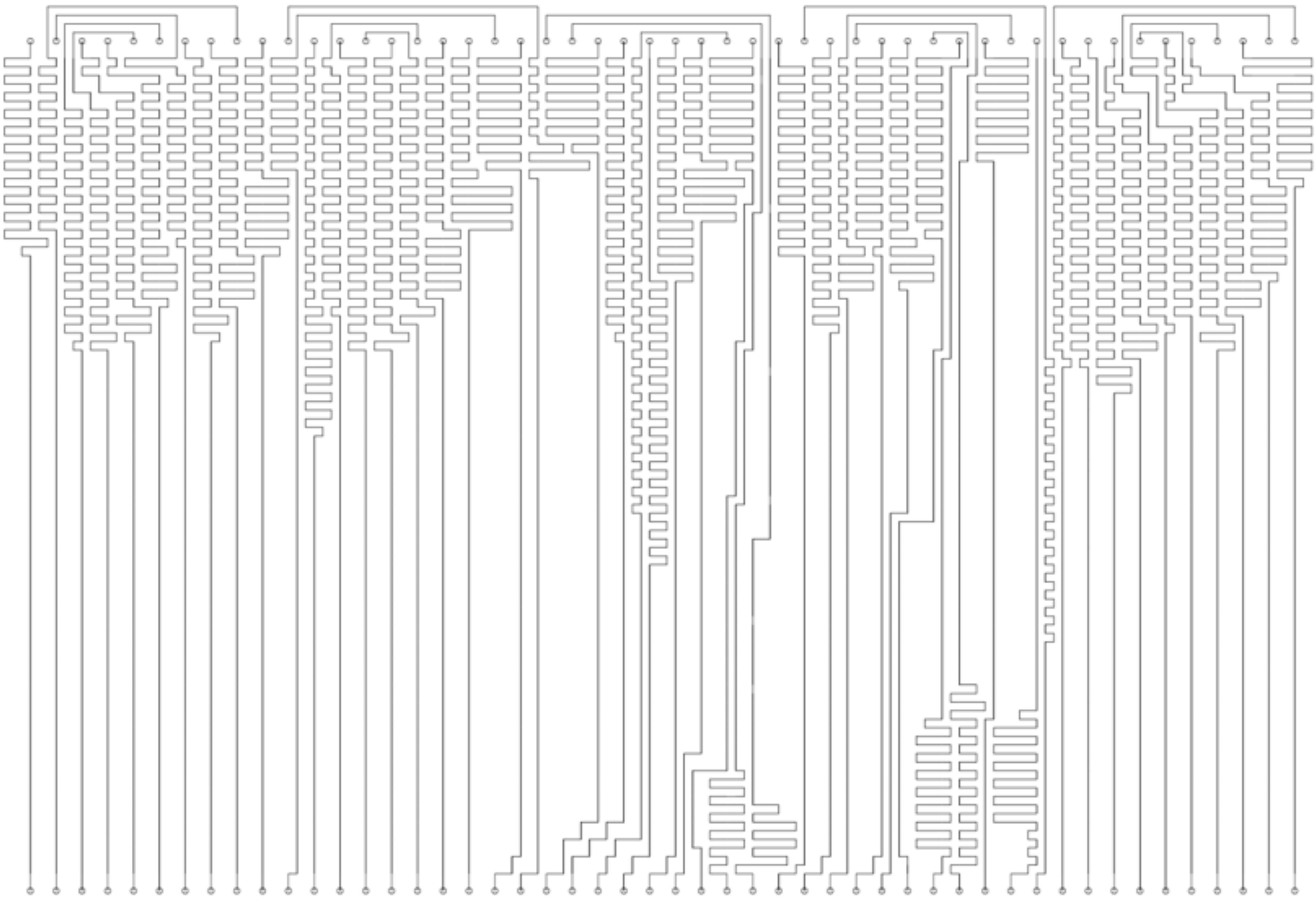
Escape Routing
[Tan et al. DAC'2009]

Modern PCB Design — 3



Simultaneously Escape Routing [Luo et al. ISPD'2010]

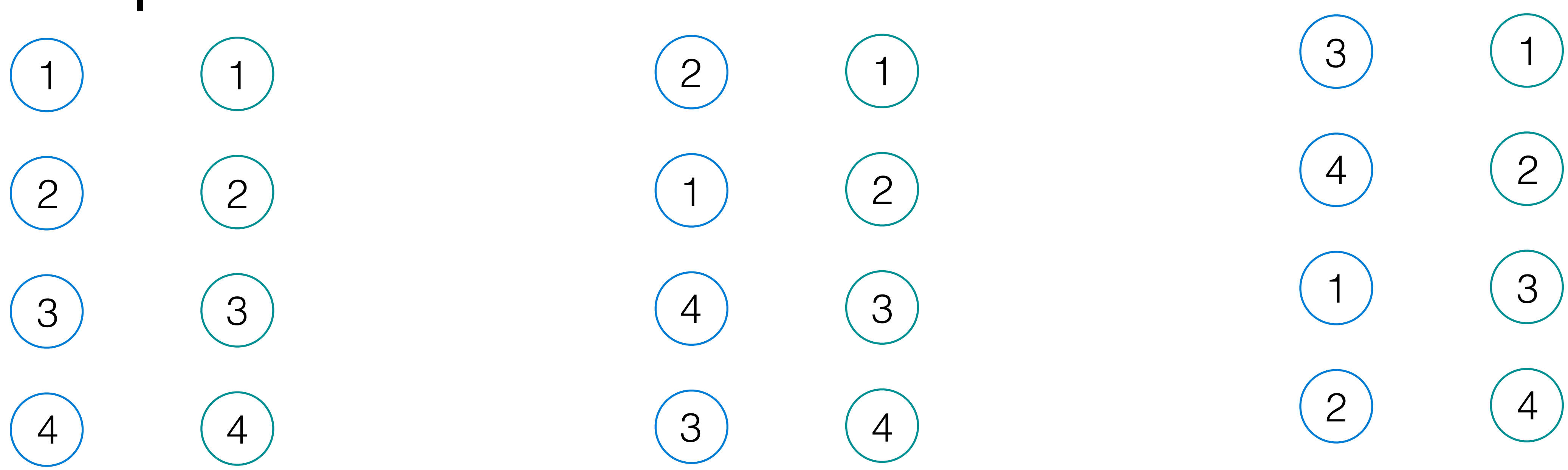
Modern PCB Design — 4



Untangling Twisted Nets + Length-Matched Routing [Tan et al. ICCAD'2007]

One-Side Untangle Twisted Nets

- Route left side pins to the right side pins
  - ✦ Each pin has an ID.
  - ✦ Planar routing
  - ✦ Only untangle the twisted nets on the left-side
- Example:



How to automatically handle extreme large cases?

Stacking Circuit Board Layers

- Need to specify
  - Which are the power, ground and signal layers
  - Dielectric constant of the substrate
  - Spacing between layers
  - Desire trace dimensions and minimum trace spacing
- Power & Ground Planning
  - Choose solid, hatched or finger ground plane model
  - Use ground & power planes in pair
  - Symmetric pairing in a layer stack helps prevent wrapping
  - Both ground & power planes may be used as low-inductance signal return paths
  - Adequate bypass capacitors between ground and power planes

Selecting Trace Dimensions

- Dense design requires fewer layers but
- Smaller, more closely spaced traces also yield more crosstalk and power-handling capacity problem
- Power-handling capacity depends on
  - Cross sectional area
  - Allowable temperature rise (amount of power dissipated)
- Power is not a problem for a large distribution bus
  - is a big problem for extremely small trace
- High density will lower yield, thus increase cost
  - avoid using minimum attainable line width
- Other factors:
  - Control etching process to avoid wide line width variations to control the impedance

Routing Density versus Layer

- More layer will cost more but easier to lay
- From experience
  - Divide the circuit into quadrants, half of the wires will stay with a quadrant
  - Same statistics when this quadrant is further subdivided into quadrants
  - Average wire length = spacing between quadrants

Thank You