CENG4480 Homework 3

Solutions

Q1 Elaborate and examplify the differences between Combinational and Sequential Circuit.

A1 *Scatch.* Sequential logic is related to time. NAND, NOR, XOR are all combinational circuit. Examples of Sequential circuit include D-type Trigger, Counter and Finite State Machine.

Q2 What is the modern memory hierarchy? Analysis the properties of each hierarchy level.

A2 *Hint*. Analyze from speed, cost, storage...

Q3 For the given SR Latch Fig. 1. Draw the waveform of Q if S, R, and E(Clk) have the input shown in Fig. 2

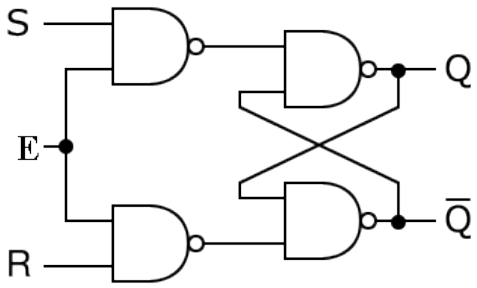

Figure 1: Gated SR Latch

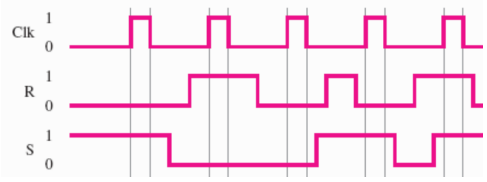

Figure 2: Gated SR Latch

A3 As shown in Fig. 3

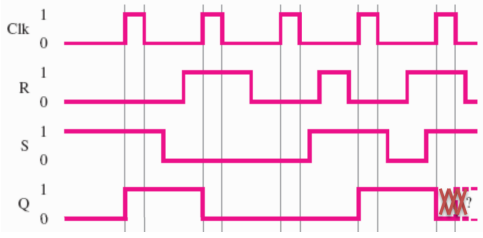

Figure 3: A2

Q4 Show the differences between DRAM and SRAM and which level of hierarchy of memory are they employed.

A4 Trivial.

Q5 Design a finite state machine to detect the pattern of "11010" in the bit stream. How many states are required? Draw the state transition graph.

A5 As shown in Fig. 4

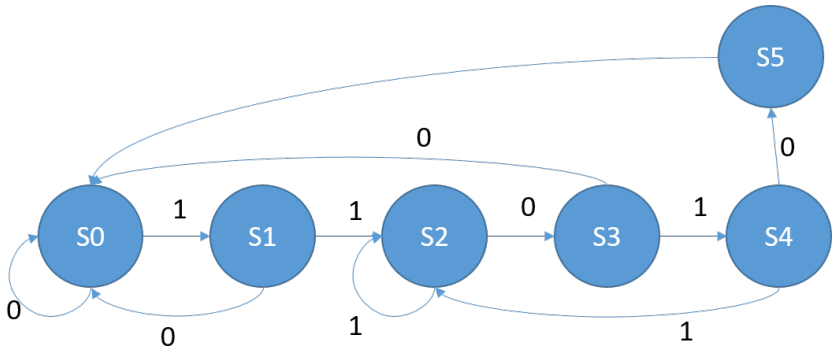

Figure 4: A5

Q6 (a) What is setup time?
(b) How is clock skew generated? (c) How to alleviate clock skew?

A6 Trivial.

Q7 Explain the working principle of the following register (Fig. 5) and show that the circuit is not sensitive to clock skew.

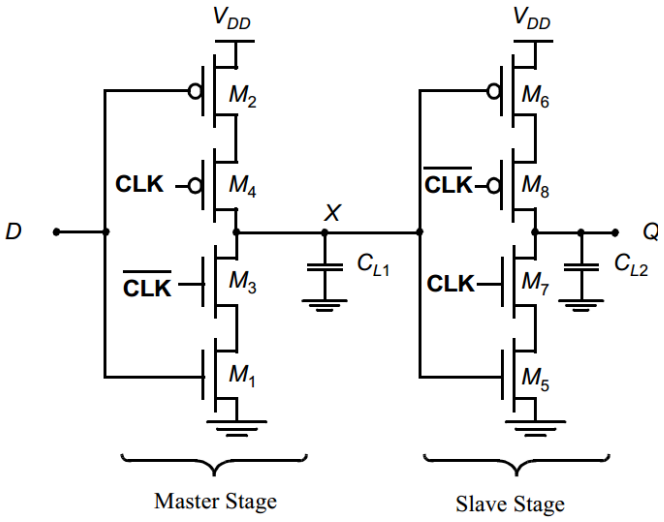

Figure 5: Sample Register.

A7 (1) **a**. $CLK = 0$ ($\overline{CLK} = 1$): The first stage is turned on, and the master stage acts as an inverter sampling the inverted version of D on the internal node X. Meanwhile, the slave section is in a high-impedance mode, or in a hold mode. Both transistors M_7 and M_8 are off, decoupling the output from the input. The output Q retains its previous value stored on the output capacitor C_{L2}. **b**. The roles are reversed when $CLK = 1$: The master stage section is in hold mode (M_3 and M_4 off), while the second section evaluates (M_7 and M_8 on). The value stored on C_L1 propagates to the output node through the slave stage which acts as an inverter.
(2) To show the circuit is insensitive to skew, we examine when CLK and $\overline{CLK}$ are both 0 and 1. In the (0-0) overlap case, the circuit simplifies to the network shown in Fig. 6(a) in which both PMOS devices are on during this period. The question is does any new data sampled during the overlap window propagate to the output Q. This is not desirable since data should not change on the negative edge for a positive edge-triggered register. Indeed new data is sampled on node X through the series PMOS devices M2-M4, and node X can make a 0-to-1 transition during the overlap period. However, this data cannot propagate to the output since the NMOS device M7 is turned off. At the end of the overlap period, CLK=1 and both M7 and M8 turn off, putting the slave stage is in the hold mode. Therefore, any new data sampled on the falling clock edge is not seen at the slave output Q, since the slave state is off till the next rising edge of the clock. As the circuit consists of a cascade of inverters, signal propagation requires one pull-up followed by a pull-down, or vice-versa, which is not feasible in the situation presented. (1-1) overlap case can be analyzed similarly as shown in Fig. 6(b).

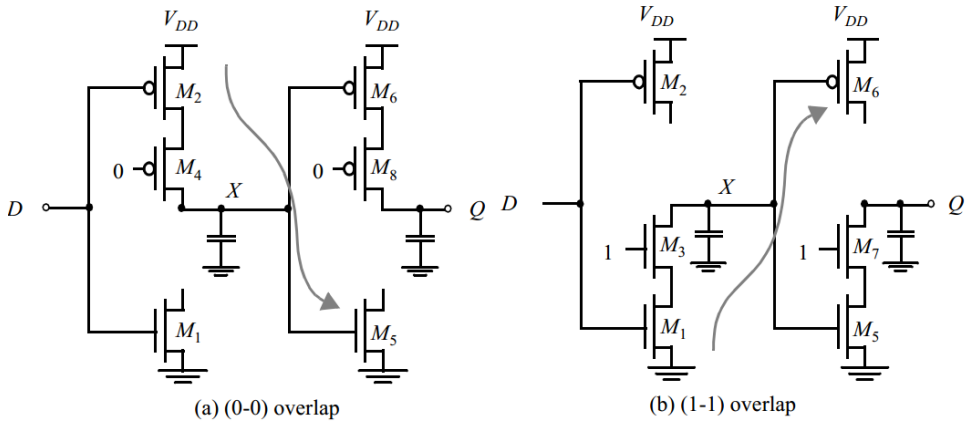

Figure 6: A7.

Q8 Explain cross-talk and approaches to eliminate cross-talk.

A8 *Hint*. by-pass, guard traces,...