

# CENG 4480

## Lecture 11: Clock

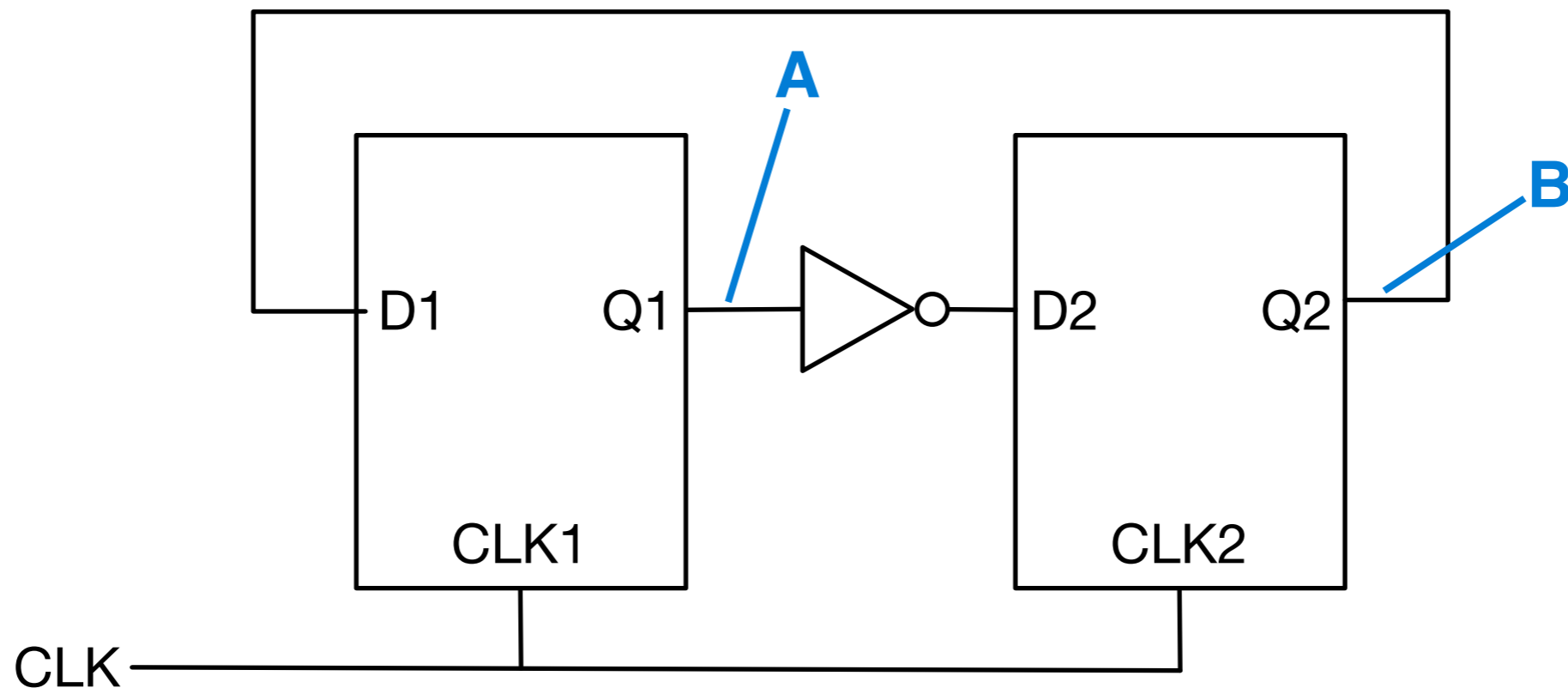
**Bei Yu**

### **Reference:**

- **Chapter 11 Clock Distribution**
- **High speed digital design**
- by Johnson and Graham

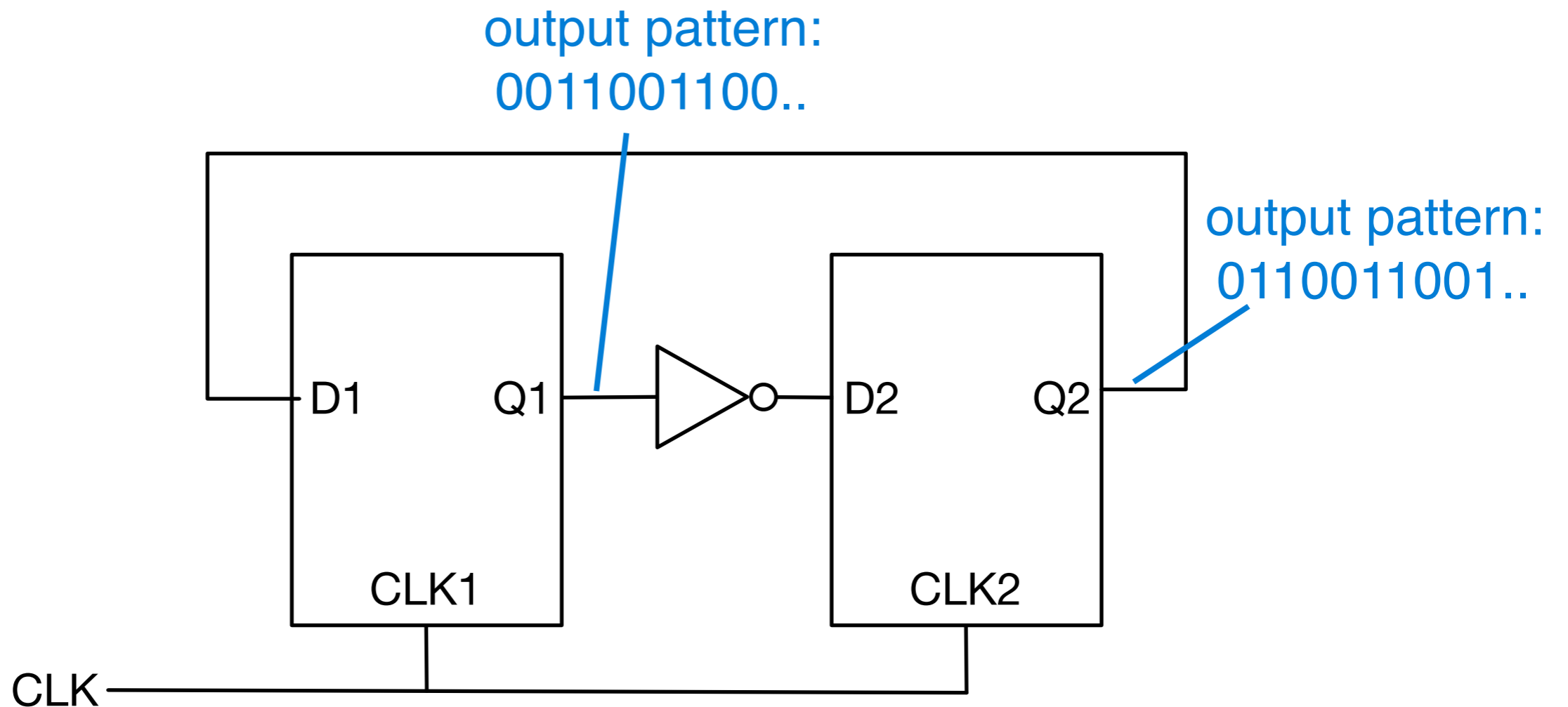
# A 2-bit ring counter example

- 2-bit ring counter
- Initially  $A = B = 0$ ;  $A = 0011001100$
- What is  $B$ ?



# A 2-bit ring counter example

- The result is Okay when clock is **slow**
- But, when clock is **TOO fast**, get some **problem**

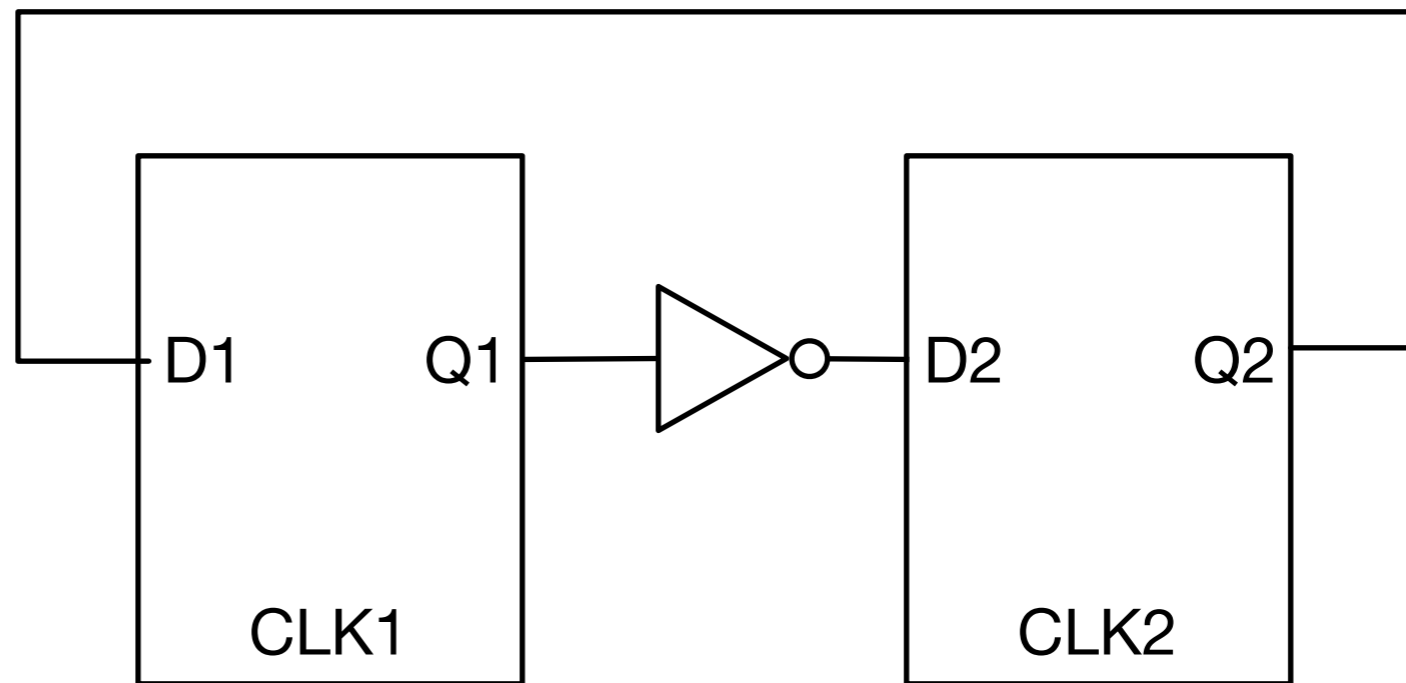


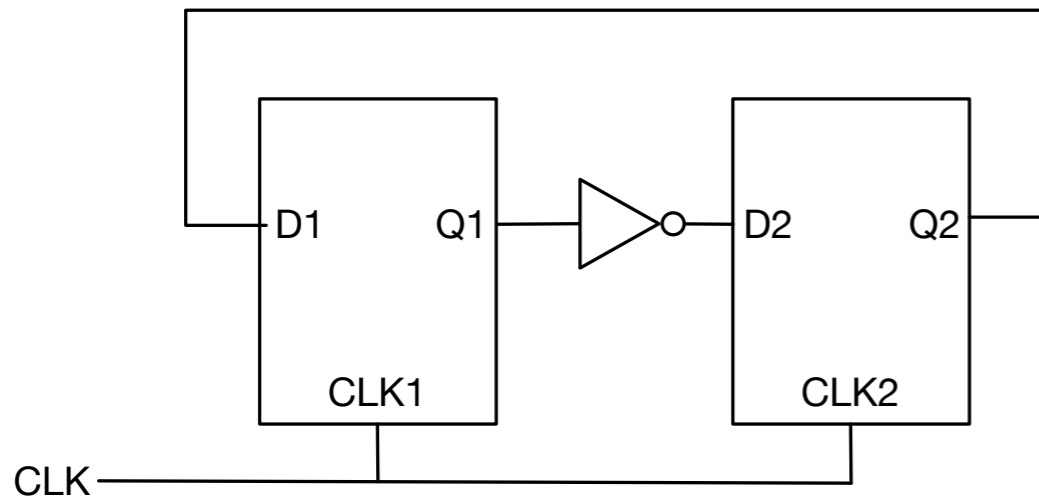
# Setup Time and Time Margin

- **Setup Time**: The time that the input data must be stable before the clock transition of the system occurs
- **Time Margin**: measures the **slack**, or excess time, remaining in each clock cycle
  - ◆ Protects your circuit against signal cross-talk, miscalculation of logic delays, and later minor changes in the layout
  - ◆ Depends on both time delay of logic paths and clock interval

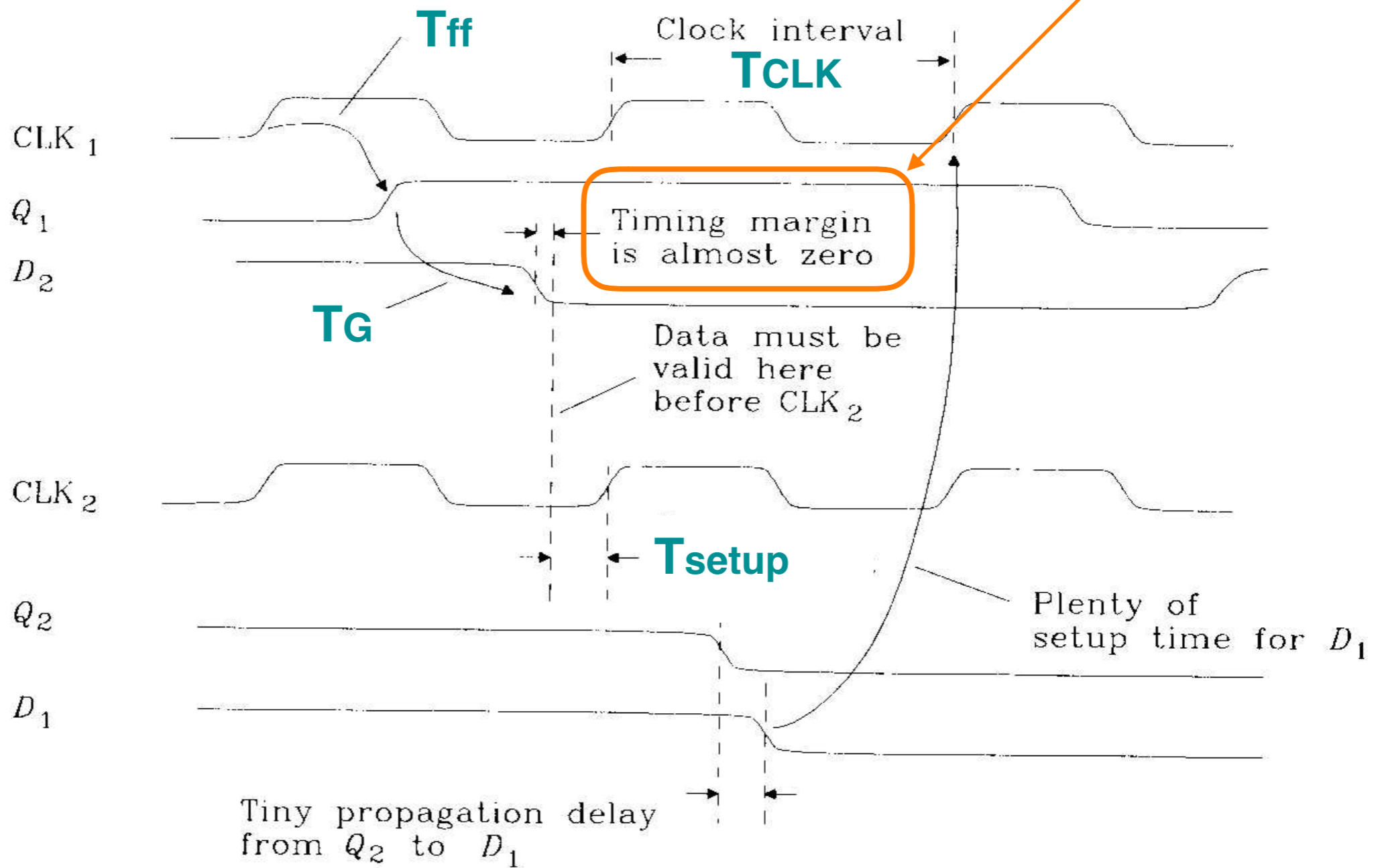
# Notations in Clock Skew Calculation

- **$T_{ff}$** : delay of flip-flop (FF)
- **$T_G$** : delay of gate G, including track delay
- **$T_{setup}$** : worst-case setup time required by FF2, data at D2 must arrive at least  $T_{setup}$  before  $CLK_2$
- **$T_{CLK}$** : clock period; interval between clocks



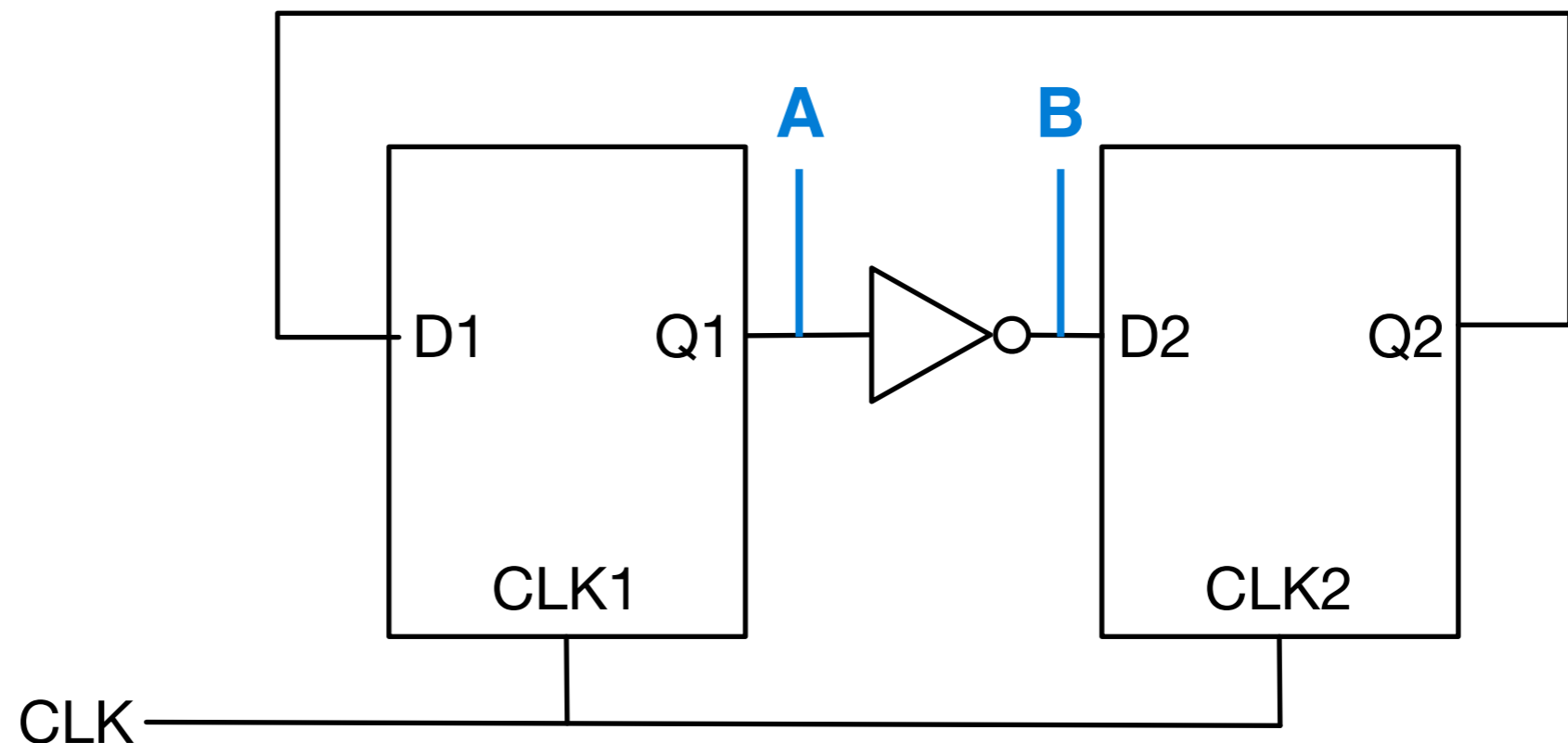


May cause problem if  $T_{CLK}$  is too small



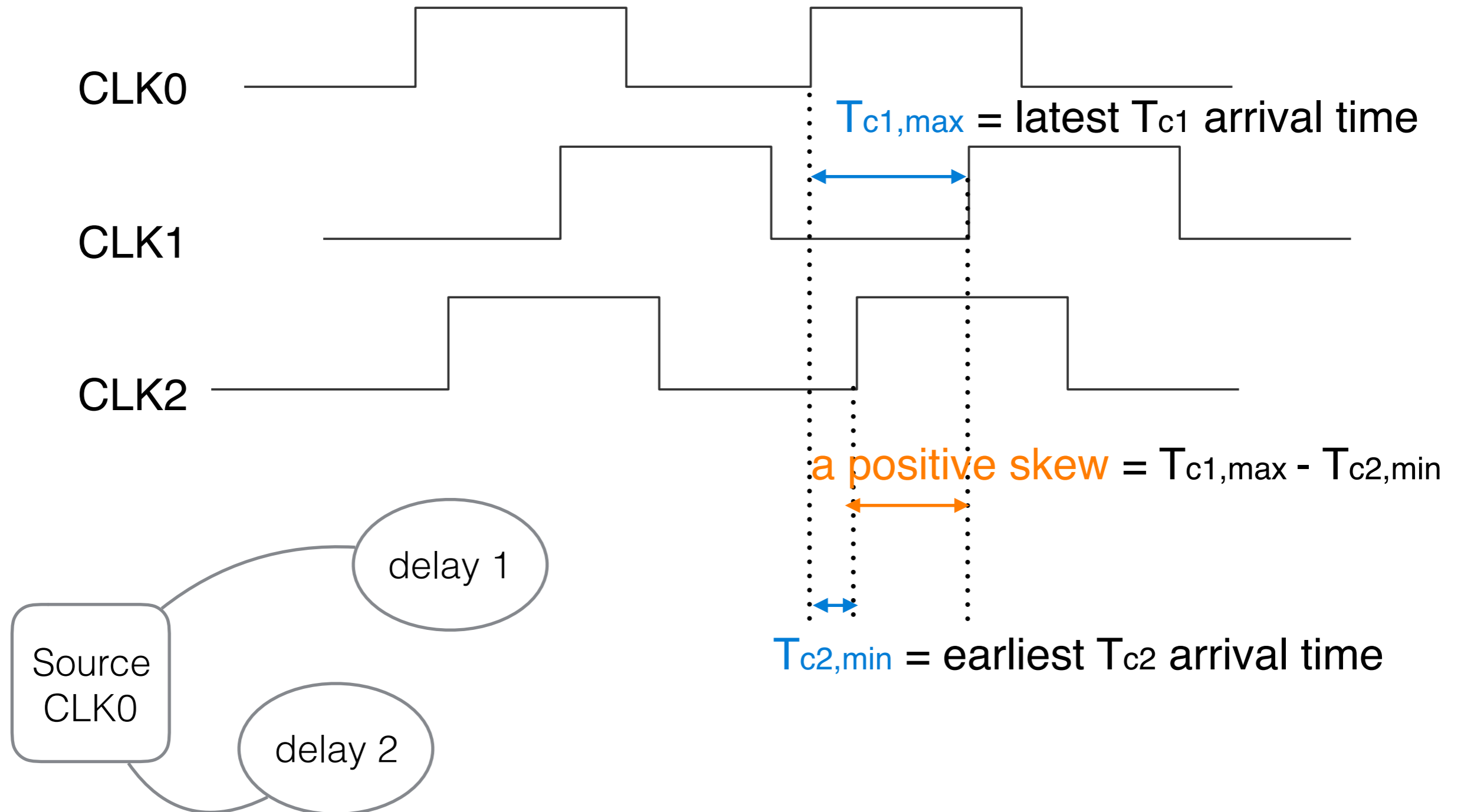
# EX. B2-1

- $\text{CLK1} = \text{CLK2} = 20\text{MHz}$ ;  $T_{\text{ff}} = 8\text{ns}$ ;  $T_{\text{setup}} = 5\text{ns}$ ;  $T_{\text{G}} = 10\text{ns}$ .
- **Questions:**
  - ♦ Find time margin
  - ♦ How many delay G gates can you insert between A and B without creating error?



# Clock Skew

- The clock does NOT reach FF1, FF2 at the same time





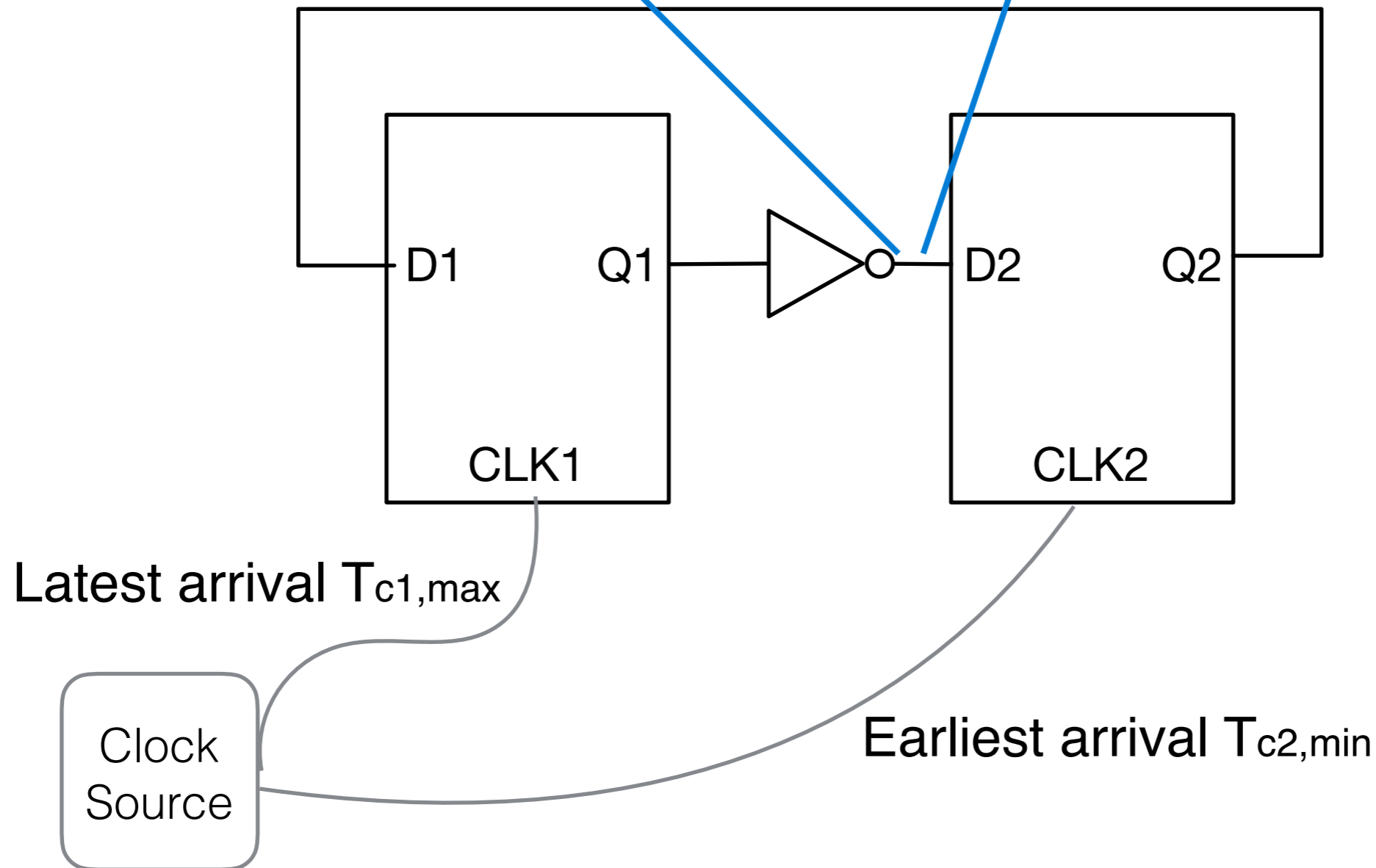
# Why Care Clock Skew?

Signal arrives here no later than

$$T_{c1,max} + T_{ff} + T_G$$

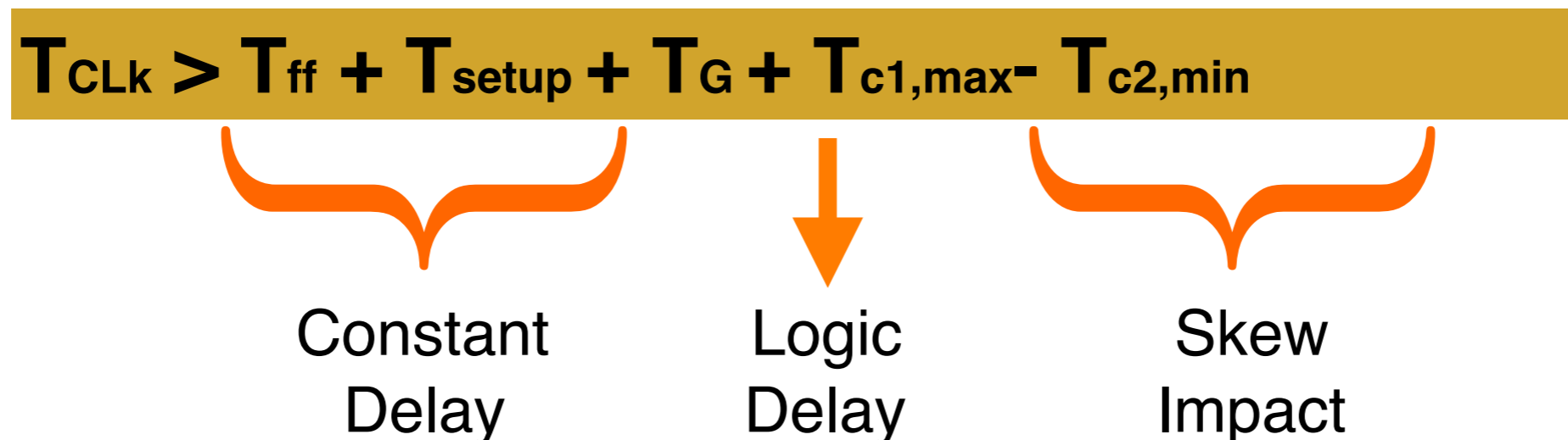
Signal arrives must be valid before next clock

$$T_{CLK} + T_{c2,min} - T_{setup}$$



# Why Care Clock Skew?

- $T_{\text{delay}} = T_{c1,\text{max}} + T_{\text{ff}} + T_{\text{G}}$
- $T_{\text{clk}'} = T_{\text{CLK}} + T_{c2,\text{min}} - T_{\text{setup}}$
- Since  $T_{\text{delay}} < T_{\text{clk}'} \Rightarrow$



# EX. B2-2

Question: Given

- $T_{ff} = 7\text{ns};$
- $T_G = 5\text{ns};$
- $T_{\text{setup}} = 4\text{ns};$
- $T_{CL} = 40\text{MHZ};$

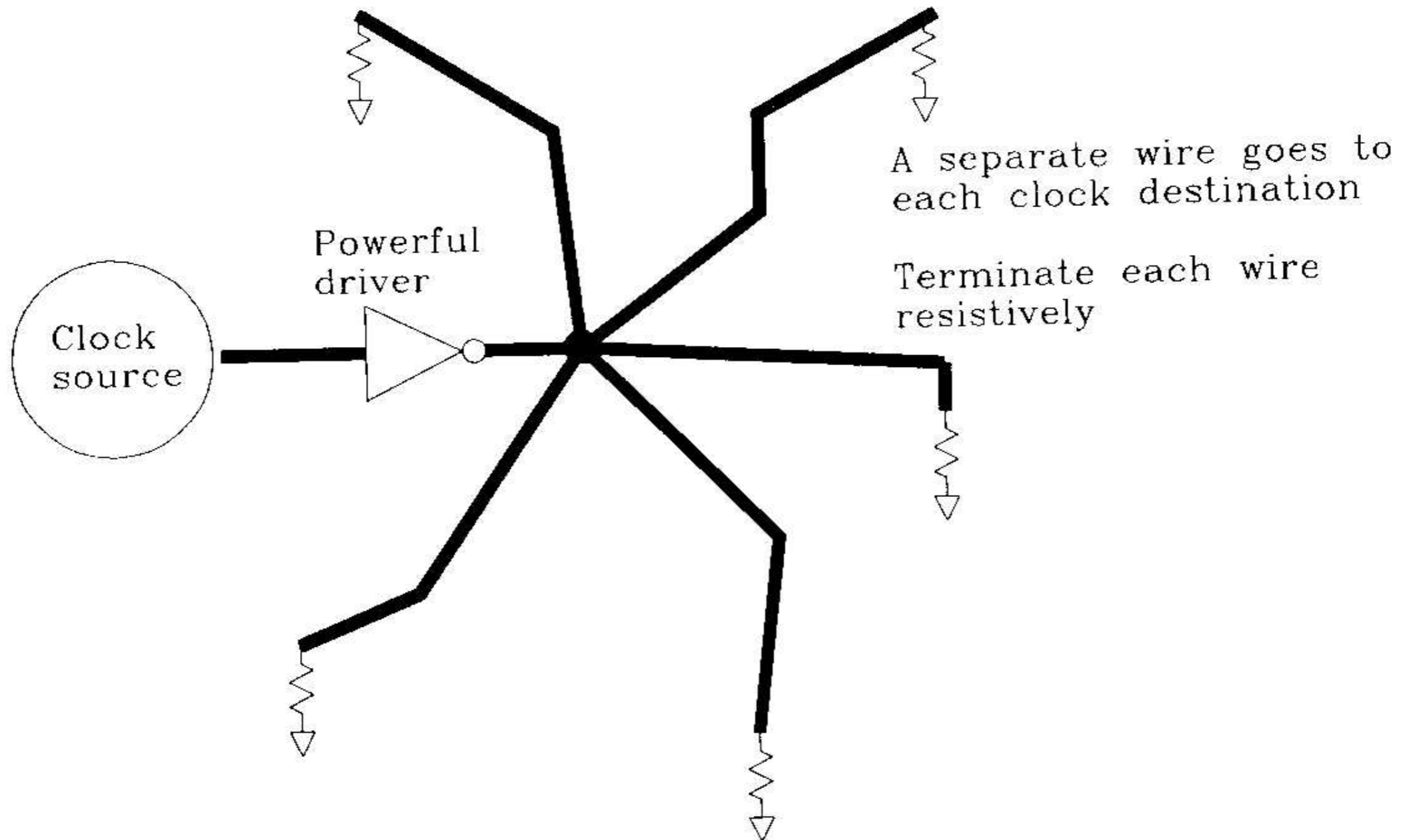
What's the biggest time skew allowed?

Answer:

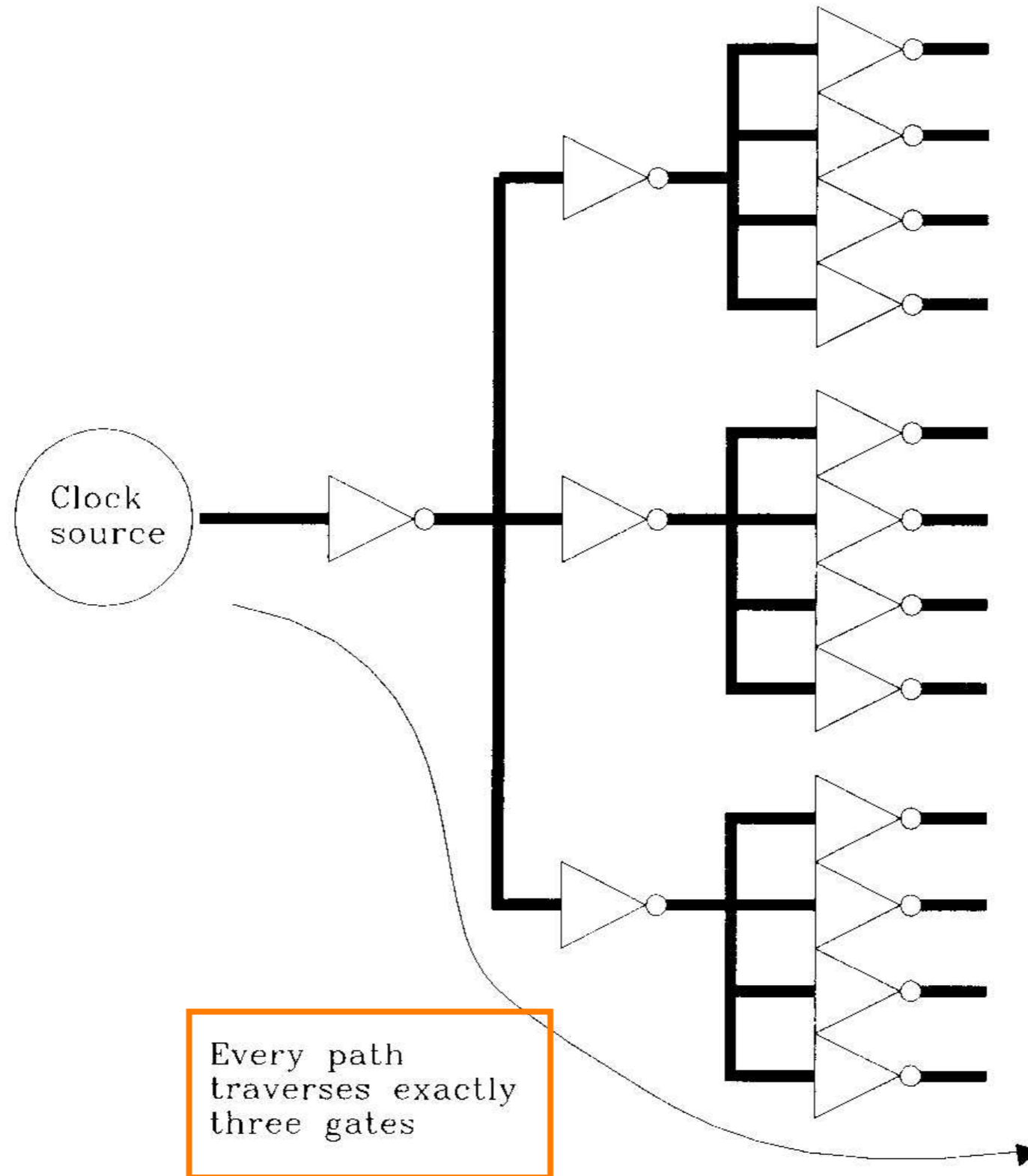
# Strategies to reduce clock skew

- Drive them from the **same** source & balance the delays
- **Style 1**: Spider-leg distribution network
  - ♦ use a power driver to drive N outputs.
  - ♦ Use load (R) termination to reduce reflection if the traces are long (distributed circuit). Total load =  $R/N$ .
  - ♦ Two or more driver outputs in parallel may be needed.
- **Style 2**: Clock distribution tree

# Style 1: Spider-leg Clock

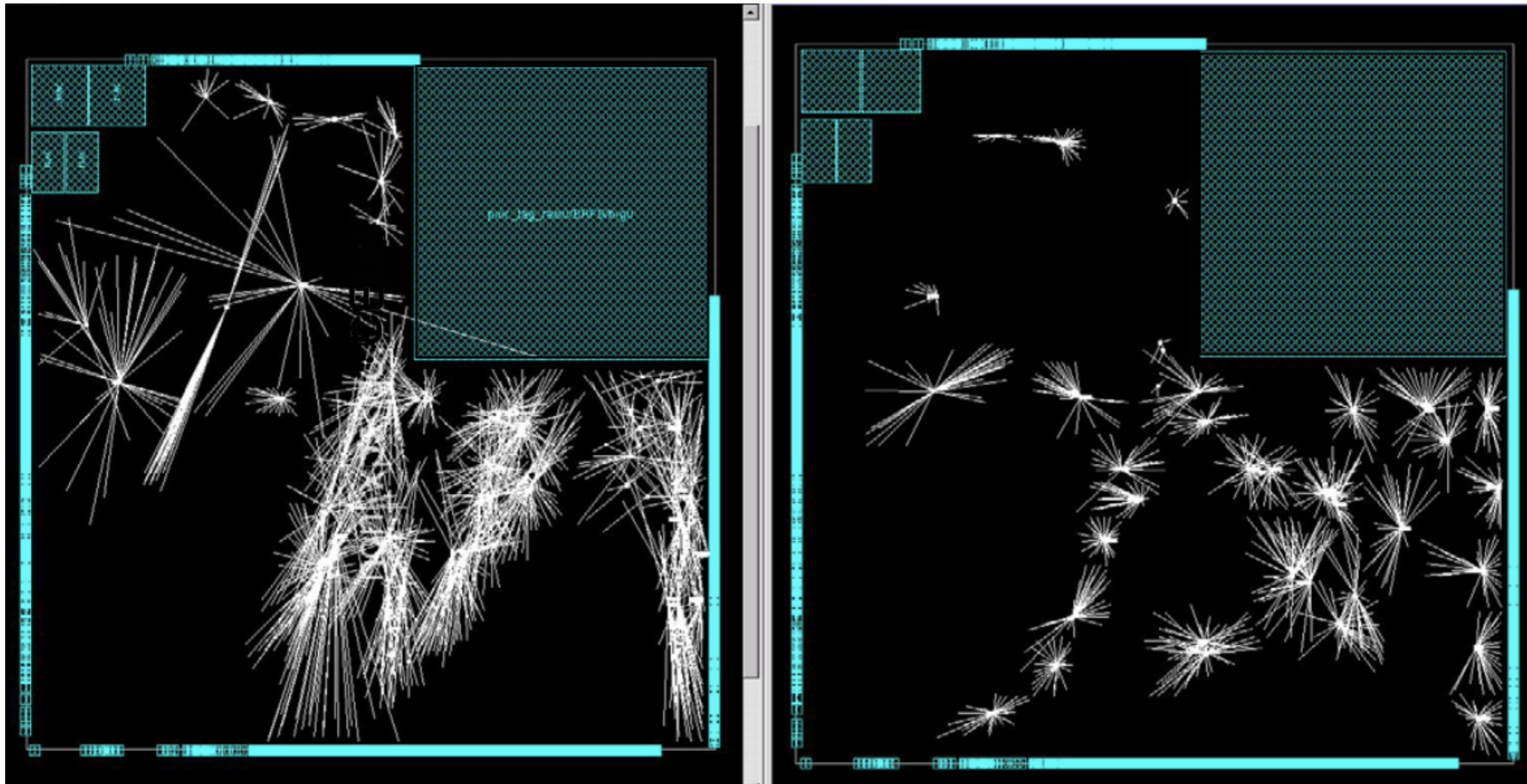


# Style 2: Clock Tree



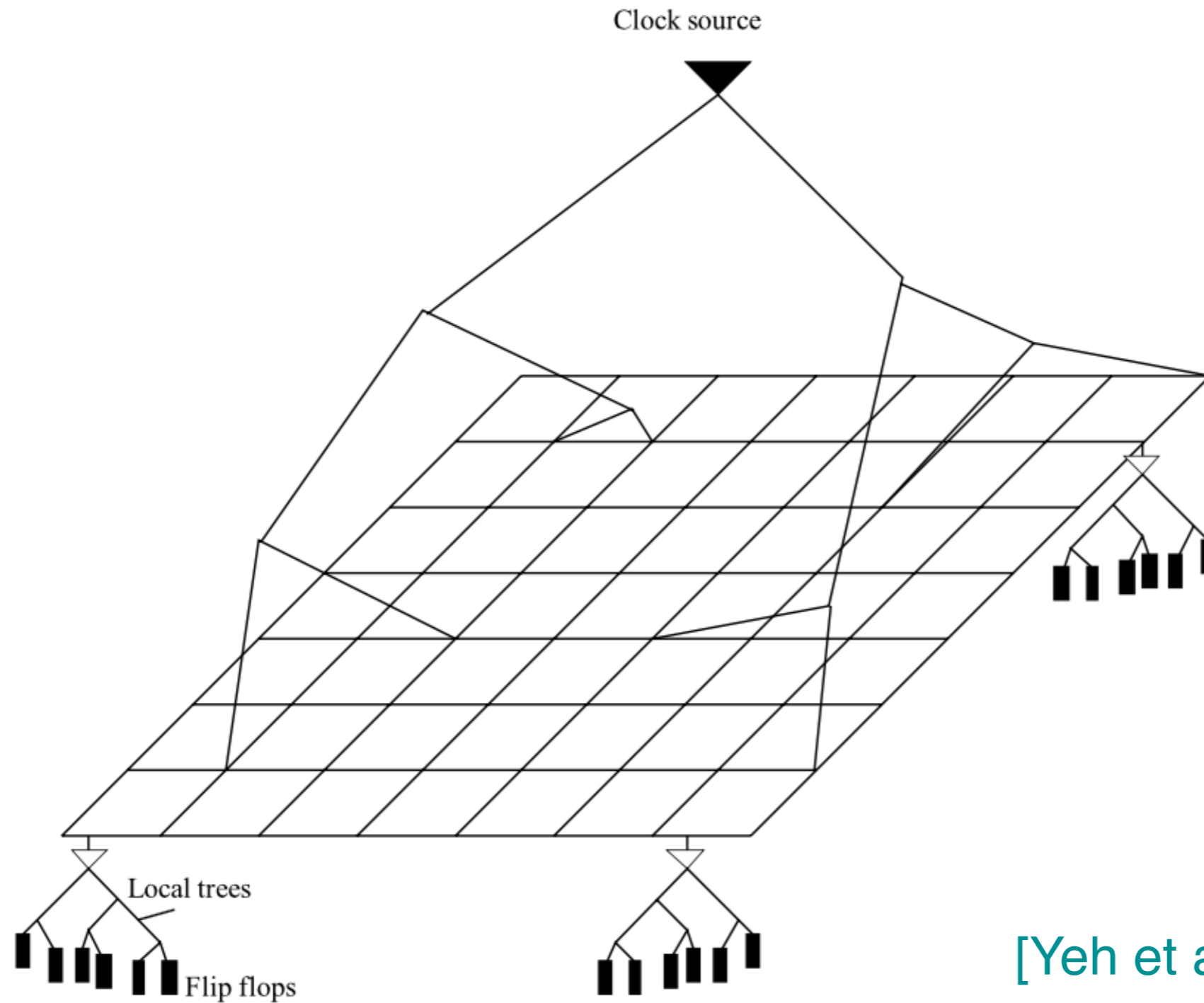


# Modern Clock Design — 1



[Ho et al, ISPD'2009]

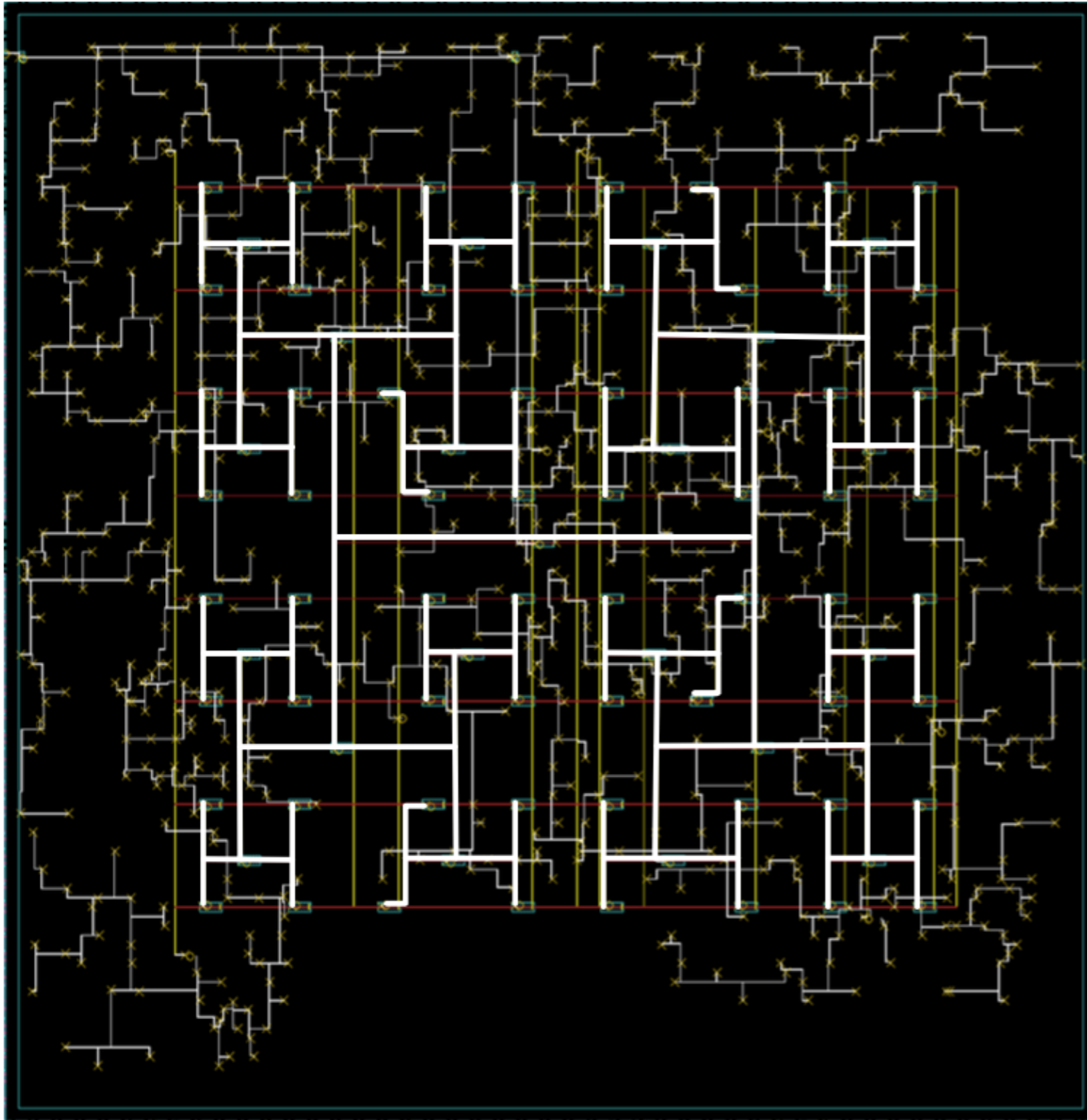
# Modern Clock Design — 2



[Yeh et al, ISQED'2006]

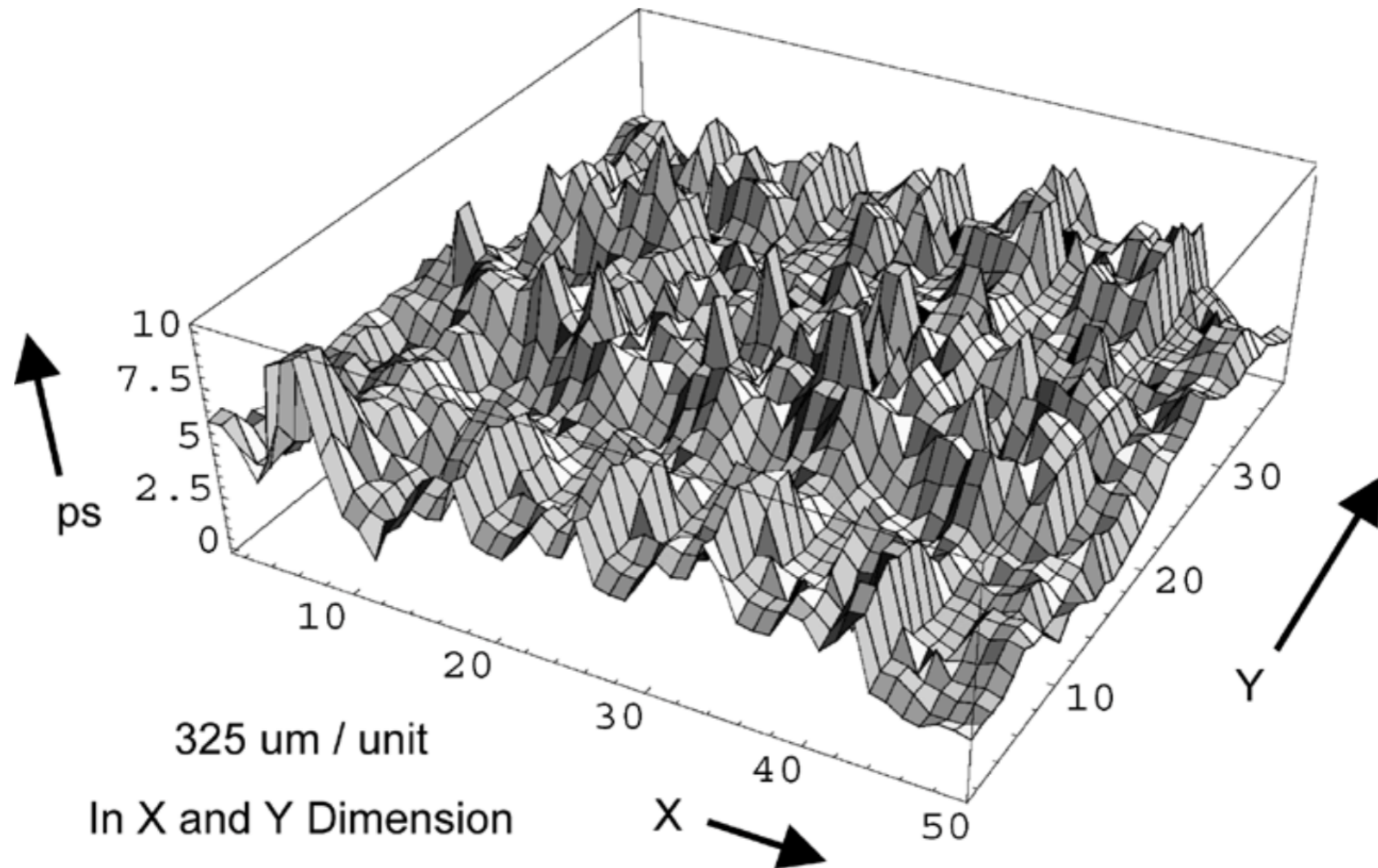


# Modern Clock Design — 3



[Seok et al, ISLPED'2010]

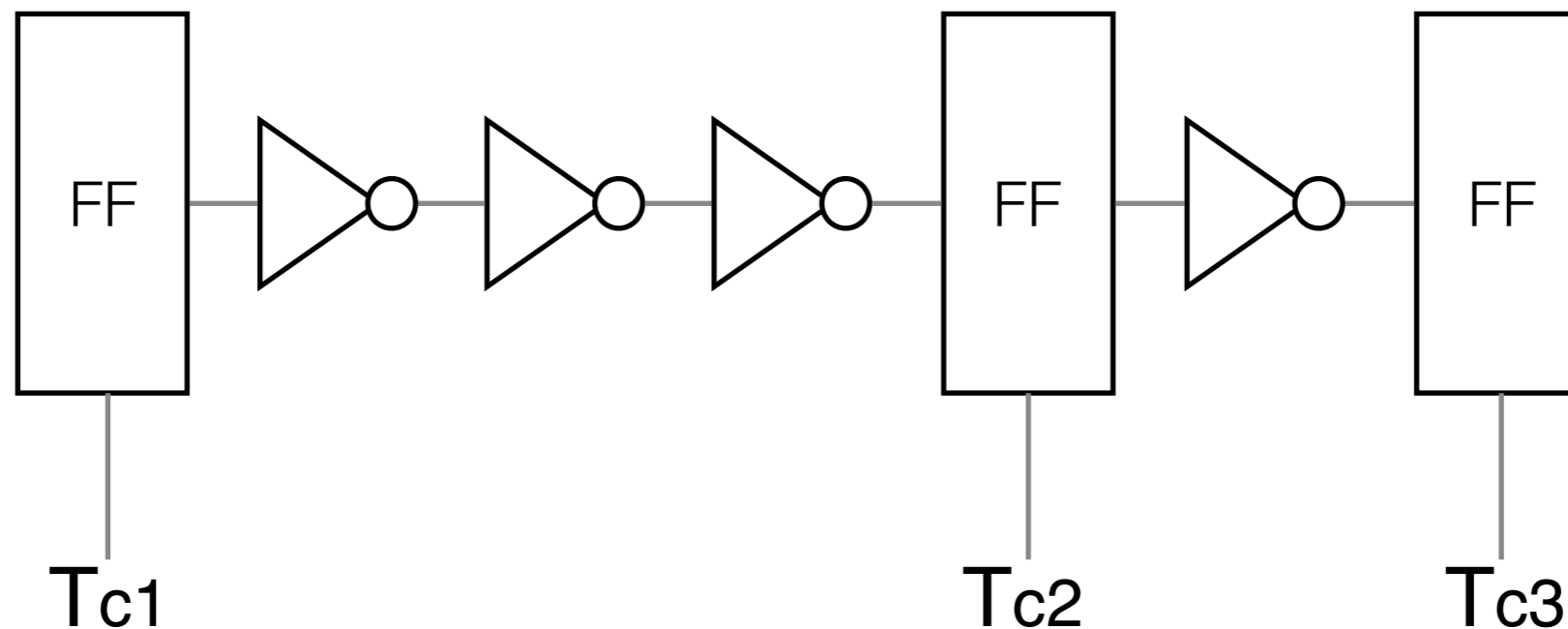
# Clock Skew Distribution



[Pham et al, JSSC'2006]

# EX. Skew Optimization

- Instead of Zero-Skew, take advantage of Skew.
- **Question:** Given  $T_G=6\text{ns}$ ,  $T_{ff}=10\text{ns}$ ,  $T_{\text{setup}}=2\text{ns}$ , what's the minimal  $T_{\text{CLK}}$ ? Assume  $T_{c3} = 0$ .



Thank You