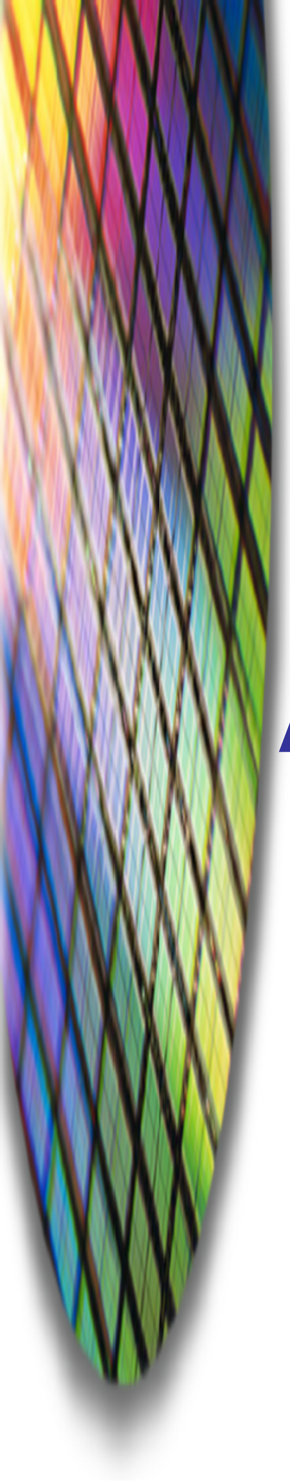

# Concurrent Guiding Template Assignment and Redundant Via Insertion for DSA-MP Hybrid Lithography

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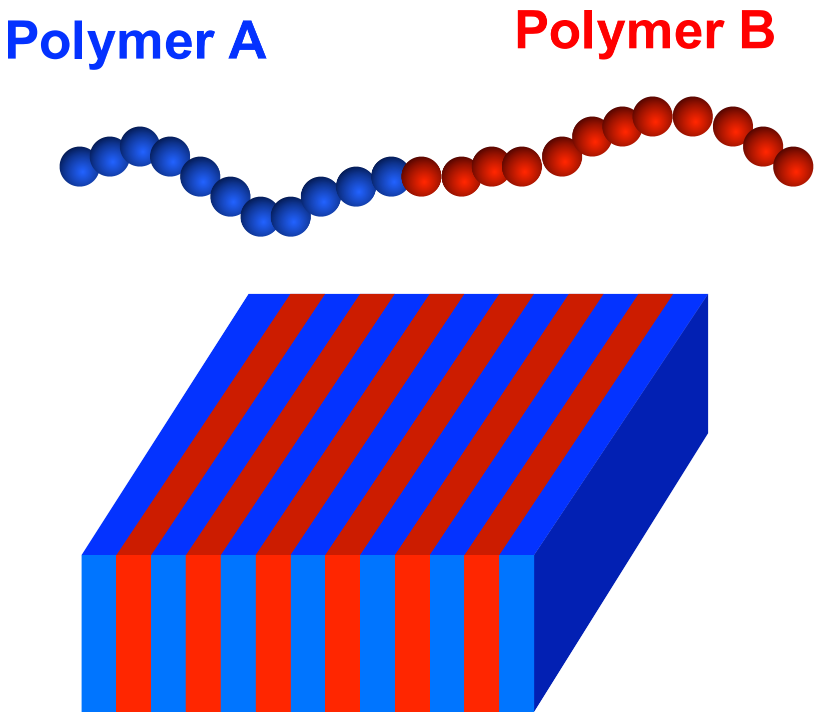
# Outline

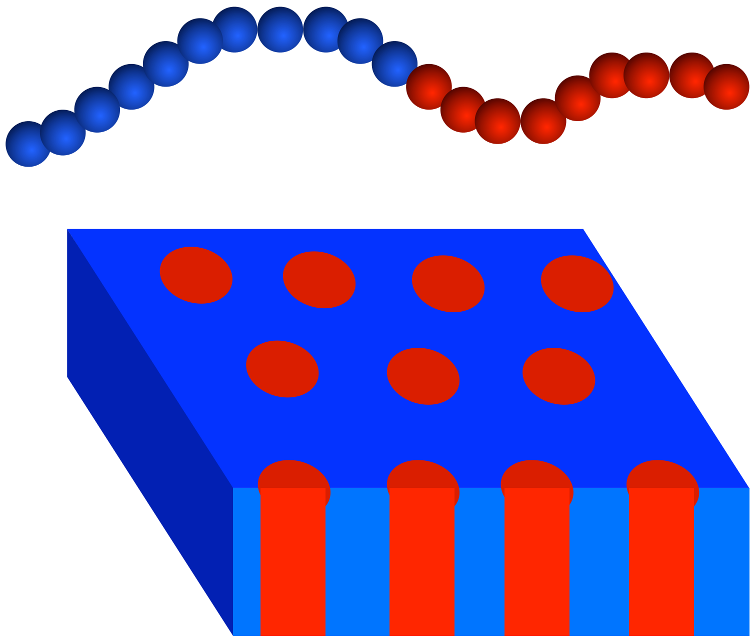
- Introduction
- Problem Formulation
- Algorithms
- Experimental Results
- Conclusion

# What is Directed Self-Assembly ?

- **Self Assembly**
  - Enabled by block copolymers (BCPs)
- Block Copolymers (BCPs)
  - Polymers composed of 2 or more homopolymer
  - Micro-phase separation through annealing
  - Morphology is determined by several factors



Lamellae

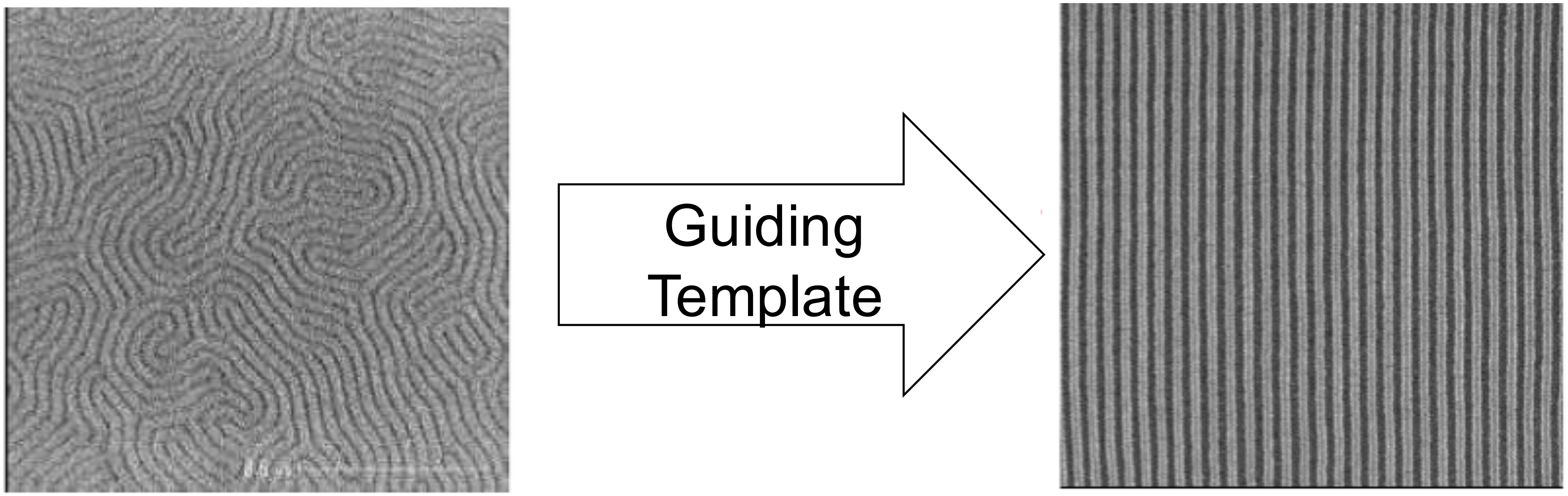


Cylinders

# What is Directed Self-Assembly ?

- **Direct** the Self Assembly process
  - No orientational order of the material
  - Given additional driving force to thermodynamics
  - Turn random “finger print” to oriented and aligned pattern

Directed Self-Assembly (DSA)

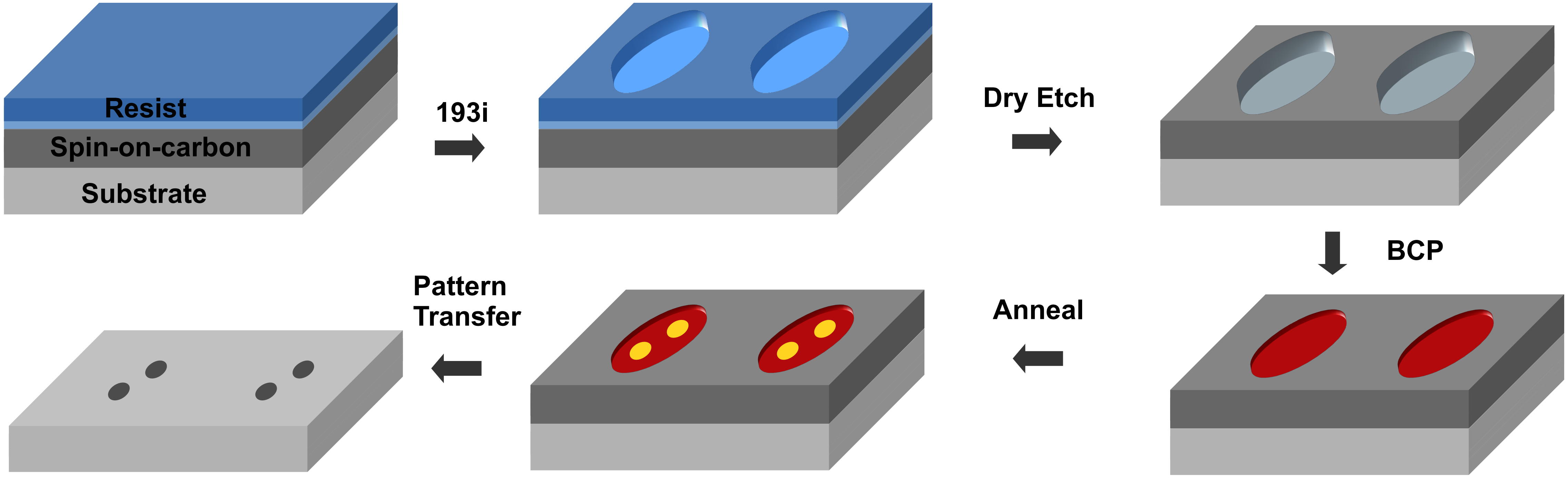


Guiding Template

*Figure source: J.W. Lee et al., DONGJIN SEMICHEM co., Ltd*

# Why DSA ?

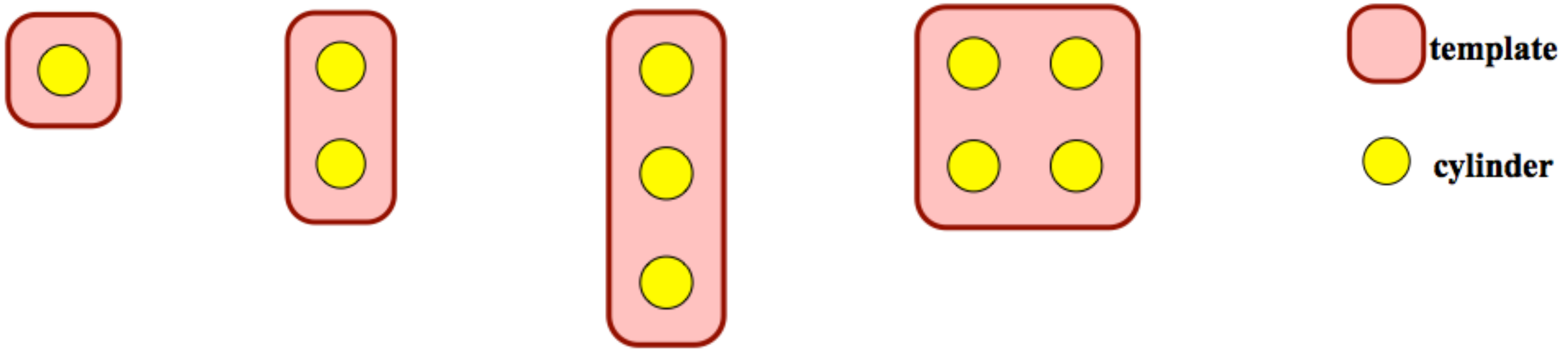
- Multiply pitch of line/hole patterns
- High throughput
- Potentially extend 193i lithography to 7nm at lower cost



Typical DSA manufacturing process

# DSA Pattern Properties

- Within-group contact/via distance
- Complex shapes are difficult to print
- Unexpected holes and placement error of holes for some patterns
- Pre-defined DSA pattern set to improve robust

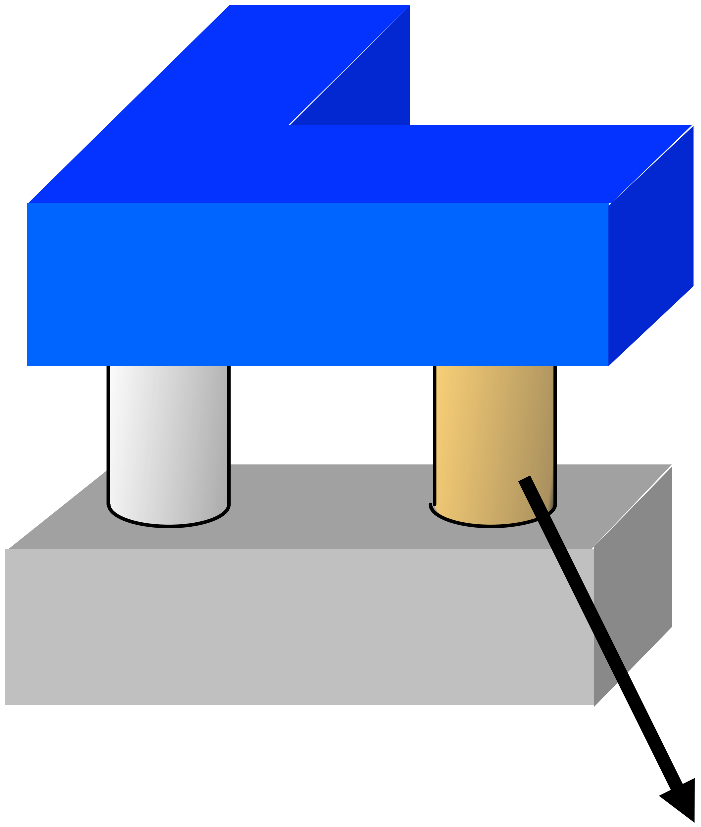


# Design Co-optimization of DSA Lithography

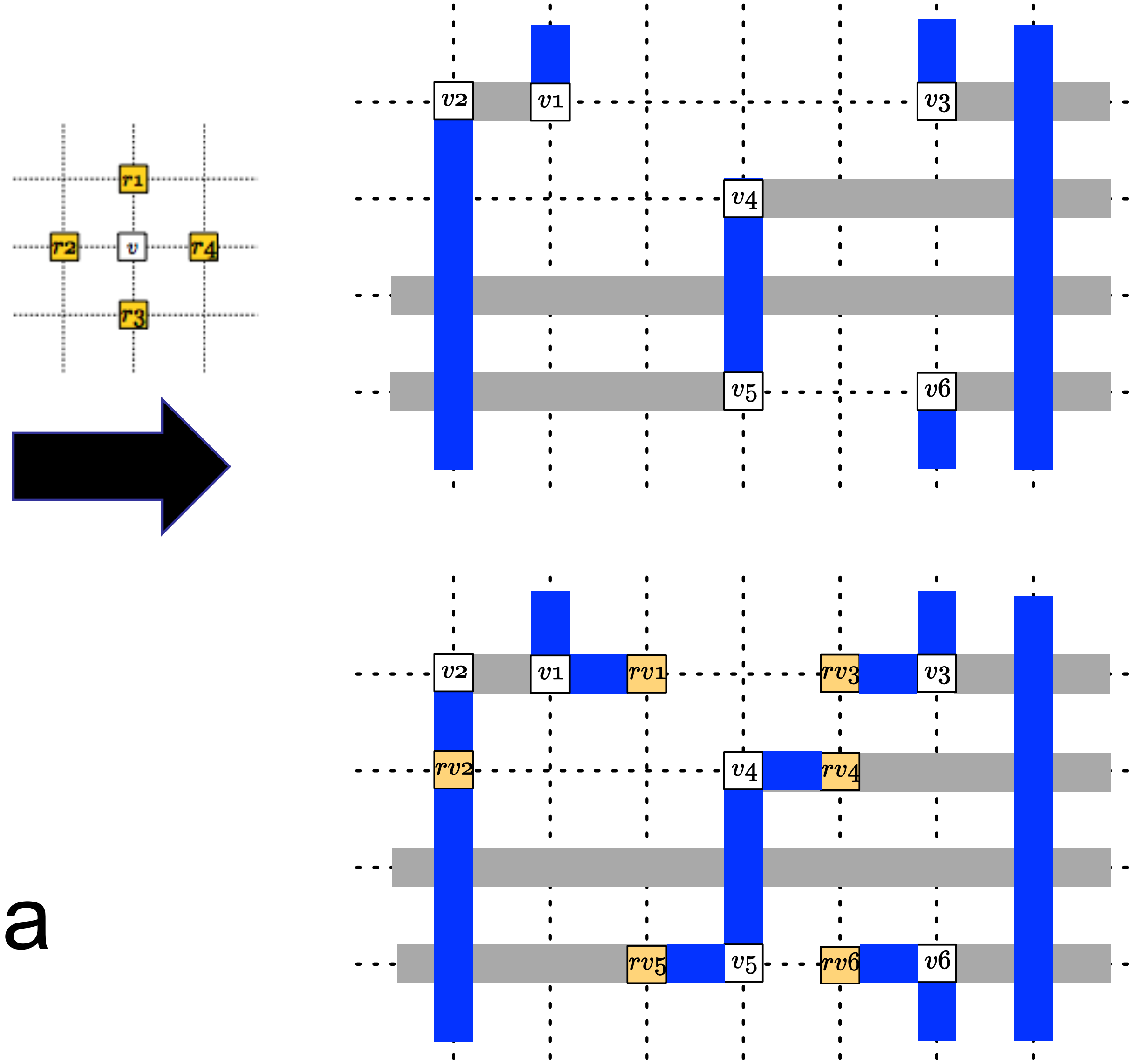
- To best use of DSA patterns
- To find optimal DSA-compatible design
- Previous related work on DSA co-design
  - Cut-mask optimization
    - [Xiao+, SPIE’13], [Ou+, GLSVLSI’15], [Lin+, ASPDAC’16]
  - Via layer optimization in standard cell library design
    - [Du+, ICCAD’13]
  - Mask decomposition
    - [Badr+, DAC’15], [Kuang+, ASPDAC’16], [Xiao+,ASPDAC’16]
  - Redundant via insertion
    - [Fang+, ICCAD’15]
  - Etc.

# Redundant Via Insertion (RVI)

- Insert an extra via near a single via
- Prevent via failure
- Improve circuit yield and reliability

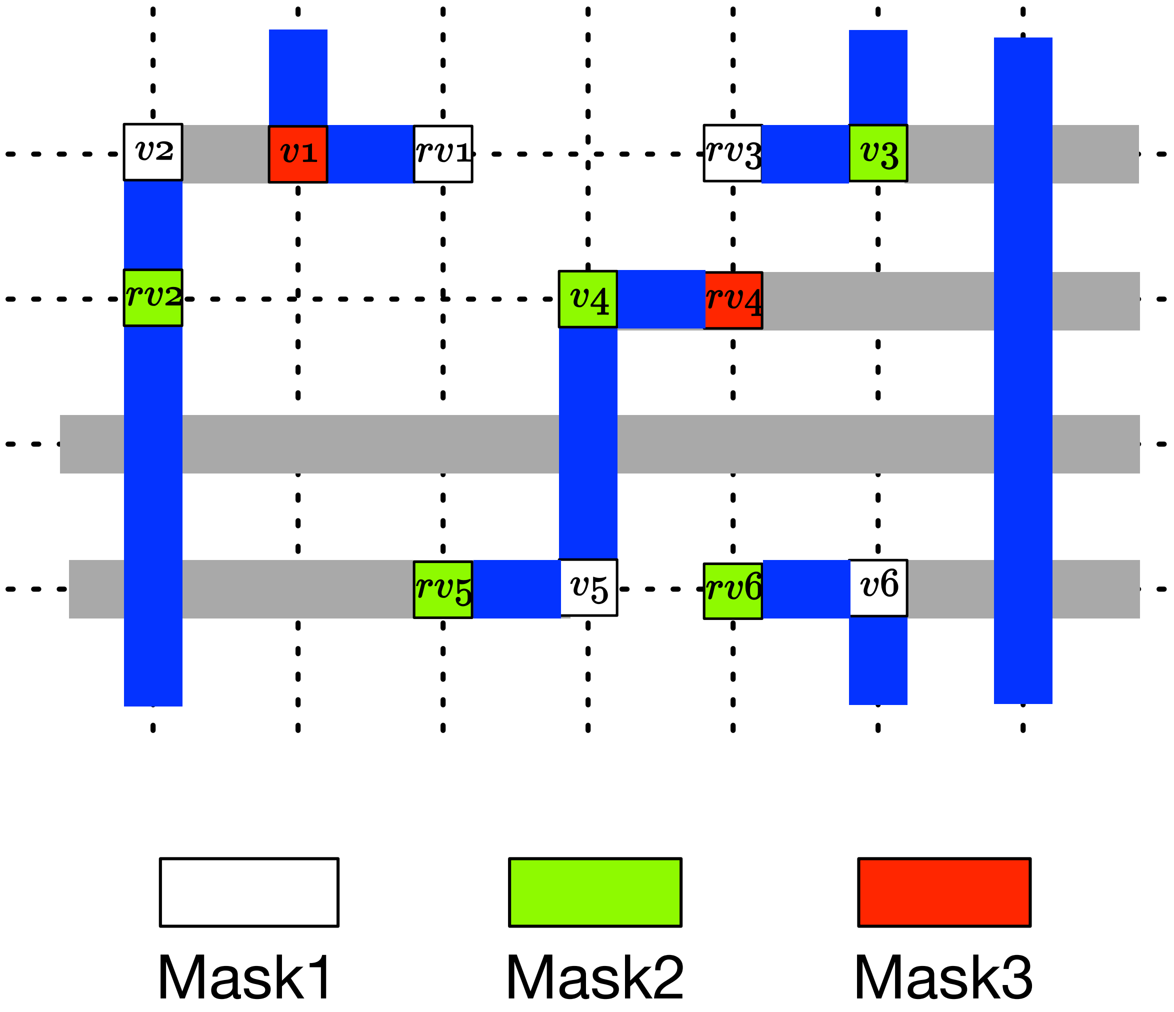


Redundant Via



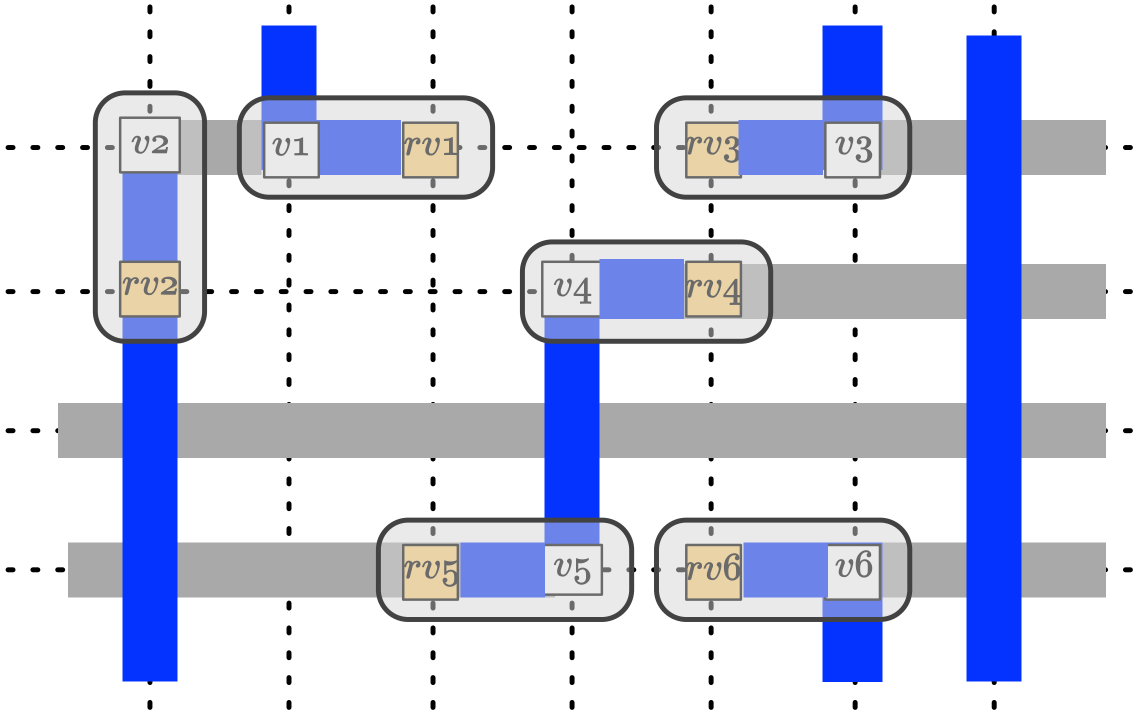
# Multiple Patterning (MP) for Via Layer

- LELE or LELELE is required for advanced technology node
- Mask cost increases

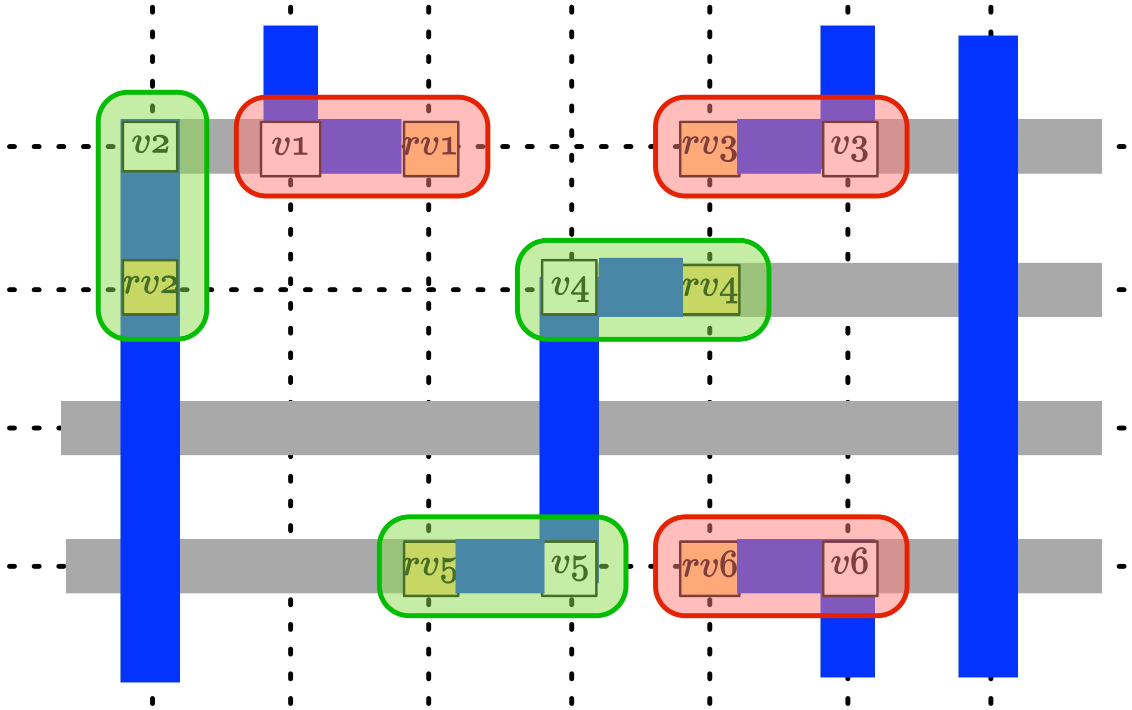


# DSA + MP for Via Layer

- Reduce the number of masks
  - DSA guiding template assignment (GTA)
  - Mask decomposition



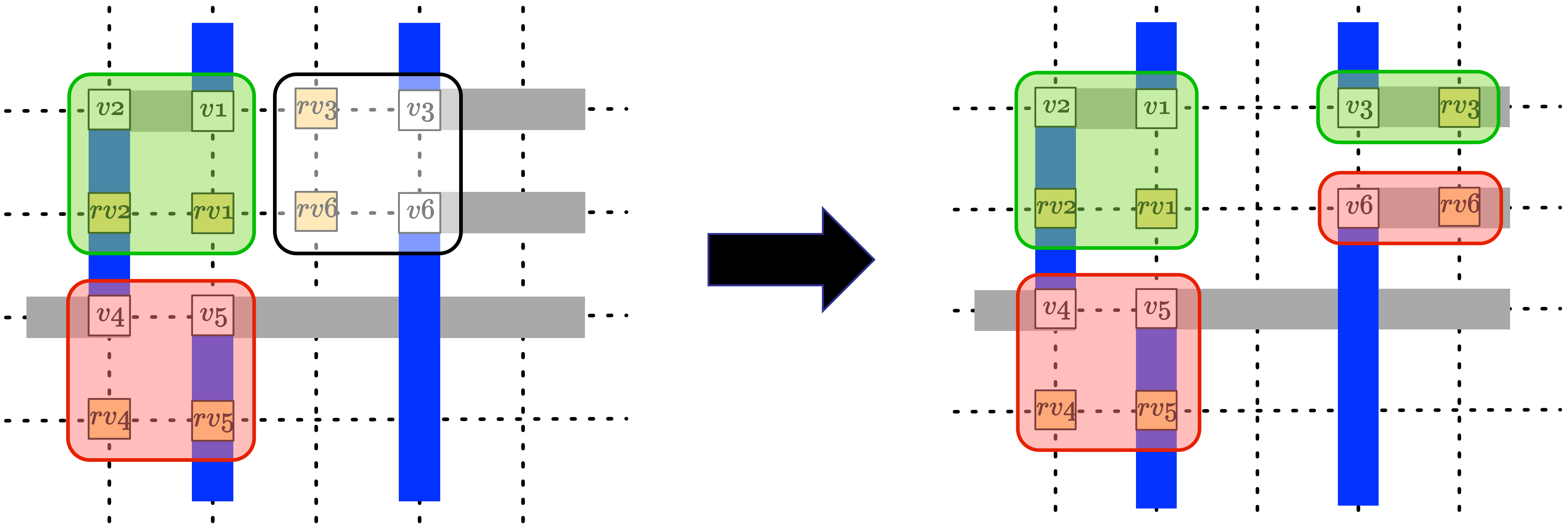
GTA



Mask decomposition

# DSA + MP Compatible RVI

- Conventional RVI does not consider DSA pattern
  - More masks may be required
- Consider “DSA + MP” in redundant via insertion stage
- **Previous work does not consider MP during RVI**



DSA + TP

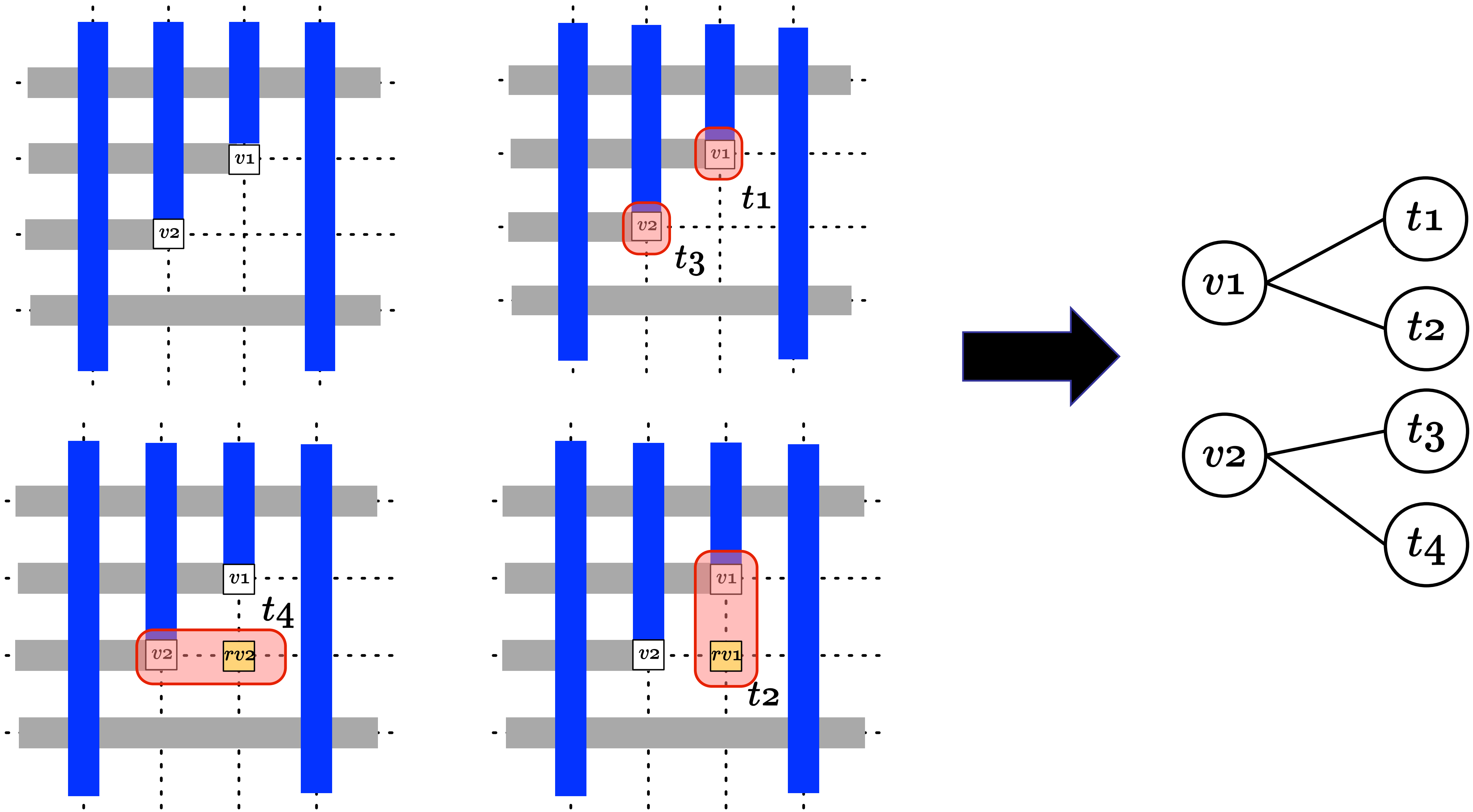
DSA + DP

# Problem Formulation

- Input
  - Post-routing layout
  - Pre-defined DSA pattern set
  - Mask number for via layer
- Objective
  - Maximize redundant via insertion rate
  - Maximize number of vias patterned by DSA

# DSA Guiding Template Assignment

- Search all possible DSA group combinations for each via
- Construct bipartite graph

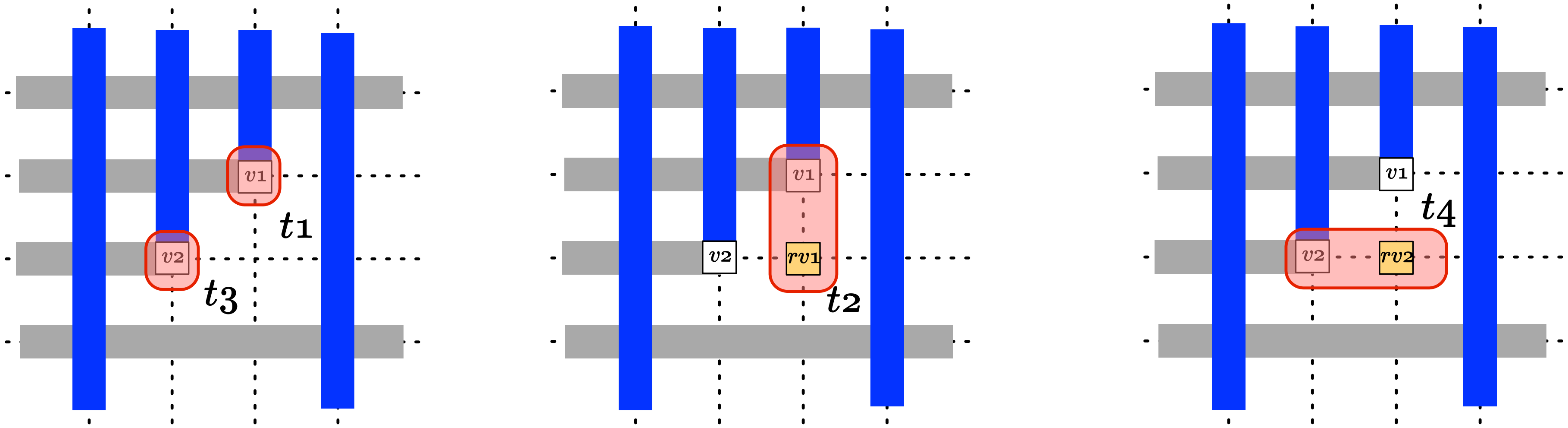


# Design Rule Constraints

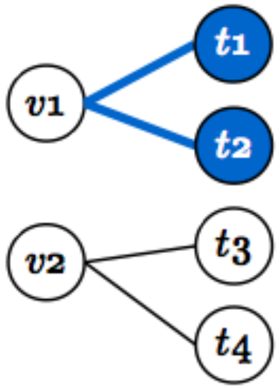
- Guiding template violation:
  - overlaps
  - minimum distance
- Edge color assignment
  - Assign same color to edges which connects any two violated guiding templates

# Design Rule Constraints

- Overlaps

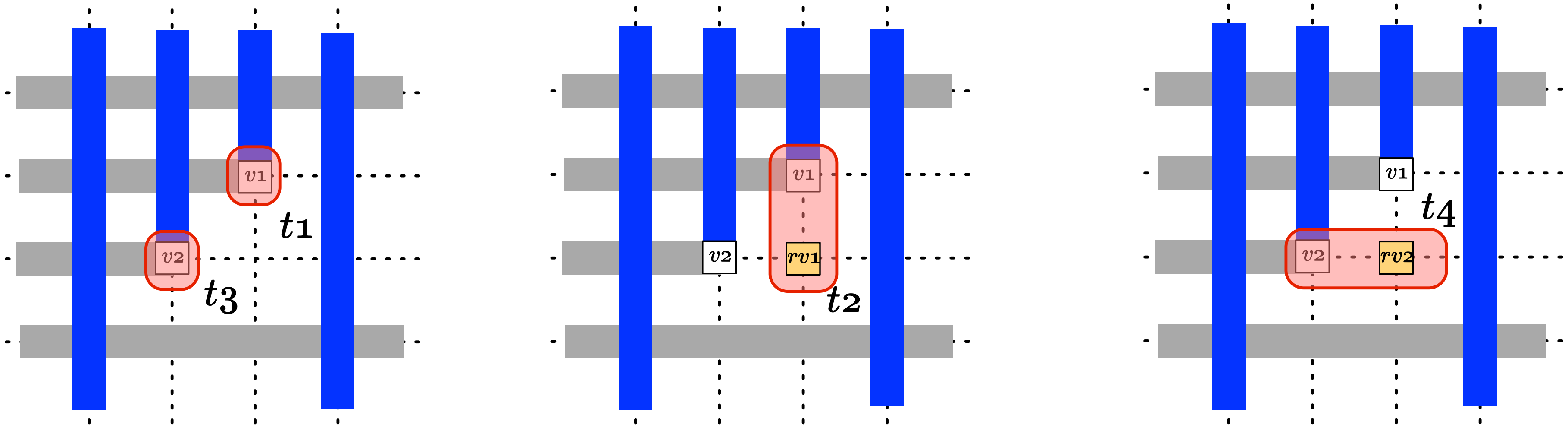


Overlap

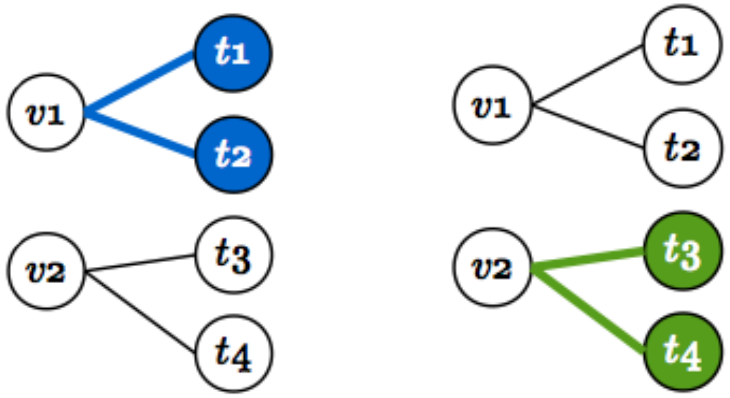


# Design Rule Constraints

- Overlaps

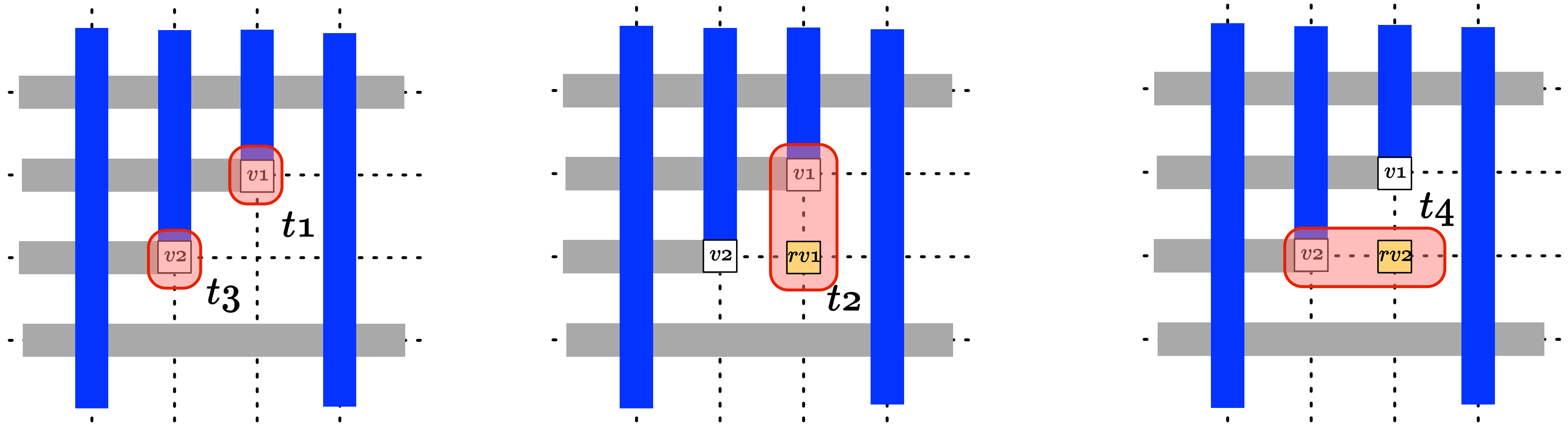


Overlap

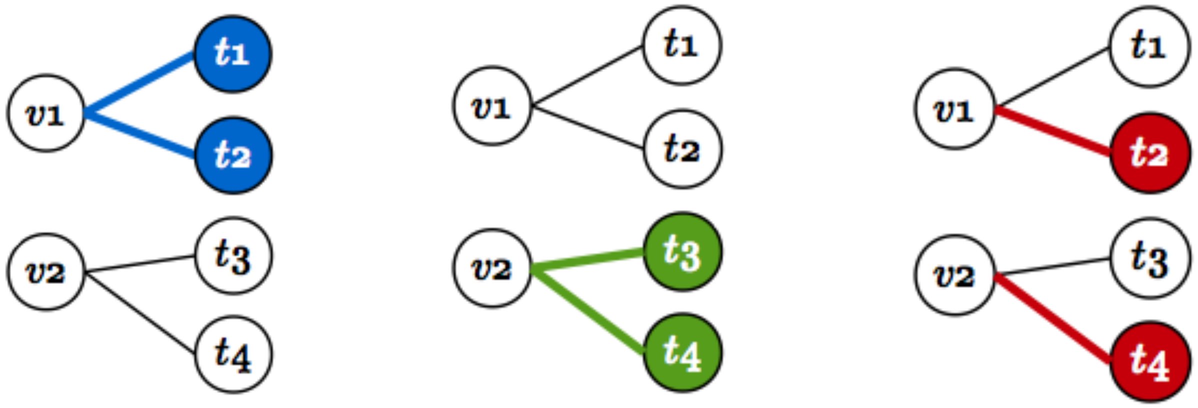


# Design Rule Constraints

- Overlaps

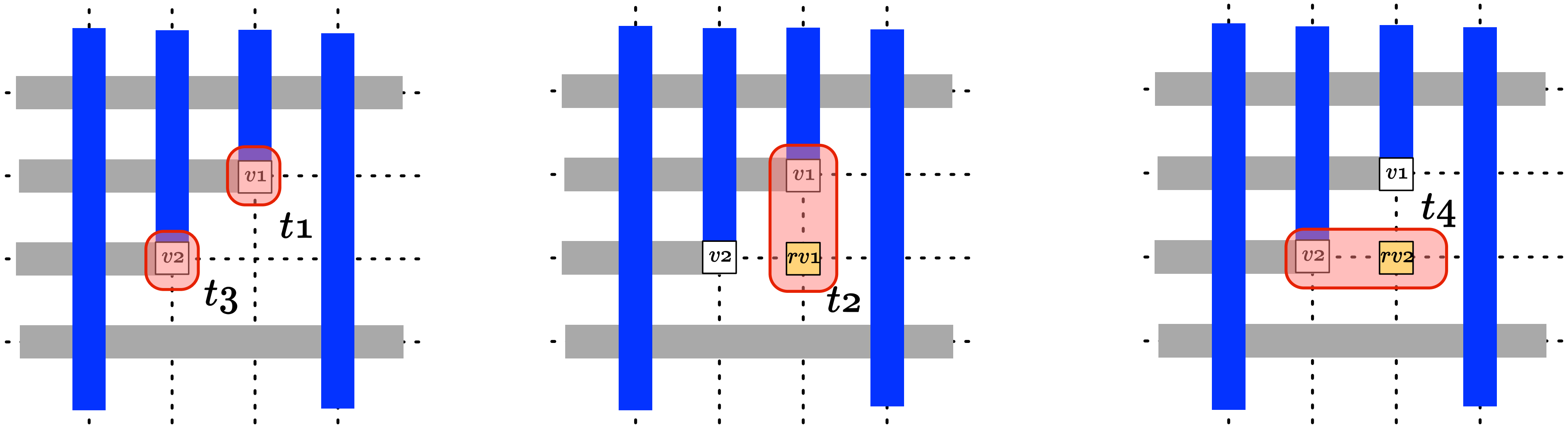


Overlap

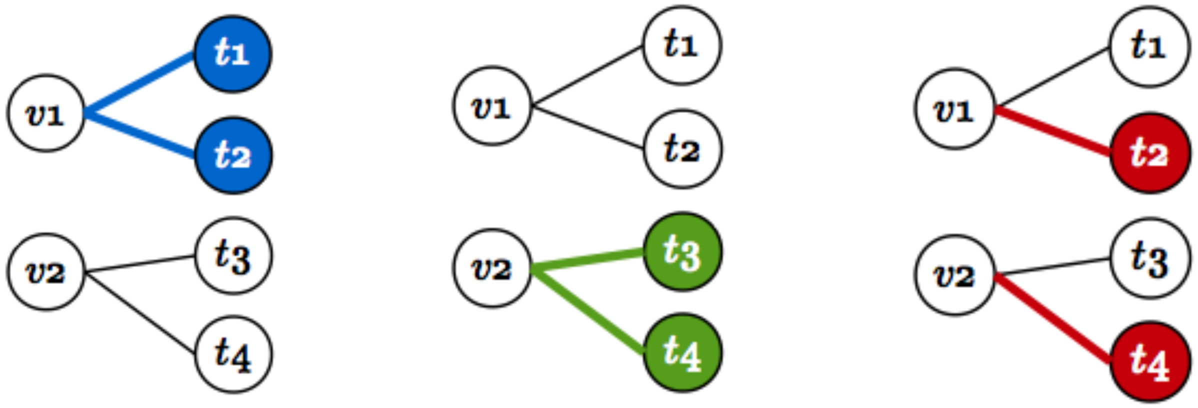


# Design Rule Constraints

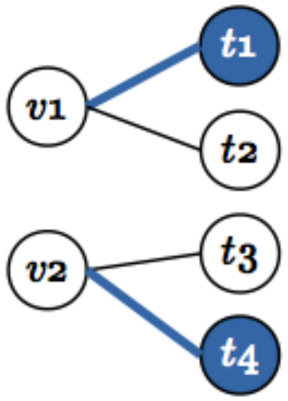
- Adjacent design rule violations



Overlap



Adjacent



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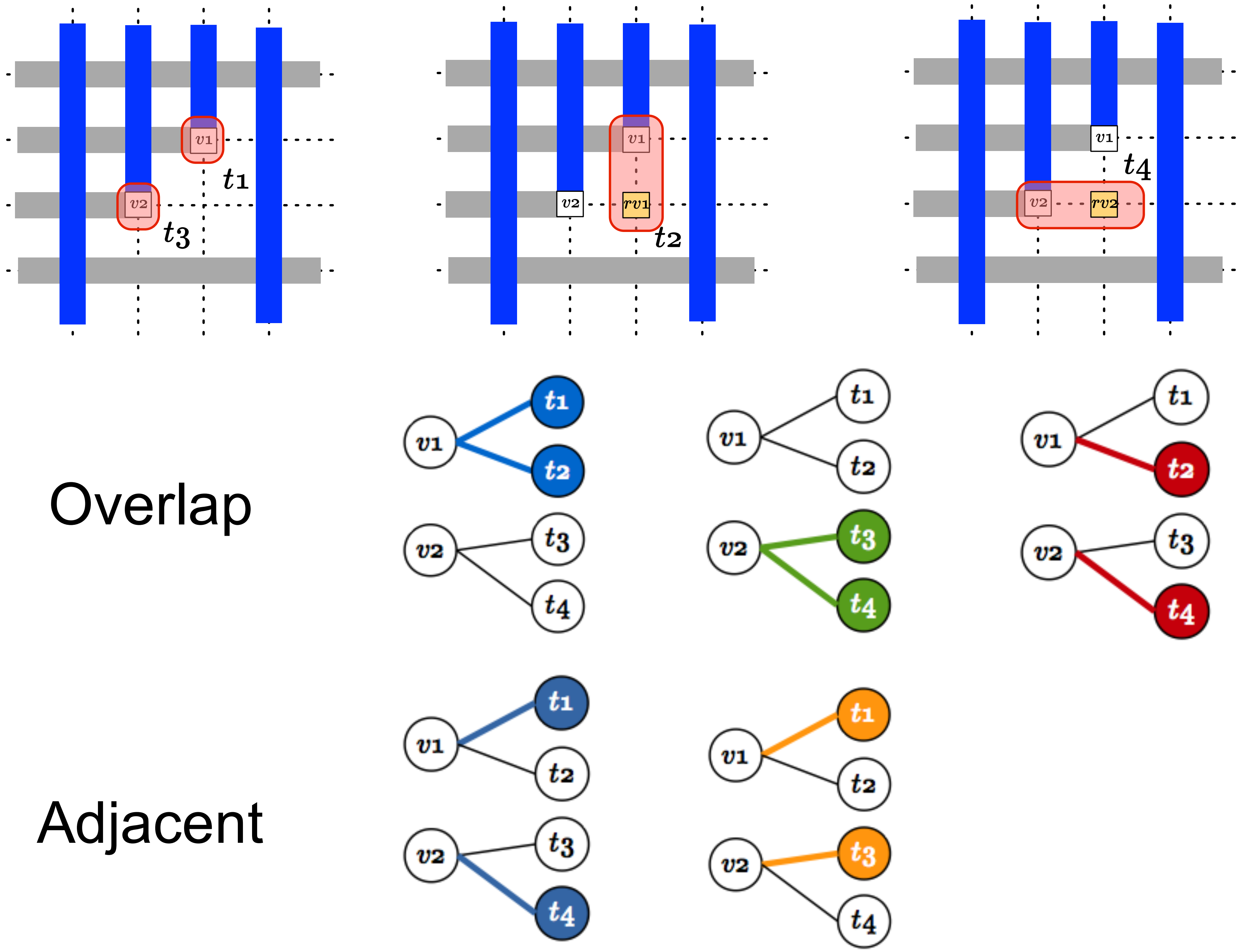
- Adjacent design rule violations

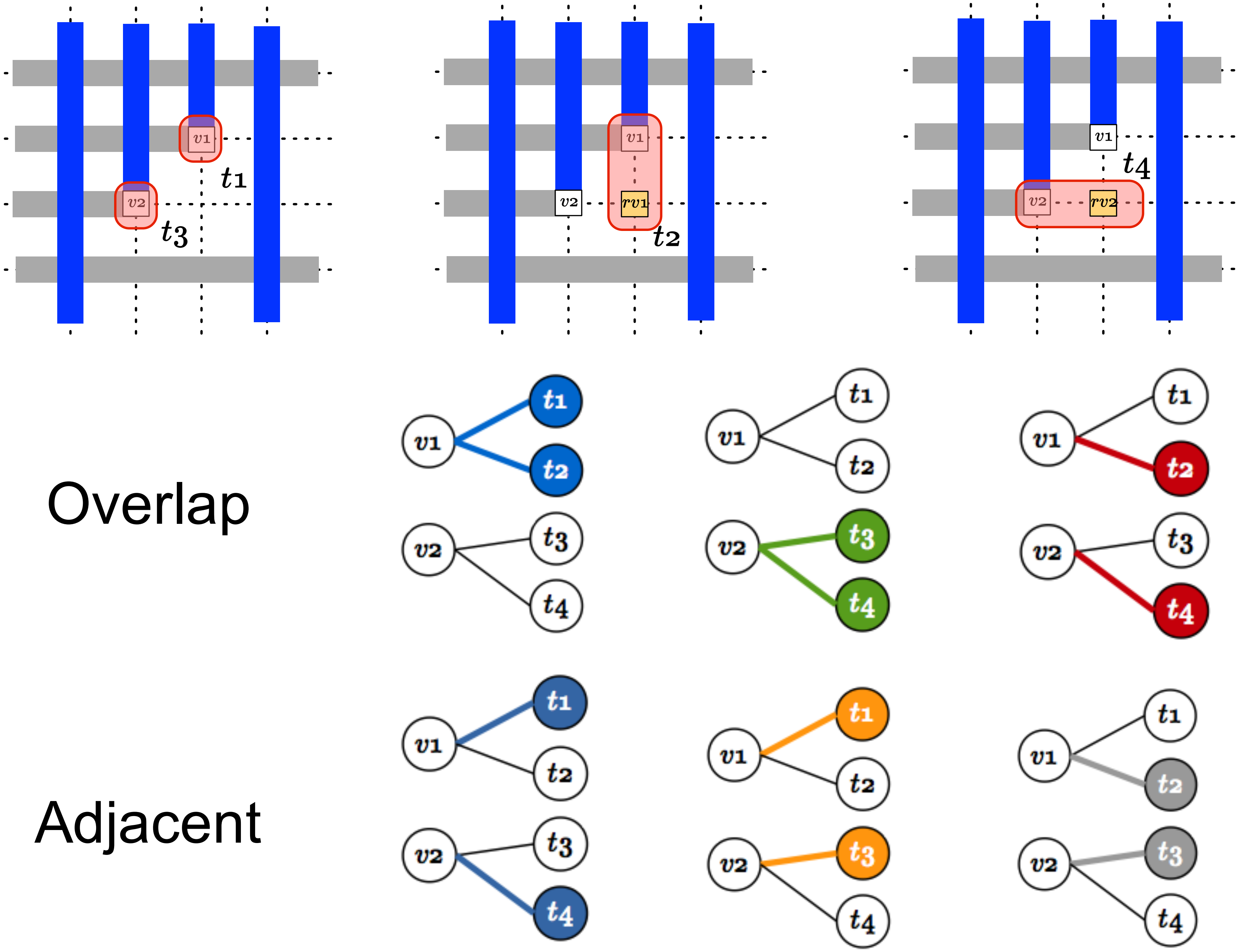


Overlap

Adjacent

# Design Rule Constraints

- Adjacent design rule violations

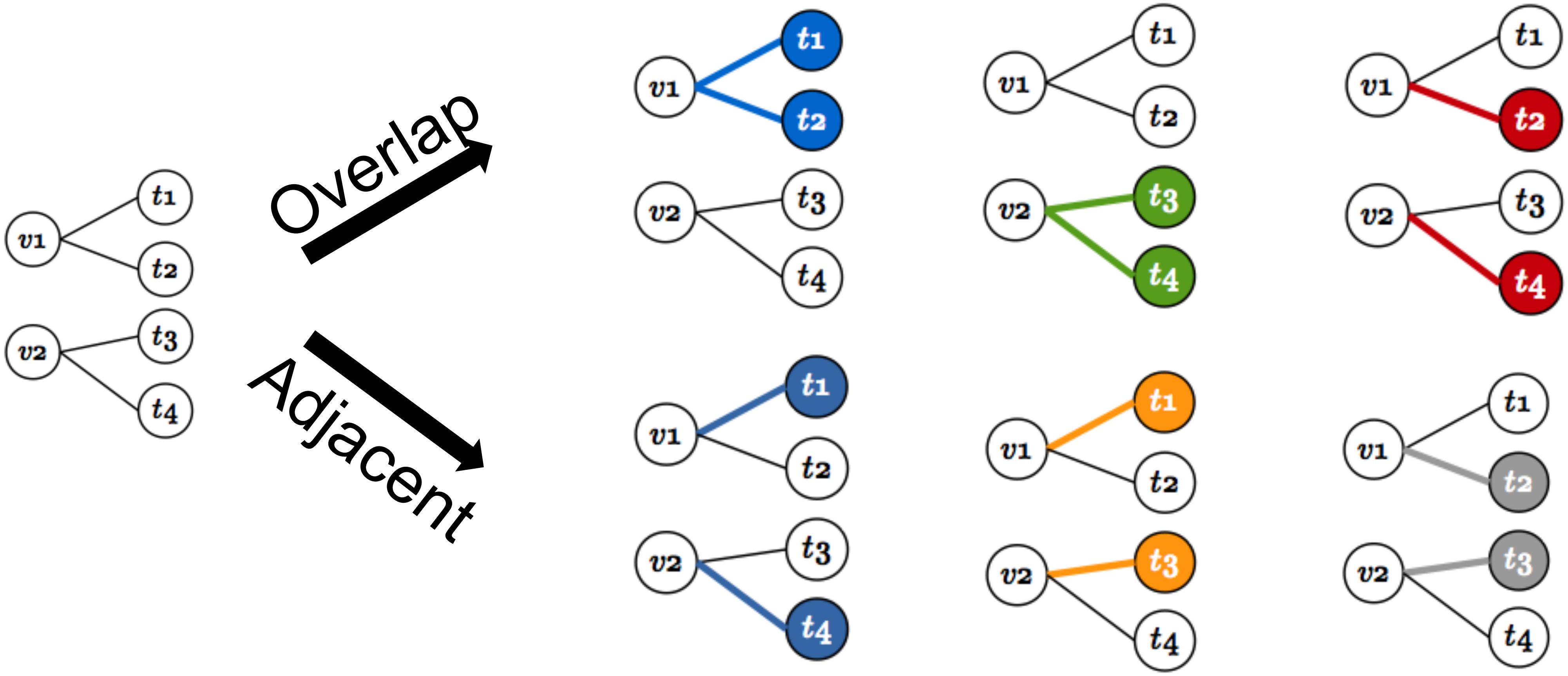


Overlap

Adjacent

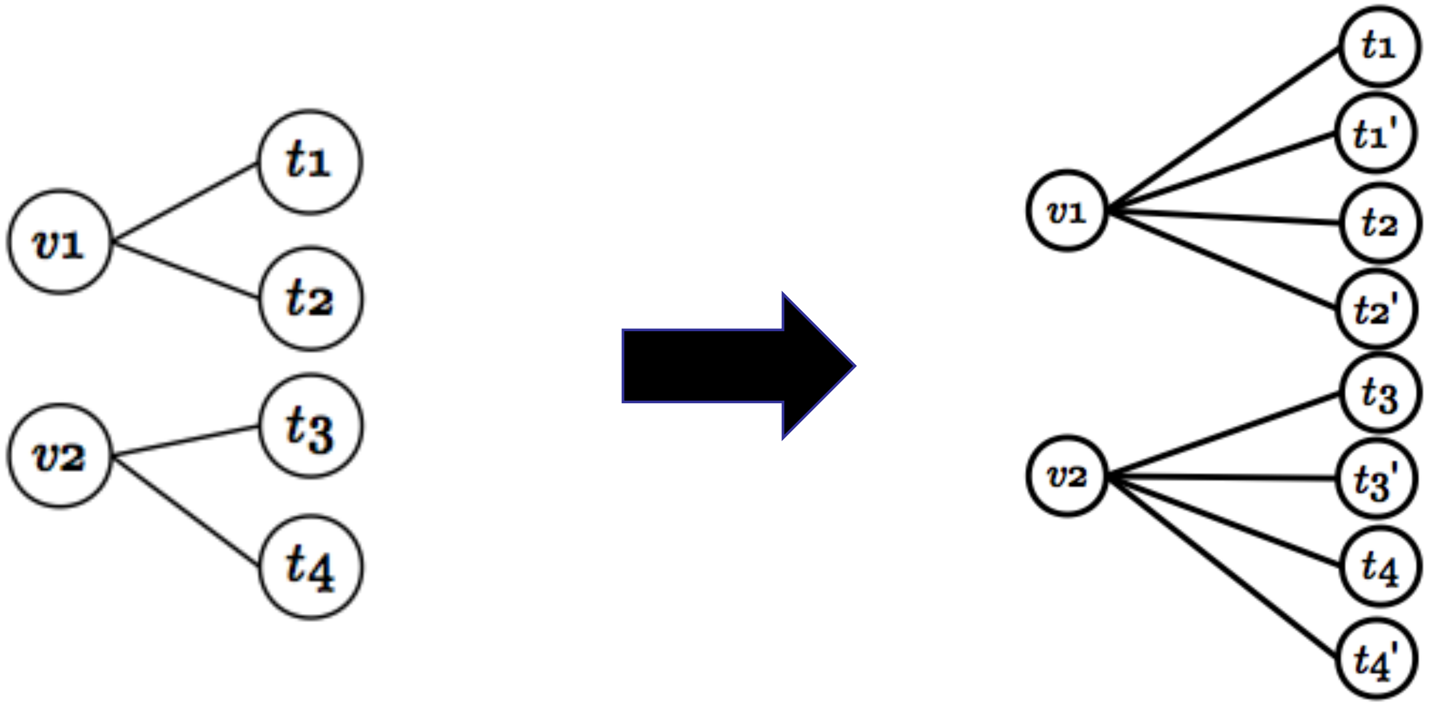
# Design Rule Constraints

- At most 1 edge can be selected for the same color group



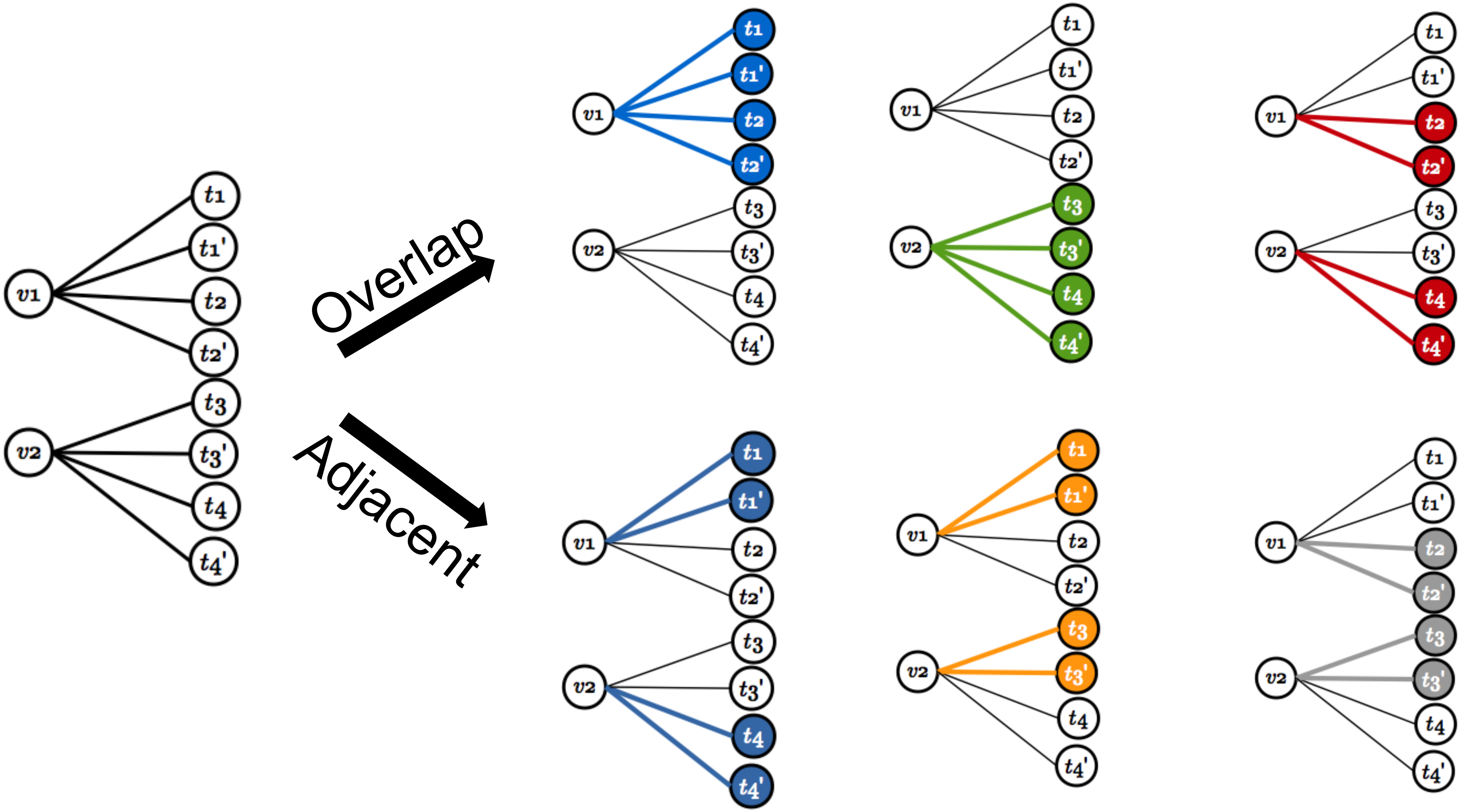
# Design Rule Constraints – Double Patterning

- Double DSA guiding patterns to indicate the masks they are assigned
  - $t$ : mask 1
  - $t$’: mask 2



# Design Rule Constraints – Double Patterning

- At most 1 edge can be selected for overlapping group
- At most 2 edges can be selected for every 2 edges in different masks for adjacent group



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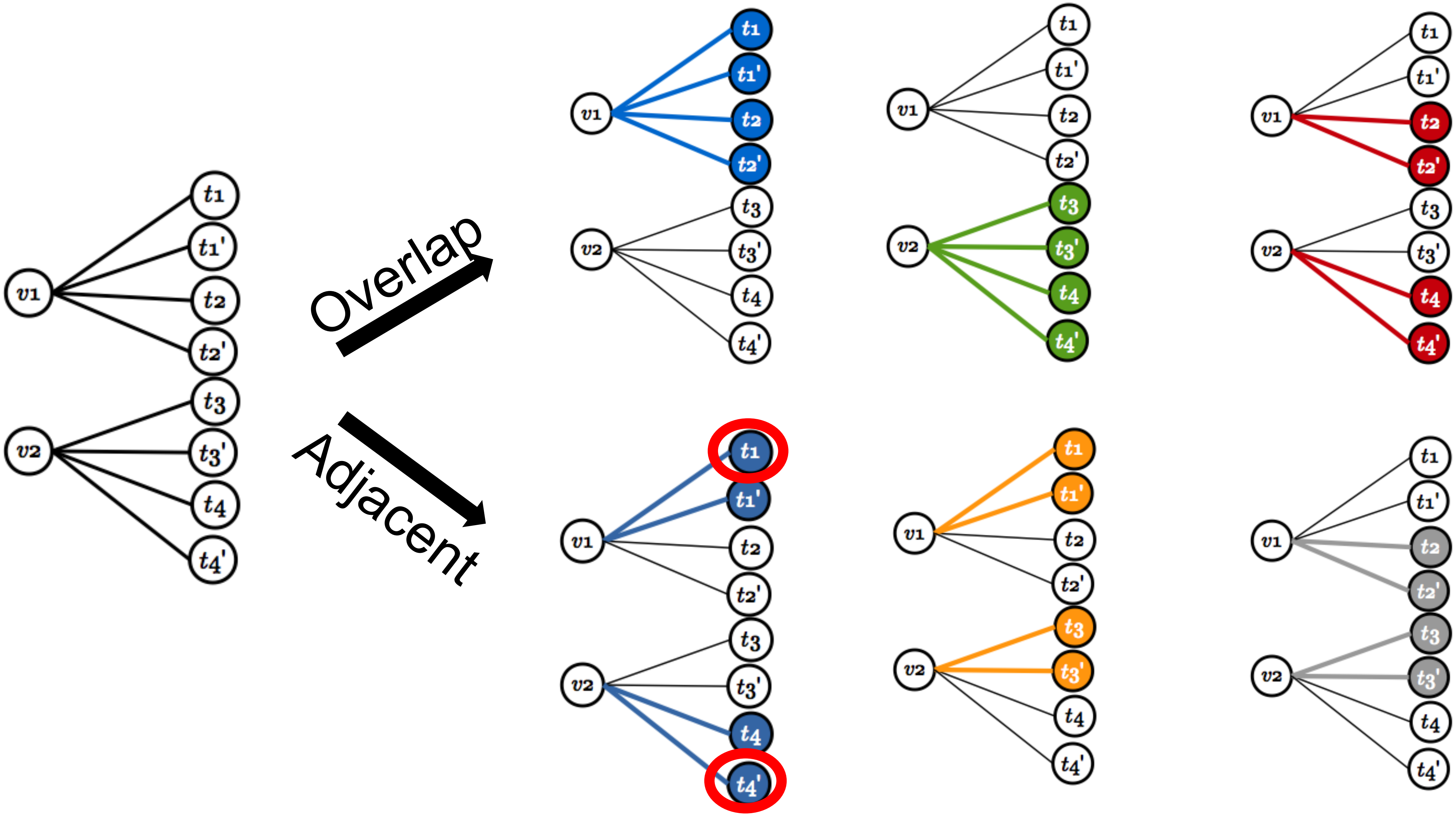

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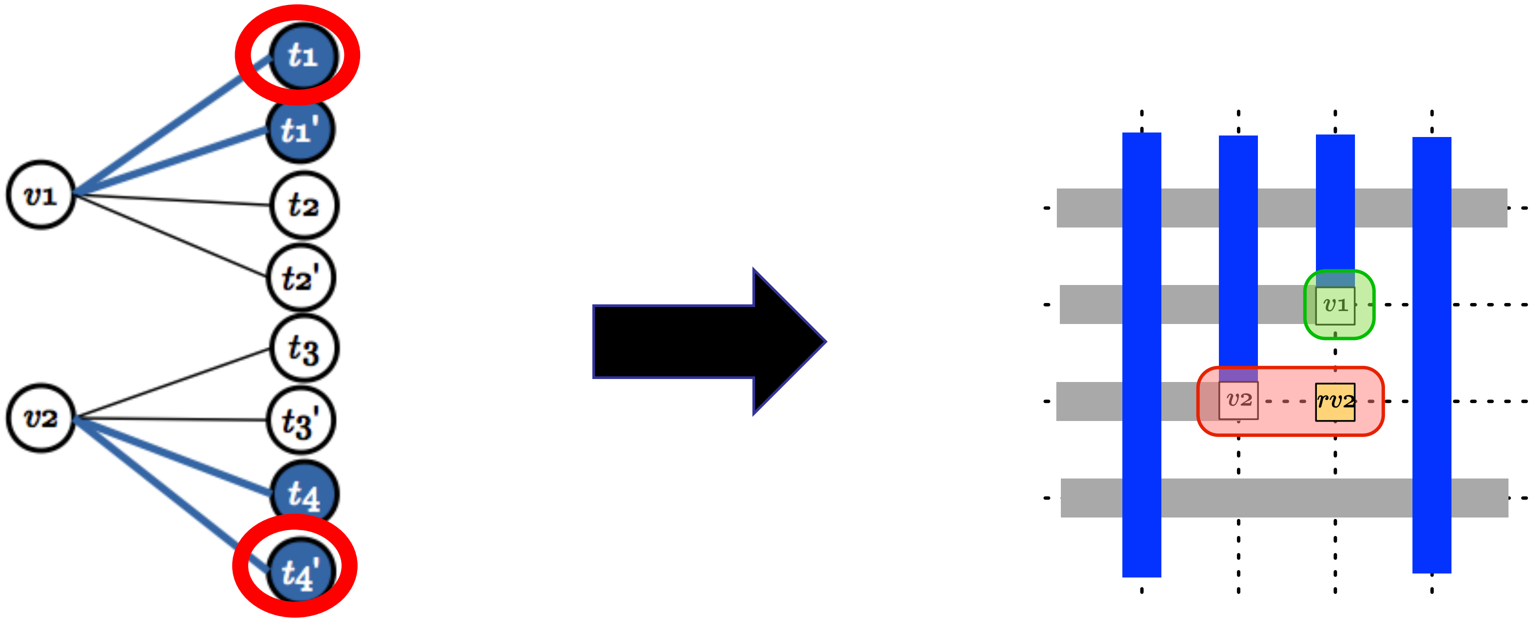
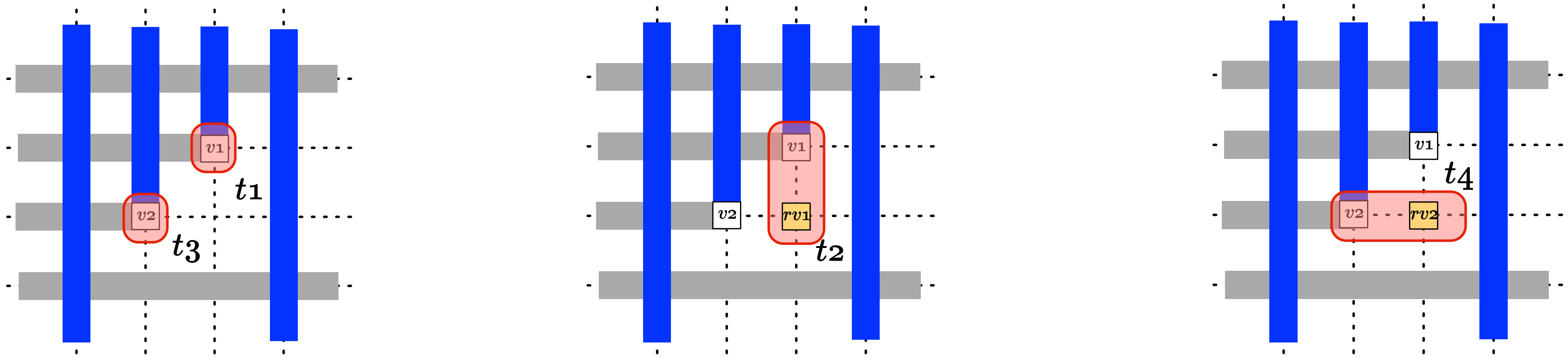
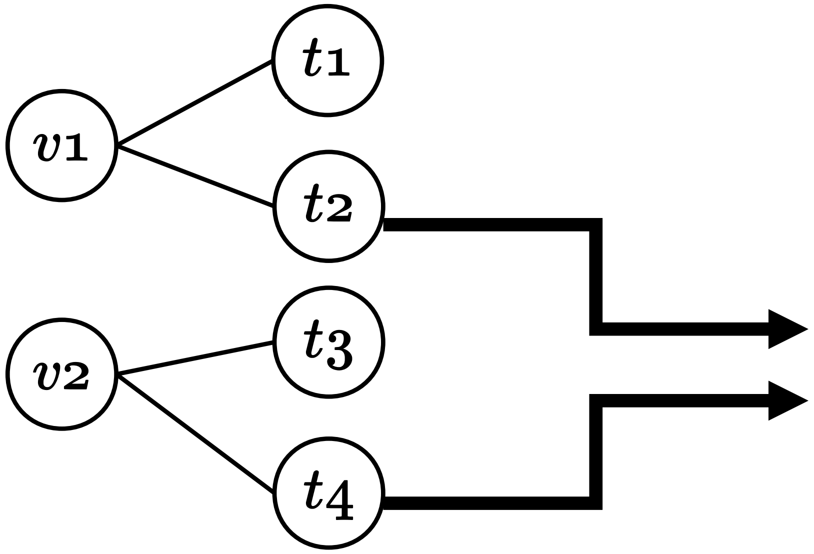


# DSA Guiding Pattern Weight

- To balance between insertion rate and number of vias patterned by DSA
- Assign higher weight to edges connecting with template with redundant via





Larger weight

# Constrained Bipartite Graph Matching

- Maximize the cost function
  - Maximize the number of edges (DSA coverage)
  - Edges with redundant via has higher priority (insertion rate)
- ILP formulation

$$\text{maximize} \quad \alpha \sum_{e_{ij} \in E_w} x_{e_{ij}} + \beta \sum_{e_{ij} \in E_{wo}} x_{e_{ij}} \qquad (2)$$

s.t.

$$x_{e_{ij}} + x_{e_{\tilde{i}\tilde{j}}} \leq 1, \qquad \forall e_{ij} \in E, \forall e_{\tilde{i}\tilde{j}} \in EO_{ij}$$

For overlaps

$$x_{e_{ij}} + x_{e_{\tilde{i}\tilde{j}}} \leq 2, \qquad \forall e_{ij} \in E, \forall e_{\tilde{i}\tilde{j}} \in EV_{ij}, \tilde{j} \neq j$$

$$x_{e_{ij}} + x_{e_{\tilde{i}\tilde{j}}} \leq 1, \qquad \forall e_{ij} \in E, \forall e_{\tilde{i}\tilde{j}} \in EV_{ij}, \tilde{j} = j$$

For adjacent

$$x_{e_{ij}} \in \{0, 1\}$$

# LP Relaxation

- Relax integer to continuous variables

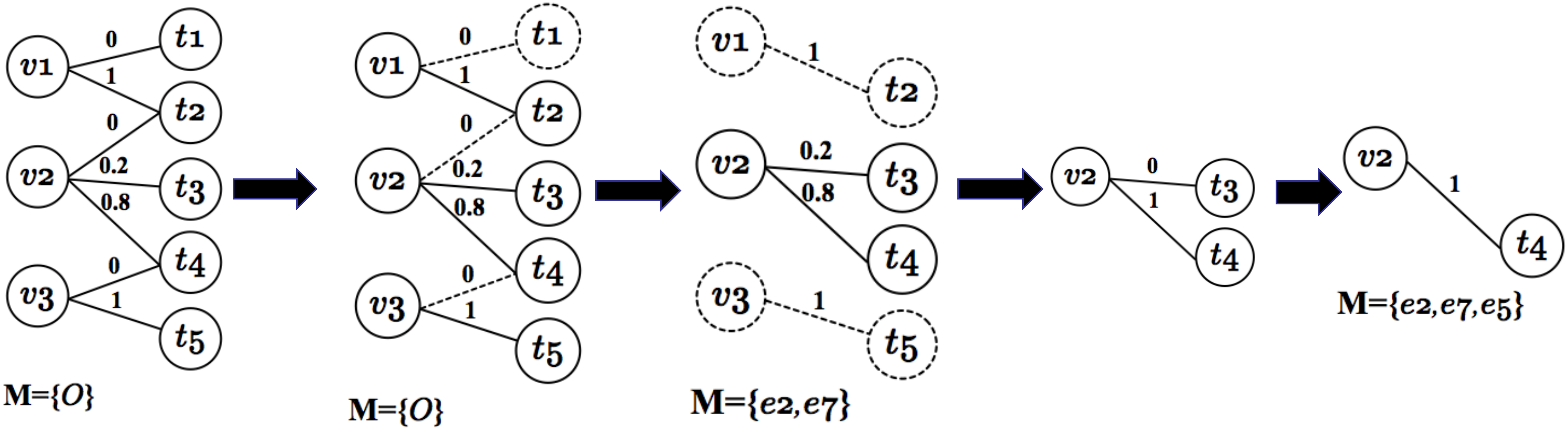
$$\text{maximize} \quad \alpha \sum_{e_{ij} \in E_w} x_{e_{ij}} + \beta \sum_{e_{ij} \in E_{wo}} x_{e_{ij}} \tag{2}$$

$$\begin{aligned} \text{s.t.} \\ & x_{e_{ij}} + x_{e_{\tilde{i}\tilde{j}}} \le 1, && \forall e_{ij} \in E, \forall e_{\tilde{i}\tilde{j}} \in EO_{ij} \\ & x_{e_{ij}} + x_{e_{\tilde{i}\tilde{j}}} \le 2, && \forall e_{ij} \in E, \forall e_{\tilde{i}\tilde{j}} \in EV_{ij}, \tilde{j} \neq j \\ & x_{e_{ij}} + x_{e_{\tilde{i}\tilde{j}}} \le 1, && \forall e_{ij} \in E, \forall e_{\tilde{i}\tilde{j}} \in EV_{ij}, \tilde{j} = j \end{aligned}$$

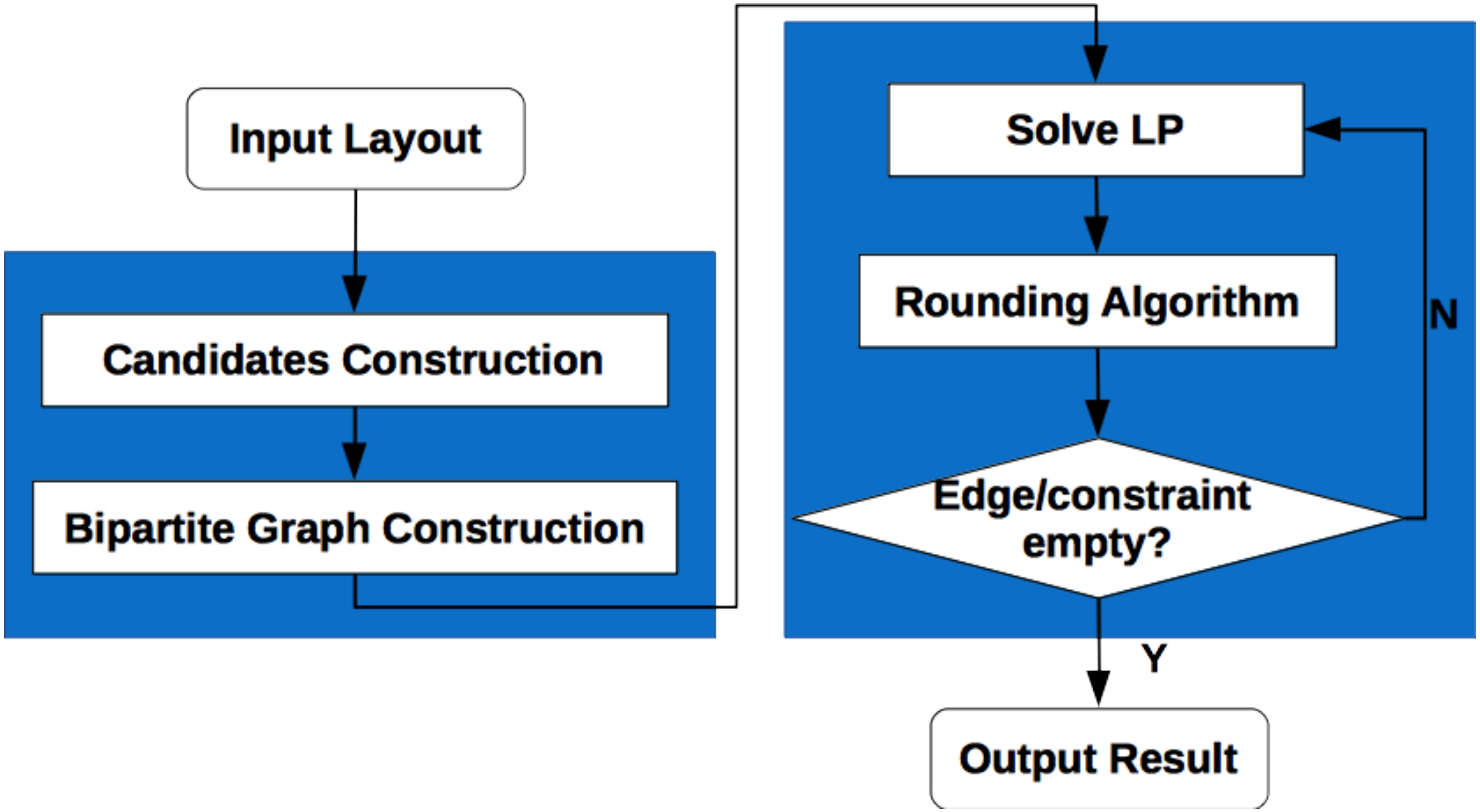
~~$x_{e_{ij}} \in \{0, 1\}$~~

# Rounding Algorithm

- LP result
- Trim LP solution: remove 0-value edges/nodes
- Update solution set: add 1-value edges
- Rounding (tight vertex):
  - 1: $x_e > 0.5$
  - 0: $x_e < 0.5$



# Speed-up Algorithm



Overall Flow

# Experimental Environment

- Implemented in C++
- 8-Core 3.4GHz Linux Server
- 32GB RAM
- ILP/LP solver: CBC

# Benchmarks and Compared Algorithms

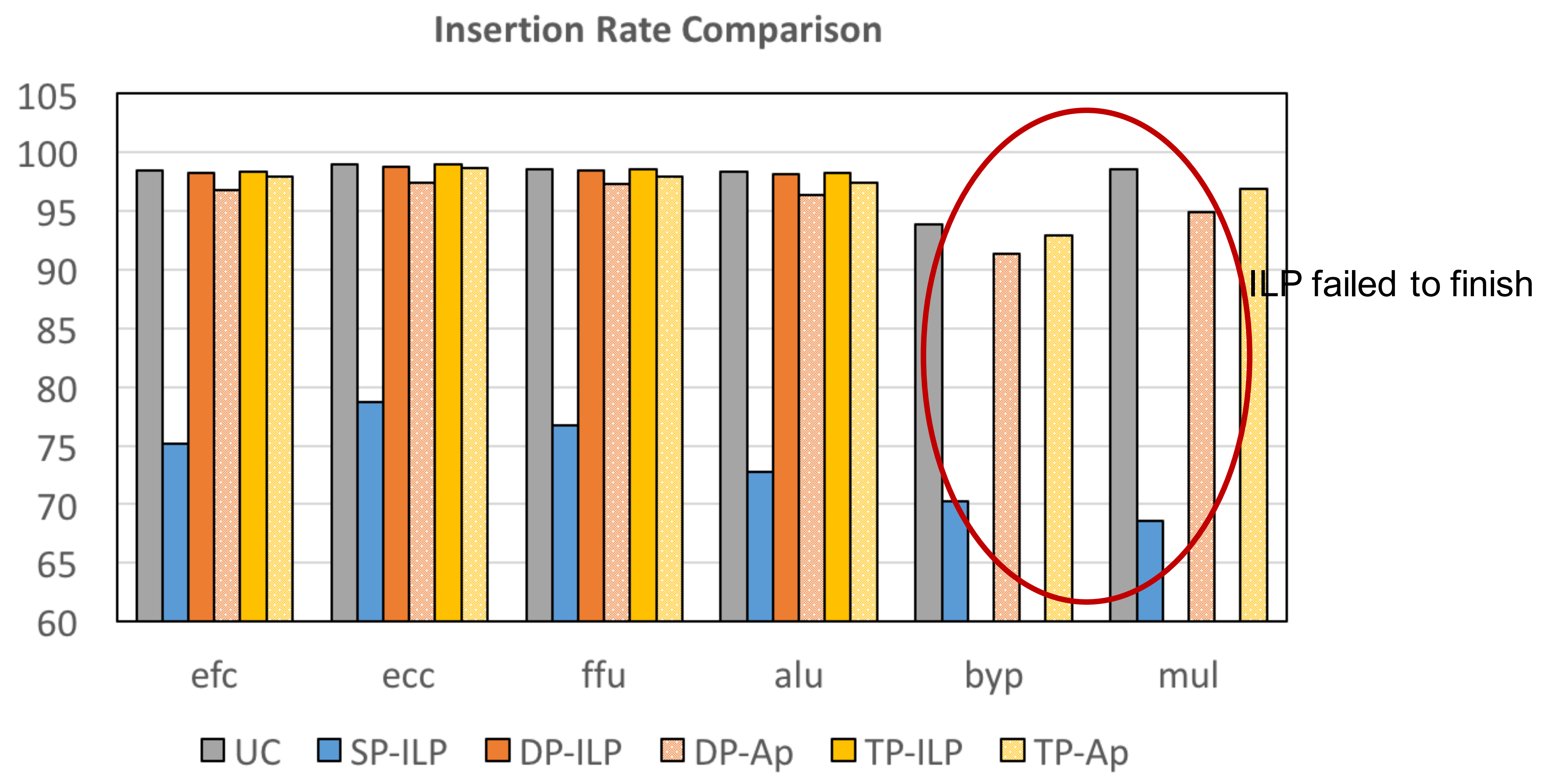
- OpenSPARC T1 design

| Bench | efc | ecc | ffu | alu | byp | mul |
|---|---|---|---|---|---|---|
| #vias | 4983 | 5523 | 7026 | 7046 | 28847 | 62989 |

- Algorithms
  - Conventional RVI: Un-Constrained (UC)
  - DSA+Single Patterning: SP-ILP
  - DSA+Double Patterning: DP-ILP, DP-Ap
  - DSA+Triple Patterning: TP-ILP, TP-Ap

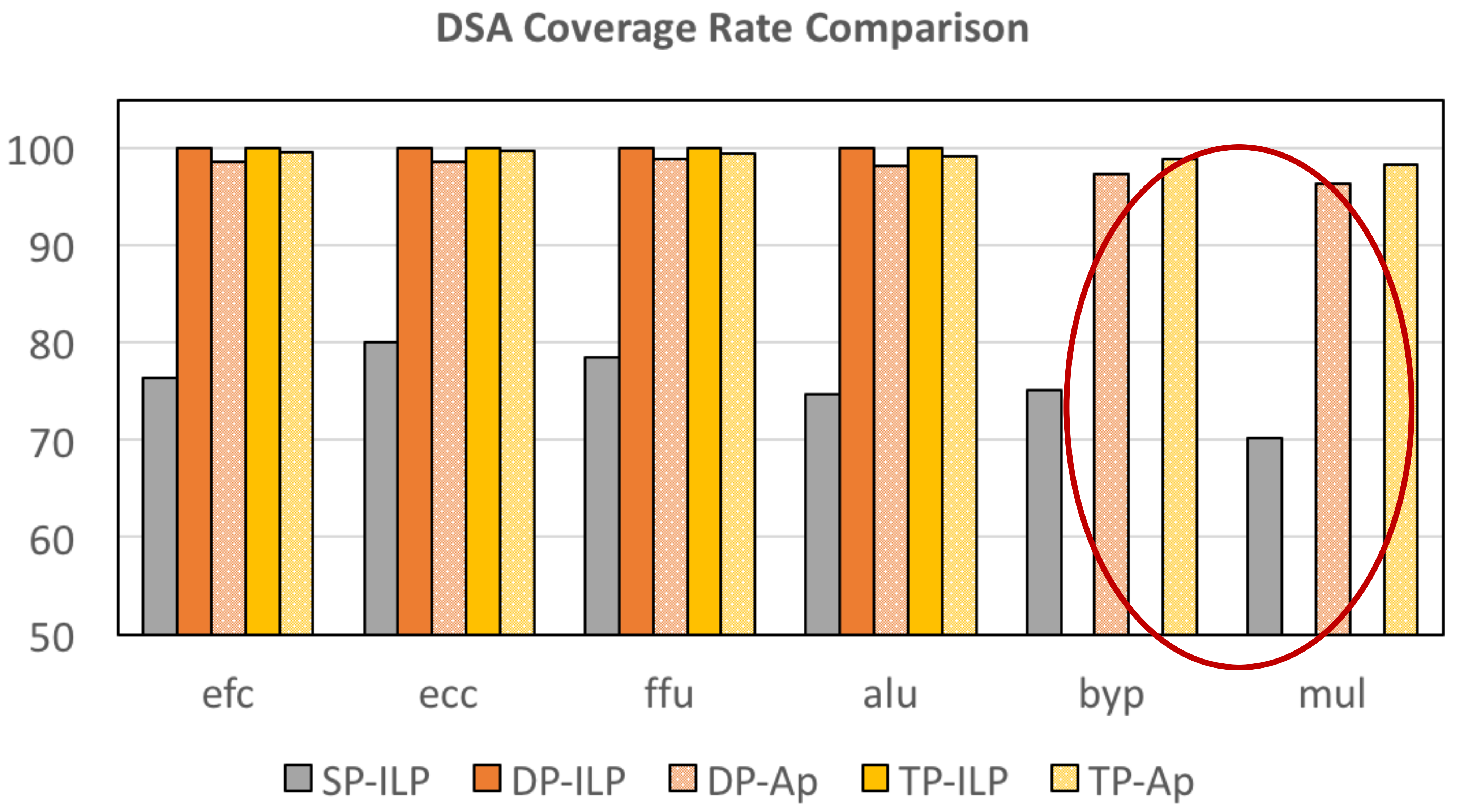
# Redundant Via Insertion Rate

- UC is thought to have highest insertion rate
- DSA+DP and DSA+TP have almost the same insertion rate with UC



# DSA Coverage Rate

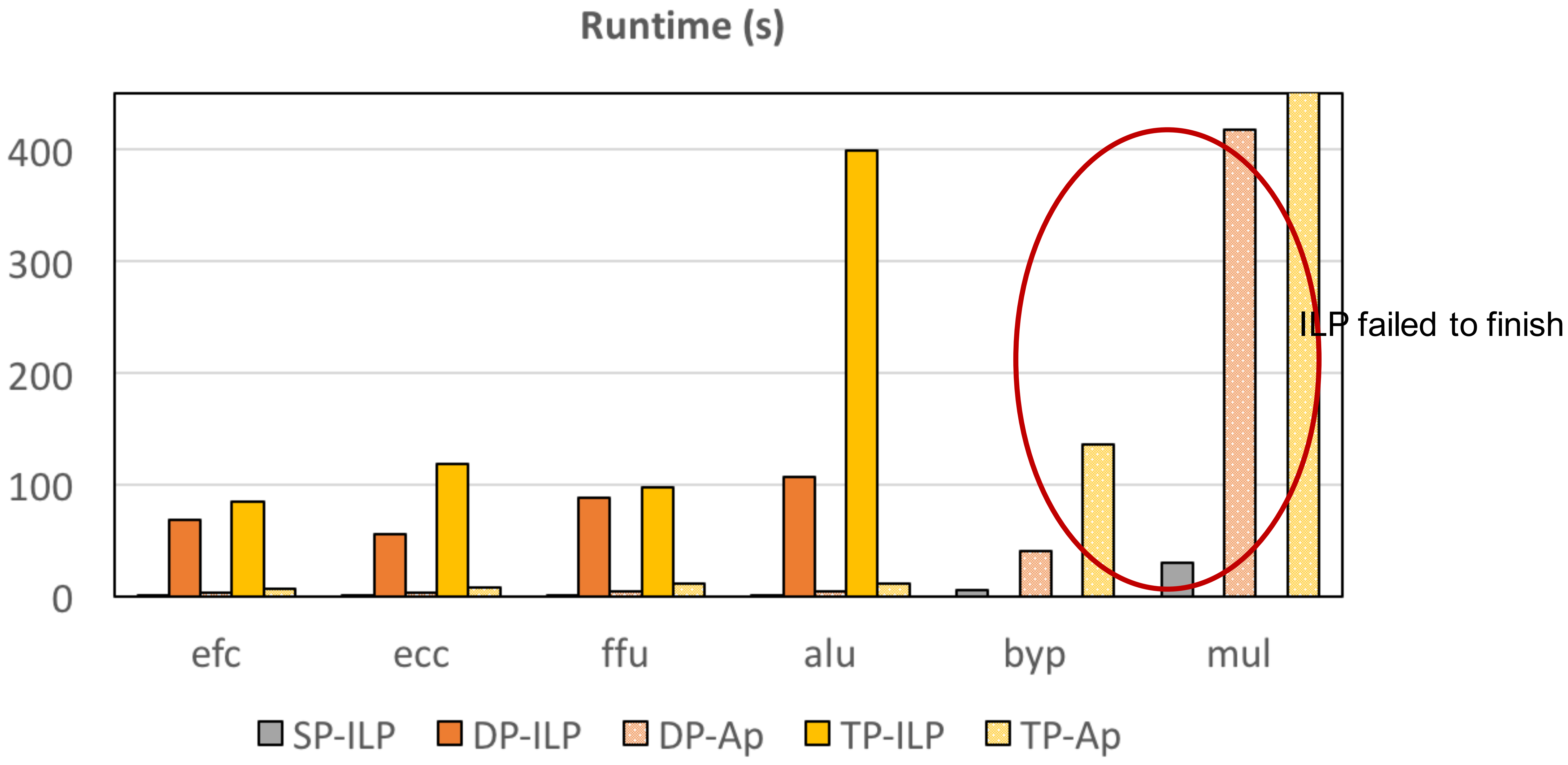
- Coverage rate: #patterned via/#total via
- DP-ILP and TP-ILP can reach 100% coverage



ILP failed to finish

# Runtime

- Approximation algorithm is 20x faster than ILP



# Conclusion

- Directed Self-Assembly is a promising candidate for next generation lithography
- We proposed a general ILP formulation and a speed-up algorithm to solve the DSA aware redundant via insertion with MP simultaneously
- The experimental results demonstrate the effectiveness of our algorithm
- Future work:
  - DSA+RVI during routing
  - New ways of hybrid?

# Thank you!

Q&A