香港中文大學
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Machine Learning in Nanometer AMS Design-for-Reliability

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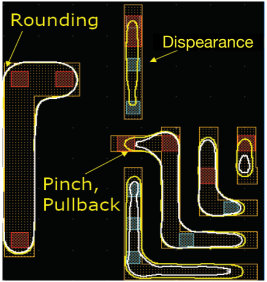
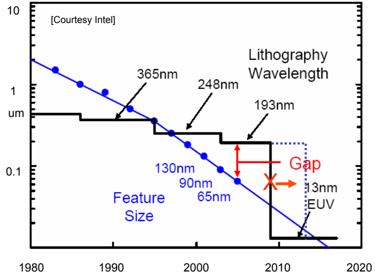
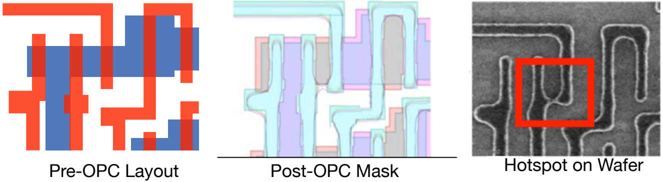
Spatial reliability issues

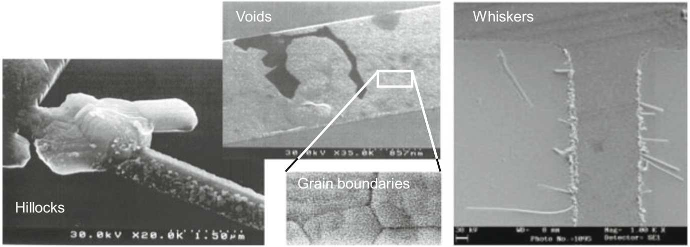




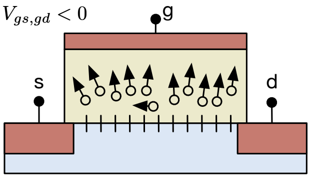


Lithography hotspots (GENG+,ICCAD'20)

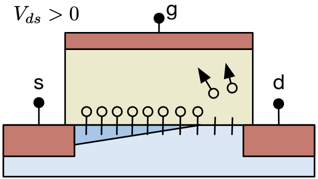
Temporal reliability issues



EM (Photo courtesy of G. H. Bernstein und R. Frankovic, University of Notre Dame)

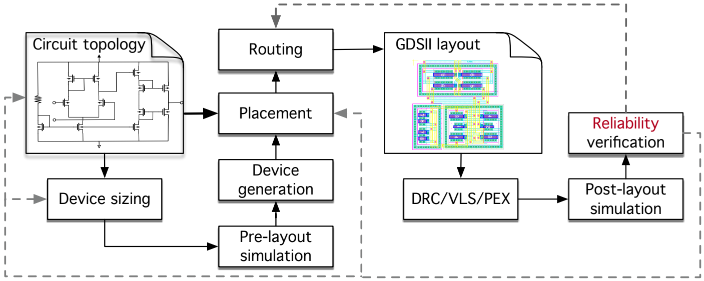


BTI (CHEN+,ASPDAC'21)



HCI (CHEN+,ASPDAC'21)

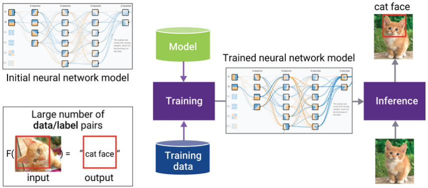
AMS circuits design flow



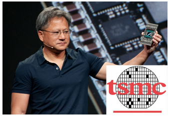
ML As a Solution: Why ML?

- Big Data
  - Large unstructured data sets flood us everyday
  - Facebook, LinkedIn, Amazon, Google

- Deep Neural Networks
  - Approaching human intelligence

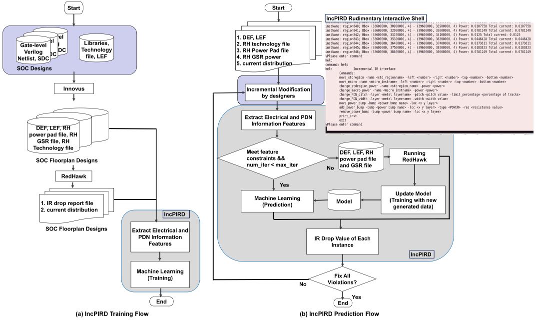


- Hardware advances
  - GPU, FPGA, TPU, ...



ML-based Verification

Shallow model: IR-drop prediction



IncPIRD flow (HO+,ICCAD'19)

ML model

- Input features: chip/Block size, pitch of metal layer, pulldown and pullup component in node itself and its neighbors;
- Model: XGBoost;
- Output: IR drop value of each instance.

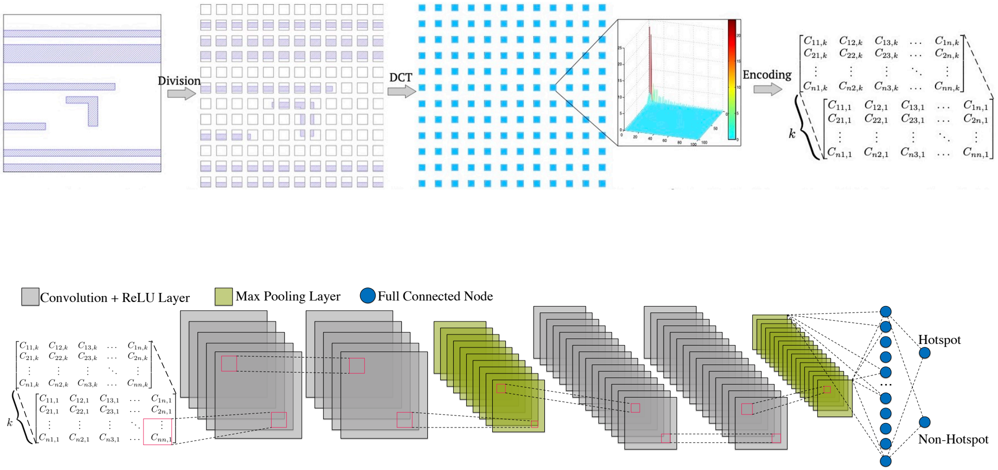
Shallow model

Drawbacks

- Needs complicated feature engines;
- Needs more domain knowledge;
- Features cannot be extracted by task orientation.

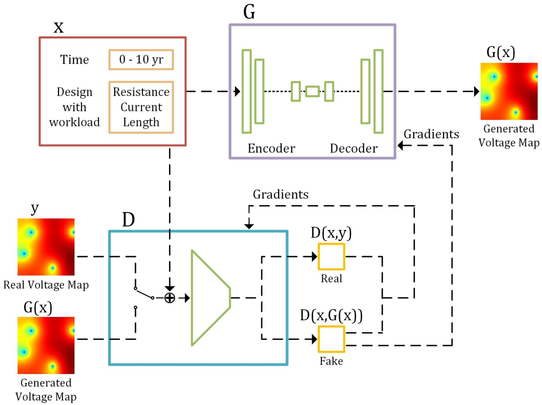
Solution

- Build a model with a certain “depth”;
- Use a learning algorithm to automatically learn a good feature representation.

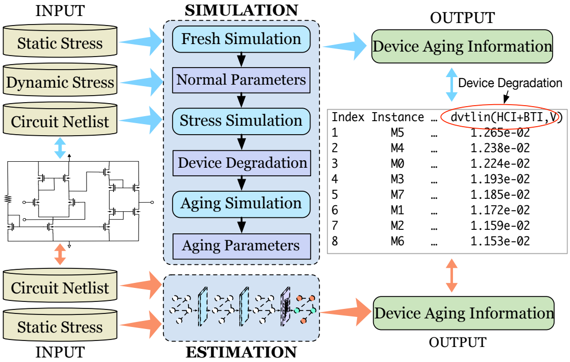


CNN-based HSD flow (YANG+,DAC'17).

Generative model

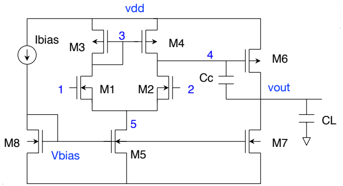


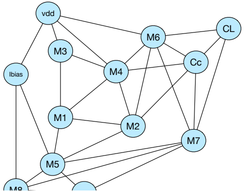
GAN-based EM-induced voltage prediction flow (ZHOU+,ICCAD'20).

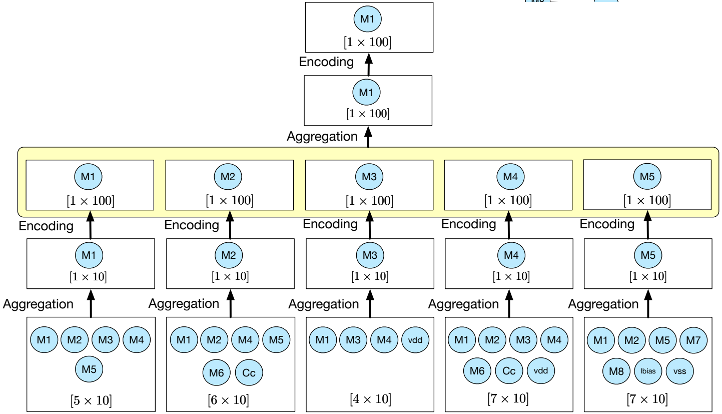


GCN-based aging degradation flow (CHEN+,TCAD'21)

Node embedding





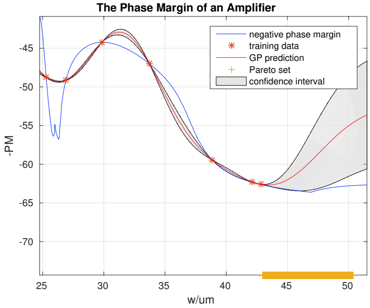


ML-based CAD Flow For DFR

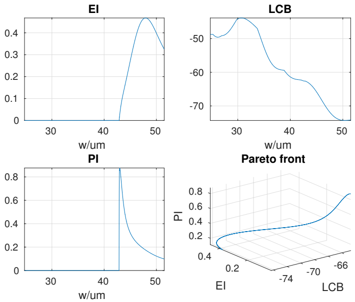
Sizing: Bayesian optimization

Objective

$$\text{minimize} \quad \mathrm{LCB}(\boldsymbol{x}), -\mathrm{EI}(\boldsymbol{x}), \quad -\mathrm{PI}(\boldsymbol{x})$$

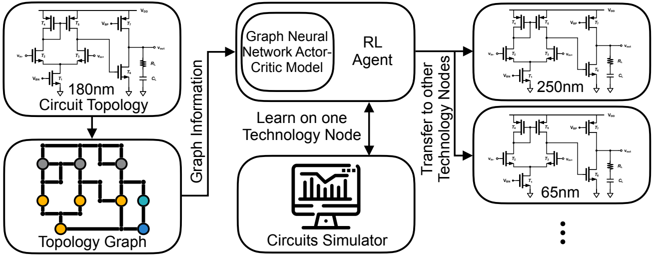


(a) True phase margin curve, GP predictions, and Pareto set

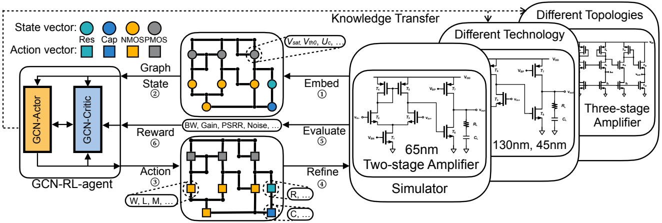


(b) The LCB, EI, and PI functions and the Pareto front

The multi-objective optimization (LYU+,ICML'18)



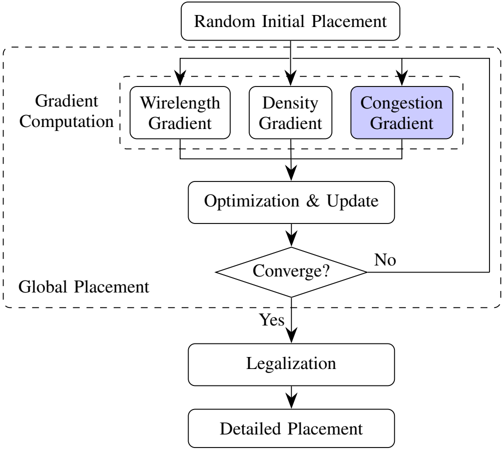
GNN-based Reinforcement Learning for Transistor Sizing



Overview (WANG+,DAC'20).

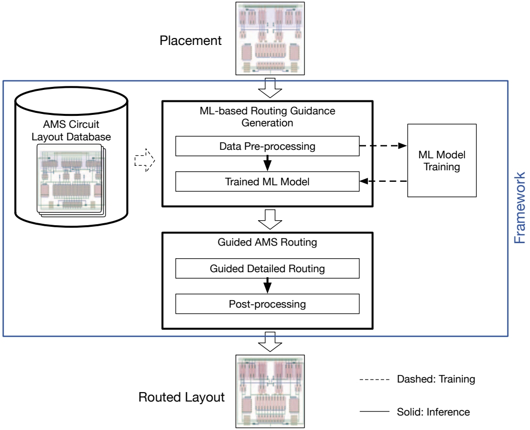
DREAMPlace Strategies (LIN+,DAC'19)

- Cast the non-linear placement problem into a neural network training problem.
- Leverage deep learning hardware (GPU) and software toolkit (e.g. `Pytorch`)
- Enable ultra-high parallelism and acceleration while getting the state-of-the-art results.



Routability Estimation × DREAMPlace (LIU+,DATE'21)

Routing (Mimic the manual layout approach)



Overall flow (ZHU+,ICCAD'19)

Open challenges and potential directions

Verify dynamic reliability for large-scale design

Dilemma

- Inputing the entire design causes out-of-memory on GPU;
- Inputing a subcircuit netlist or layout tile cannot consider corresponding stress conditions.

Potential solutions

- Estimate the worst degradation;
- Incrementally, heuristically and hierarchically simulate subcircuits to obtain dynamic stress conditions.

Integrate reliability model into sizing stage

Dilemma

- GP has limited fitting ability for the very complicated model;
- CNNs and GCNs cannot be directly integrated into the Bayesian optimization framework.

Potential solutions

- Neural processes and graph neural processes, which have the better fitting ability and provide estimation uncertainty.

Integrate reliability models into the routing

Challenge

- It is difficult to model the performance and reliability, such as EMI noise, via routing layout and integrate ML-based models into routing cost function;
- in each search step, ML-based model inference has to be performed, which brings expensive computation.

Potential solutions

- The gradient values of the ML-based reliability model can be used as cost values in the routing stage;
- The gradient values are updated by the back-propagation for several routing nets to achieve a better trade-off between runtime and layout routing reliability quality.

Conclusion

Conclusion

- It is promising to apply ML techniques to achieve AMS circuits DFR with high efficiency.
- Some open challenges and promising solutions about ML are discussed in nanometer AMS circuits DFR.
- More studies promote the development of AMS circuits DFR.

THANK YOU!