

BEI YU

Associate Professor ◊ Department of Computer Science & Engineering
Rm 907, Ho Sin Hang Engineering Building ◊ The Chinese University of Hong Kong
byu@cse.cuhk.edu.hk ◊ (852)-3943-8435

RESEARCH INTERESTS

Machine learning & combinatorial algorithms in VLSI computer aided design (CAD) and computer vision (CV).

EXPERIENCE

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| Associate Professor, CSE Department | Aug. 2021 – present |
| Assistant Professor, CSE Department | Aug. 2015 – Aug. 2021 |
| The Chinese University of Hong Kong, Hong Kong SAR | |
| Postdoctoral Researcher, ECE Department | Aug. 2014 – July 2015 |
| University of Texas at Austin, TX, USA | |

EDUCATION

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| University of Texas at Austin, TX, USA | Aug. 2010 – Aug. 2014 |
| Ph.D., Department of Electrical and Computer Engineering | |
| Tsinghua University, Beijing, P.R. China | Sep. 2007 – Jul. 2010 |
| M.S., Department of Computer Science and Technology | |
| UESTC, Chengdu, P.R. China | Sep. 2003 – Jul. 2007 |
| B.S., Information and Compute Science | |

SELECTED AWARDS AND HONORS

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| Best Paper Award | DATE | 2022 |
| Best Paper Award | ICCAD | 2021 |
| Best Paper Award | ASPDAC | 2021 |
| Best Paper Award | Integration, VLSI Journal | 2018 |
| Best Paper Award | ISPD | 2017 |
| Best Paper Award | ICCAD | 2013 |
| Best Paper Award | ASPDAC | 2012 |
| Best Student Paper Award | ICTAI | 2019 |
| Best Student Paper Award | SPIE | 2016 |
| Best Paper Award Nomination | ASPDAC | 2023 |
| Best Paper Award Nomination | MLCAD | 2022 |
| Best Paper Award Nomination | DATE | 2021 |
| Best Paper Award Nomination | ASPDAC | 2019 |
| Best Paper Award Nomination | DAC | 2014 |
| Best Paper Award Nomination | ASPDAC | 2013 |
| Best Paper Award Nomination | ICCAD | 2011 |
| Ernest S. Kuh Early Career Award | CEDA | 2022 |
| Meritorious Service Award | SIGDA | 2021 |
| Outstanding Dissertation Award | EDAA | 2014 |
| Outstanding Students Abroad Award | China Scholarship Council | 2014 |
| SPIE Scholarship | SPIE | 2013 |
| IBM Ph.D. Scholarship | IBM | 2012 |
| 1st Place Award in CAD Contest | ICCAD | 2015 |
| 2nd Place Award in CAD Contest | ICCAD | 2018 |
| 2nd Place Award in CAD Contest | ICCAD | 2013 |
| 2nd Place Award in CAD Contest | ICCAD | 2012 |
| 3rd Place Award in ISPD Contest | ISPD | 2020 |
| 3rd Place Award in ISPD Contest | ISPD | 2017 |
| 2nd Place Award in ICDAR Competition | ICDAR | 2021 |

PUBLICATIONS

Journal Papers

- [J87] Ziyi Wang, Zhuolun He, Chen Bai, Haoyu Yang, Bei Yu, “Efficient Arithmetic Block Identification with Graph Learning and Network-flow”, accepted by IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**).
- [J86] Siting Liu, Yuan Pu, Peiyu Liao, Hongzhong Wu, Rui Zhang, Zhitang Chen, Wenlong Lv, Yibo Lin, Bei Yu, “FastGR : Global Routing on CPU-GPU with Heterogeneous Task Graph Scheduler”, accepted by IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**).

- [J85] Tinghuan Chen, Grace Li Zhang, Bei Yu, Bing Li, Ulf Schlichtmann, “Machine Learning in Advanced IC Design: A Methodological Survey”, accepted by IEEE Design & Test. (**Invited Paper**)
- [J84] Yilun Chen, Shijia Huang, Shu Liu, Bei Yu, Jiaya Jia, “DSGN++: Exploiting Visual-Spatial Relation for Stereo-based 3D Detectors”, accepted by IEEE Transactions on Pattern Analysis and Machine Intelligence (**TPAMI**).
- [J83] Yuzhe Ma, Xufeng Yao, Ran Chen, Ruiyu Li, Xiaoyong Shen, Bei Yu, “Small is Beautiful: Compressing Deep Neural Networks for Partial Domain Adaptation”, accepted by IEEE Transactions on Neural Networks and Learning Systems (**TNNLS**).
- [J82] Ran Chen, Shoubo Hu, Zhitang Chen, Shengyu Zhu, Bei Yu, Pengyun Li, Cheng Chen, Yu Huang, Jianye Hao, “A Unified Framework for Layout Pattern Analysis with Deep Causal Estimation”, accepted by IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**).
- [J81] Ziyang Yu, Guojin Chen, Yuzhe Ma, Bei Yu, “A GPU-enabled Level Set Method for Mask Optimization”, accepted by IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**).
- [J80] Jianwang Zhai, Chen Bai, Binwu Zhu, Yici Cai, Qiang Zhou, Bei Yu, “McPAT-Calib: A RISC-V BOOM Microarchitecture Power Modeling Framework”, accepted by IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**).
- [J79] Zhuotao Tian, Pengguang Chen, Xin Lai, Li Jiang, Shu Liu, Hengshuang Zhao, Bei Yu, Ming-Chang Yang, Jiaya Jia, “Adaptive Perspective Distillation for Semantic Segmentation”, accepted by IEEE Transactions on Pattern Analysis and Machine Intelligence (**TPAMI**).
- [J78] Hao Geng, Tinghuan Chen, Yuzhe Ma, Binwu Zhu, Bei Yu, “PTPT: Physical Design Tool Parameter Tuning via Multi-Objective Bayesian Optimization”, accepted by IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**).
- [J77] Qi Xu, Junpeng Wang, Qi Sun, Bo Yuan, Song Chen, Bei Yu, Yi Kang, Feng Wu, “Reliability-Driven Memristive Crossbar Design in Neuromorphic Computing Systems”, accepted by IEEE Transactions on Automation Science and Engineering (**TASE**).
- [J76] Tinghuan Chen, Bin Duan, Qi Sun, Meng Zhang, Guoqing Li, Hao Geng, Qianru Zhang, Bei Yu, “An Efficient Sharing Grouped Convolution via Bayesian Learning”, IEEE Transactions on Neural Networks and Learning Systems (**TNNLS**), vol. 33, no. 12, pp. 7367–7379, 2022.
- [J75] Qi Sun, Xufeng Yao, Arjun Ashok Rao, Bei Yu, Shiyan Hu, “Counteracting Adversarial Attacks in Autonomous Driving”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**), vol. 41, no. 12, pp. 5193–5206, 2022.
- [J74] Xiaodong Wang, Changhao Yan, Yuzhe Ma, Bei Yu, Fan Yang, Dian Zhou, Xuan Zeng, “Analog Circuit Yield Optimization via Freeze-Thaw Bayesian Optimization Technique”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**), vol. 41, no. 11, pp. 4887–4900, 2022.
- [J73] Wei Li, Yuzhe Ma, Yibo Lin, Bei Yu, “Adaptive Layout Decomposition with Graph Embedding Neural Networks”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**), vol. 41, no. 11, pp. 5030–5042, 2022.
- [J72] Qi Xu, Hao Geng, Tianming Ni, Song Chen, Bei Yu, Xiaoqing Wen, “Fortune: A New Fault-Tolerance TSV Configuration in Router-based Redundancy Structure”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**), vol. 41, no. 10, pp. 3182–3187, 2022.
- [J71] Martin Rapp, Hussam Amrouch, Yibo Lin, Bei Yu, David Z. Pan, Marilyn Wolf, Jorg Henkel, “MLCAD: A Survey of Research in Machine Learning for CAD”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**), vol. 41, no. 10, pp. 3162–3181, 2022. (**Keynote Paper**)
- [J70] Guojin Chen, Wanli Chen, Qi Sun, Yuzhe Ma, Haoyu Yang, Bei Yu, “DAMO: Deep Agile Mask Optimization for Full Chip Scale”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**), vol. 41, no. 9, pp. 3118–3131, 2022.
- [J69] Hao Geng, Yuzhe Ma, Qi Xu, Jin Miao, Subhendu Roy, Bei Yu, “High-Speed Adder Design Space Exploration via Graph Neural Processes”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**), vol. 41, no. 8, pp. 2657–2670, 2022.
- [J68] Hao Geng, Haoyu Yang, Lu Zhang, Fan Yang, Xuan Zeng, Bei Yu, “Hotspot Detection via Attention-based Deep Layout Metric Learning”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**), vol. 41, no. 8, pp. 2685–2698, 2022.
- [J67] Bentian Jiang, Lixin Liu, Yuzhe Ma, Bei Yu, Evangeline F.Y. Young, “Neural-ILT 2.0: Migrating ILT to Domain-specific and Multi-task-enabled Neural Network”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**), vol. 41, no. 8, pp. 2671–2684, 2022.
- [J66] Yiyang Jiang, Fan Yang, Bei Yu, Dian Zhou, Xuan Zeng, “Efficient Layout Hotspot Detection via Neural Architecture Search”, ACM Transactions on Design Automation of Electronic Systems (**TODAES**), vol. 27, no. 6, 2022.

- [J65] Tinghuan Chen, Qi Sun, Canhui Zhan, Changze Liu, Huatao Yu, Bei Yu, “[Deep H-GCN: Fast Analog IC Aging-induced Degradation Estimation](#)”, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 41, no. 7, pp. 1990–2003, 2022.
- [J64] Yibo Lin, Xiaohan Gao, Tinghuan Chen, Bei Yu, “Machine learning for digital circuit backend design”, *Micro/nano Electronics and Intelligent Manufacturing*, vol. 2, no. 3, 2022. (in Chinese)
- [J63] Qi Sun, Tinghuan Chen, Siting Liu, Jianli Chen, Hao Yu, Bei Yu, “[Correlated Multi-objective Multi-fidelity Optimization for HLS Directives Design](#)”, *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, vol. 27, no. 4, 2022.
- [J62] Wei Zhong, Shuxiang Hu, Yuzhe Ma, Haoyu Yang, Xiuyuan Ma, Bei Yu, “[Deep Learning-Driven Simultaneous Layout Decomposition and Mask Optimization](#)”, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 41, no. 3, pp. 709–722, 2022.
- [J61] Ran Chen, Wei Zhong, Haoyu Yang, Hao Geng, Fan Yang, Xuan Zeng, Bei Yu, “[Faster Region-based Hotspot Detection](#)”, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 41, no. 3, pp. 669–680, 2022.
- [J60] Haoyu Yang, Shuhe Li, Wen Chen, Piyush Pathak, Frank Gennari, Ya-Chieh Lai, Bei Yu, “[DeePattern: Layout Pattern Generation with Transforming Convolutional Auto-Encoder](#)”, *IEEE Transactions on Semiconductor Manufacturing (TSM)*, vol. 35, no. 1, pp. 67–77, 2022.
- [J59] Haocheng Li, Wing-Kai Chow, Gengjie Chen, Bei Yu, and Evangeline F.Y. Young, “[Pin-Accessible Legalization for Mixed-Cell-Height Circuits](#)”, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 41, no. 1, pp. 143–154, 2022.
- [J58] Wei Li, Yuzhe Ma, Qi Sun, Lu Zhang, Yibo Lin, Iris Hui-Ru Jiang, Bei Yu, David Z. Pan, “[OpenMPL: An Open Source Layout Decomposer](#)”, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 40, no. 11, pp. 2331–2344, 2021.
- [J57] Haocheng Li, Satwik Patnaik, Mohammed Ashraf, Haoyu Yang, Johann Knechtel, Bei Yu, Ozgur Sinanoglu, Evangeline F.Y. Young, “[Deep Learning Analysis for Split Manufactured Layouts with Routing Perturbation](#)”, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 40, no. 10, pp. 1995–2008, 2021.
- [J56] Guyue Huang, Jingbo Hu, Yifan He, Jialong Liu, Mingyuan Ma, Zhaoyang Shen, Juejian Wu, Yuanfan Xu, Hengrui Zhang, Kai Zhong, Xuefei Ning, Yuzhe Ma, Haoyu Yang, Bei Yu, Huazhong Yang, Yu Wang, “[Machine Learning for Electronic Design Automation: A Survey](#)”, *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, vol. 26, no. 5, 2021.
- [J55] Yiyang Jiang, Fan Yang, Bei Yu, Dian Zhou, Xuan Zeng, “[Efficient Layout Hotspot Detection via Binarized Residual Neural Network Ensemble](#)”, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 40, no. 7, pp. 1476–1488, 2021.
- [J54] Haoyu Yang, Shuhe Li, Cyrus Tabery, Bingqing Lin, Bei Yu, “[Bridging the Gap Between Layout Pattern Sampling and Hotspot Detection via Batch Active Learning](#)”, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 40, no. 7, pp. 1464–1475, 2021.
- [J53] Tinghuan Chen, Bingqing Lin, Hao Geng, Shiyan Hu, Bei Yu, “[Leveraging Spatial Correlation for Sensor Drift Calibration in Smart Building](#)”, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 40, no. 7, pp. 1273–1286, 2021.
- [J52] Haoyu Yang, Wei Zhong, Yuzhe Ma, Hao Geng, Ran Chen, Wanli Chen, Bei Yu, “[VLSI Mask Optimization: From Shallow To Deep Learning](#)”, *Integration, the VLSI Journal*, vol. 77, Mar., pp. 96–103, 2021.
- [J51] Xiaowei Xu, Xinyi Zhang, Bei Yu, Xiaobo Sharon Hu, Christopher Rowen, Jingtong Hu, Yiyu Shi, “[DAC-SDC Low Power Object Detection Challenge for UAV Applications](#)”, *IEEE Transactions on Pattern Analysis and Machine Intelligence (TPAMI)*, vol. 43, no. 2, pp. 392–403, 2021.
- [J50] Yuzhe Ma, Wei Zhong, Shuxiang Hu, Jih-Rong Gao, Jian Kuang, Jin Miao, Bei Yu, “[A Unified Framework for Simultaneous Layout Decomposition and Mask Optimization](#)”, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 39, no. 12, pp. 5069–5082, 2020.
- [J49] Grace Li Zhang, Bing Li, Meng Li, Bei Yu, David Z. Pan, Michaela Brunner, Georg Sigl, Ulf Schlichtmann, “[TimingCamouflage+: Netlist Security Enhancement with Unconventional Timing](#)”, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 39, no. 12, pp. 4482–4495, 2020.
- [J48] Hao Geng, Wei Zhong, Haoyu Yang, Yuzhe Ma, Joydeep Mitra, Bei Yu, “[SRAF Insertion via Supervised Dictionary Learning](#)”, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 39, no. 10, pp. 2849–2859, 2020.
- [J47] Haoyu Yang, Shuhe Li, Zihao Deng, Yuzhe Ma, Bei Yu, and Evangeline F. Y. Young, “[GAN-OPC: Mask Optimization with Lithography-guided Generative Adversarial Nets](#)”, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 39, no. 10, pp. 2822–2834, 2020.

- [J46] Kang Liu, Haoyu Yang, Yuzhe Ma, Benjamin Tan, Bei Yu, Evangeline F. Y. Young, Ramesh Karri, Siddharth Garg, “[Adversarial Perturbation Attacks on ML-based CAD: A Case Study on CNN-based Lithographic Hotspot Detection](#)”, *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, vol. 25, no. 5, 2020.
- [J45] Qi Xu, Song Chen, Hao GENG, Bo Yuan, Bei Yu, Feng Wu, Zhengfeng Huang, “[Fault Tolerance in Memristive Crossbar-Based Neuromorphic Computing Systems](#)”, *Integration, the VLSI Journal*, vol. 70, Jan., pp. 70–79, 2020.
- [J44] Xingquan Li, Bei Yu, Jianli Chen, Wenxing Zhu, “[DSA Guiding Template Assignment with Multiple Redundant Via and Dummy Via Insertion](#)”, *Integration, the VLSI Journal*, vol. 70, Jan., pp. 32–42, 2020.
- [J43] Yuzhe Ma, Subhendu Roy, Jin Miao, Jiamin Chen, Bei Yu, “[Cross-layer Optimization for High Speed Adders: A Pareto Driven Machine Learning Approach](#)”, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 38, no. 12, pp. 2298–2311, 2019.
- [J42] Qi Xu, Hao Geng, Song Chen, Bei Yu, Feng Wu, “[Memristive Crossbar Mapping for Neuromorphic Computing Systems on 3D IC](#)”, *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, vol. 25, no. 1, pp. 8:1–8:19, 2019.
- [J41] Meng Li, Bei Yu, Yibo Lin, Xiaoqing Xu, Wuxi Li, David Z. Pan, “[A Practical Split Manufacturing Framework for Trojan Prevention via Simultaneous Wire Lifting and Cell Insertion](#)”, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 38, no. 9, pp. 1585–1598, 2019.
- [J40] Meng Li, Kaveh Shamsi, Travis Meade, Zheng Zhao, Bei Yu, Yier Jin, David Z. Pan, “[Provably Secure Camouflaging Strategy for IC Protection](#)”, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 38, no. 8, pp. 1399–1412, 2019.
- [J39] Haoyu Yang, Jing Su, Yi Zou, Yuzhe Ma, Bei Yu, Evangeline F. Y. Young, “[Layout Hotspot Detection with Feature Tensor Generation and Deep Biased Learning](#)”, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 38, no. 6, pp. 1175–1187, 2019.
- [J38] Derong Liu, Bei Yu, Vinicius Livramento, Salim Chowdhury, Duo Ding, Huy Vo, Akshay Sharma, David Z. Pan, “[Synergistic Topology Generation and Route Synthesis for On-Chip Performance-Critical Signal Groups](#)”, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 38, no. 6, pp. 1147–1160, 2019.
- [J37] Song Chen, Qi Xu, Bei Yu, “[Adaptive 3D-IC TSV Fault Tolerance Structure Generation](#)”, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 38, no. 5, pp. 949–960, 2019.
- [J36] Qianru Zhang, Meng Zhang, Tinghuan Chen, Zhifei Sun, Yuzhe Ma, Bei Yu, “[Recent Advances in Convolutional Neural Network Acceleration](#)”, *Neurocomputing*, vol. 323, pp. 37–51, Jan., 2019.
- [J35] Xingquan Li, Bei Yu, Jiaojiao Ou, Jianli Chen, David Z. Pan, Wenxing Zhu, “[Graph Based Redundant Via Insertion and Guiding Template Assignment for DSA-MP](#)”, *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*, vol. 26, no. 11, pp. 2504–2517, 2018.
- [J34] Jian Kuang, Evangeline F. Y. Young, Bei Yu, “[CRMA: Incorporating Cut Redistribution with Mask Assignment to Enable the Fabrication of 1D Gridded Design](#)”, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 37, no. 10, pp. 2036–2049, 2018.
- [J33] Gengjie Chen, Chak-Wa Pui, Wing-Kai Chow, Ka-Chun Lam, Jian Kuang, Evangeline F. Y. Young, Bei Yu, “[RippleFPGA: Routability-Driven Simultaneous Packing and Placement for Modern FPGAs](#)”, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 37, no. 10, pp. 2022–2035, 2018.
- [J32] Yibo Lin, Bei Yu, Meng Li, David Z. Pan, “[Layout Synthesis for Topological Quantum Circuits with 1D and 2D Architectures](#)”, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 37, no. 8, pp. 1574–1587, 2018.
- [J31] Shiyuan Hu, Bei Yu, Huafeng Yu, “[Guest Editorial on Special Issue on Sustainable Cyber-Physical Systems](#)”, *IEEE Transactions on Sustainable Computing (TSUSC)*, vol. 3, no. 2, pp. 58–59, 2018..
- [J30] Yibo Lin, Bei Yu, Xiaoqing Xu, Jih-Rong Gao, Natarajan Viswanathan, Wen-Hao Liu, Zhuo Li, Charles J. Alpert, David Z. Pan, “[MrDP: Multiple-row Detailed Placement of Heterogeneous-sized Cells for Advanced Nodes](#)”, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 37, no. 6, pp. 1237–1250, 2018.
- [J29] Jin Miao, Meng Li, Subhendu Roy, Yuzhe Ma, Bei Yu, “[SD-PUF: Spliced Digital Physical Unclonable Function](#)”, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 37, no. 5, pp. 927–940, 2018.
- [J28] Derong Liu, Bei Yu, Salim Chowdhury, David Z. Pan, “[TILA-S: Timing-Driven Incremental Layer Assignment Avoiding Slew Violations](#)”, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 37, no. 1, pp. 231–244, 2018.
- [J27] Xiaotao Jia, Yici Cai, Qiang Zhou, Bei Yu, “[A Multi-Commodity Flow based Detailed Router with Efficient Acceleration Techniques](#)”, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 37, no. 1, pp. 217–230, 2018.

- [J26] Haoyu Yang, Luyang Luo, Jing Su, Chenxi Lin, Bei Yu, “[Imbalance Aware Lithography Hotspot Detection: A Deep Learning Approach](#)”, *Journal of Micro/Nanolithography, MEMS, and MOEMS (JM3)*, vol. 16, no. 3, 033504, 2017.
- [J25] Yibo Lin, Xiaoqing Xu, Bei Yu, Ross Baldick, David Z. Pan, “[Triple/Quadruple Patterning Layout Decomposition via Novel Linear Programming and Iterative Rounding](#)”, *Journal of Micro/Nanolithography, MEMS, and MOEMS (JM3)*, vol. 16, no. 2, 023507, 2017.
- [J24] Derong Liu, Bei Yu, Salim Chowdhury, David Z. Pan, “[Incremental Layer Assignment for Timing Optimization](#)”, *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, vol. 22, no. 75, pp. 75:1–75:25, 2017.
- [J23] Yibo Lin, Bei Yu, David Z. Pan, “[High Performance Dummy Fill Insertion with Coupling and Uniformity Constraints](#)”, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 36, no. 9, pp. 1532–1544, 2017.
- [J22] Qi Xu, Song Chen, Xiaodong Xu, Bei Yu, “[Clustered Fault Tolerance TSV Planning for 3D Integrated Circuits](#)”, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 36, no. 8, pp. 1287–1300, 2017.
- [J21] Yibo Lin, Bei Yu, Biying Xu, David Z. Pan, “[Triple Patterning Aware Detailed Placement Toward Zero Cross-Row Middle-of-Line Conflict](#)”, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 36, no. 7, pp. 1140–1152, 2017.
- [J20] Vinicius Livramento, Derong Liu, Salim Chowdhury, Bei Yu, Xiaoqing Xu, David Z. Pan, José Luís Güntzel, Luiz C. V. dos Santos, “[Incremental Layer Assignment Driven by an External Signoff Timing Engine](#)”, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 36, no. 7, pp. 1126–1139, 2017.
- [J19] Yibo Lin, Bei Yu, Yi Zou, Zhuo Li, Charles J. Alpert, David Z. Pan, “[Stitch Aware Detailed Placement for Multiple E-Beam Lithography](#)”, *Integration, the VLSI Journal*, vol. 58, June, pp. 47–54, 2017. **(Best Paper Award)**
- [J18] Meikang Qiu, Saurabh Garg, Rujkumar Buyya, Bei Yu, Shiyan Hu, “[Special Issue on Scalable Cyber-Physical Systems](#)”, *Journal of Parallel and Distributed Computing (JPDC)*, vol. 103, pp. 1–2, May 2017.
- [J17] Bingqing Lin, Bei Yu, “[Smart Building Uncertainty Analysis via Adaptive Lasso](#)”, *IET Cyber-Physical Systems: Theory & Applications (IET-CPS)*, vol. 2, no. 1, pp. 1–7, 2017.
- [J16] Tetsuaki Matsunawa, Bei Yu, David Z. Pan, “[Laplacian Eigenmaps and Bayesian Clustering Based Layout Pattern Sampling and Its Applications to Hotspot Detection and OPC](#)”, *Journal of Micro/Nanolithography, MEMS, and MOEMS (JM3)*, vol. 15, no. 4, 043504, 2016.
- [J15] Bei Yu, Xiaoqing Xu, Subhendu Roy, Yibo Lin, Jiaojiao Ou, David Z. Pan, “[Design for Manufacturability and Reliability in Extreme-Scaling VLSI](#)”, *Science China Information Sciences (SCIS)*, vol. 59, June, 061406:2, 2016.
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- [J13] Xiaoqing Xu, Bei Yu, Jih-Rong Gao, Che-Lun Hsu, David Z. Pan, “[PARR: Pin Access Planning and Regular Routing for Self-Aligned Double Patterning](#)”, *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, vol. 21, no. 3, pp. 42:1–42:21, 2016.
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- [J9] Xiaoqing Xu, Brian Cline, Greg Yeric, Bei Yu, David Z. Pan, “[Self-Aligned Double Patterning Aware Pin Access and Standard Cell Layout Co-Optimization](#)”, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 34, no. 5, pp. 699–712, 2015.
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- [J3] Kun Yuan, Bei Yu, David Z. Pan, “[E-Beam Lithography Stencil Planning and Optimization with Overlapped Characters](#)”, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 31, no. 2, pp. 167–179, Feb. 2012.
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- [C113] Qi Sun, Chen Bai, Hao Geng, Bei Yu, “[Deep Neural Network Hardware Deployment Optimization via Advanced Active Learning](#)”, IEEE/ACM Proceedings Design, Automation and Test in Europe (**DATE**), Feb. 01–05, 2021.
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- [C94] Yuzhe Ma, Zhuolun He, Wei Li, Tinghuan Chen, Lu Zhang, Bei Yu, “[Understanding Graphs in EDA: From Shallow to Deep Learning](#)”, ACM International Symposium on Physical Design (ISPD), Taipei, Mar. 25–Apr. 01, 2020. (**Invited Paper**)
- [C93] Haoyu Yang, Wei Zhong, Yuzhe Ma, Hao Geng, Ran Chen, Wanli Chen, Bei Yu, “[VLSI Mask Optimization: From Shallow To Deep Learning](#)”, IEEE/ACM Asian and South Pacific Design Automation Conference (ASP-DAC), Beijing, Jan. 13–16, 2020. (**Invited Paper**)
- [C92] Qi Sun, Tinghuan Chen, Jin Miao, Bei Yu, “[Power-Driven DNN Dataflow Optimization on FPGA](#)”, IEEE/ACM International Conference on Computer-Aided Design (**ICCAD**), Westminster, CO, Nov. 4–7, 2019. (**Invited Paper**)
- [C91] Yuzhe Ma, Ran Chen, Wei Li, Fanhua Shang, Wenjian Yu, Minsik Cho, Bei Yu, “[A Unified Approximation Framework for Compressing and Accelerating Deep Neural Networks](#)”, IEEE International Conference on Tools with Artificial Intelligence (ICTAI), Portland, OR, Nov. 4–6, 2019. (**Best Student Paper Award**)
- [C90] Wei Li, Yuzhe Ma, Qi Sun, Yibo Lin, Iris Hui-Ru Jiang, Bei Yu, David Z. Pan, “[OpenMPL: An Open Source Layout Decomposer](#)”, IEEE International Conference on ASIC (ASICON), Chongqing, China, Oct. 29–Nov. 1, 2019. (**Invited Paper**)
- [C89] Yuzhe Ma, Ziyang Yu, Bei Yu, “[CAD Tool Design Space Exploration via Bayesian Optimization](#)”, ACM/IEEE Workshop on Machine Learning for CAD (MLCAD), Alberta, Canada, Sep. 3–4, 2019.
- [C88] Haoyu Yang, Wen Chen, Piyush Pathak, Frank Gennari, Ya-Chieh Lai, Bei Yu, “[Automatic Layout Generation with Applications in Machine Learning Engine Evaluation](#)”, ACM/IEEE Workshop on Machine Learning for CAD (MLCAD), Alberta, Canada, Sep. 3–4, 2019.
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- [C84] Tinghuan Chen, Bingqing Lin, Hao Geng, Bei Yu, “[Sensor Drift Calibration via Spatial Correlation Model in Smart Building](#)”, ACM/IEEE Design Automation Conference (**DAC**), pp. 105:1–105:6, Las Vegas, NV, June 2–6, 2019.
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- [C82] Yiyang Jiang, Fan Yang, Hengliang Zhu, Bei Yu, Dian Zhou, Xuan Zeng, “[Efficient Layout Hotspot Detection via Binarized Residual Neural Network](#)”, ACM/IEEE Design Automation Conference (**DAC**), pp. 147:1–147:6, Las Vegas, NV, June 2–6, 2019.

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- [C80] Bentian Jiang, Xiaopeng Zhang, Ran Chen, Gengjie Chen, Peishan Tu, Wei Li, Evangeline F. Y. Young, Bei Yu, “[FIT: Fill Insertion Considering Timing](#)”, ACM/IEEE Design Automation Conference (DAC), pp. 221:1–221:6, Las Vegas, NV, June 2–6, 2019.
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- [C78] Haoyu Yang, Piyush Pathak, Frank Gennari, Ya-Chieh Lai, Bei Yu, “[Detecting Multi-Layer Layout Hotspots with Adaptive Squish Patterns](#)”, IEEE/ACM Asian and South Pacific Design Automation Conference (ASPDAC), pp. 299–304, Tokyo, Jan. 21–24, 2019. (**Invited Paper**)
- [C77] Xingquan Li, Bei Yu, Jianli Chen, Wenxing Zhu, “[A Local Optimal Method on DSA Guiding Template Assignment with Redundant Dummy Via Insertion](#)”, IEEE/ACM Asian and South Pacific Design Automation Conference (ASPDAC), pp. 305–310, Tokyo, Jan. 21–24, 2019. (**Invited Paper**)
- [C76] Hao Geng, Haoyu Yang, Yuzhe Ma, Joydeep Mitra, Bei Yu, “[SRAF Insertion via Supervised Dictionary Learning](#)”, IEEE/ACM Asian and South Pacific Design Automation Conference (ASPDAC), pp. 406–411, Tokyo, Jan. 21–24, 2019. (**Best Paper Award Nomination**)
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- [C74] Hao Geng, Haoyu Yang, Bei Yu, Xingquan Li, Xuan Zeng, “[Sparse VLSI Layout Feature Extraction: A Dictionary Learning Approach](#)”, IEEE Computer Society Annual Symposium on VLSI (ISVLSI), pp. 488–493, Hong Kong, July 9–11, 2018. (**Invited Paper**)
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- [C72] Haocheng Li, Wing-Kai Chow, Gengjie Chen, Evangeline F. Y. Young, Bei Yu, “[Routability-Driven and Fence-Aware Legalization for Mixed-Cell-Height Circuits](#)”, ACM/IEEE Design Automation Conference (DAC), pp. 150:1–150:6, San Francisco, CA, June 24–28, 2018.
- [C71] Fengxian Jiao, Sheqin Dong, Bei Yu, Bing Li, Ulf Schlichtmann, “[Thermal-Aware Placement and Routing for 3D Optical Networks-on-Chips](#)”, IEEE International Symposium on Circuits and Systems (ISCAS), pp. 1–4, Florence, May 27–30, 2018.
- [C70] Qi Xu, Song Chen, Bei Yu, Feng Wu, “[Memristive Crossbar Mapping for Neuromorphic Computing Systems on 3D IC](#)”, ACM Great Lakes Symposium on VLSI (GLSVLSI), pp. 451–454, Chicago, IL, May 23–25, 2018.
- [C69] Wei Ye, Meng Li, Kai Zhong, Bei Yu, David Z. Pan, “[Power Grid Reduction by Sparse Convex Optimization](#)”, ACM International Symposium on Physical Design (ISPD), pp. 60–67, Monterey, CA, Mar. 25–28, 2018.
- [C68] Grace Li Zhang, Bing Li, Bei Yu, David Z. Pan, Ulf Schlichtmann, “[TimingCamouflage: Improving Circuit Security against Counterfeiting by Unconventional Timing](#)”, IEEE/ACM Proceedings Design, Automation and Test in Europe (DATE), pp. 91–96, Dresden, Mar. 19–23, 2018.
- [C67] Meng Li, Bei Yu, Yibo Lin, Xiaoqing Xu, Wuxi Li, David Z. Pan, “[A Practical Split Manufacturing Framework for Trojan Prevention via Simultaneous Wire Lifting and Cell Insertion](#)”, IEEE/ACM Asian and South Pacific Design Automation Conference (ASPDAC), pp. 265–270, Jeju Island, Jan. 22–25, 2018.
- [C66] Chak-Wa Pui, Gengjie Chen, Yuzhe Ma, Evangeline F. Y. Young, Bei Yu, “[Clock-Aware UltraScale FPGA Placement with Machine Learning Routability Prediction](#)”, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), pp. 929–936, Irvine, CA, Nov. 13–16, 2017. (**Invited Paper**)
- [C65] Yuzhe Ma, Jih-Rong Gao, Jian Kuang, Jin Miao, Bei Yu, “[A Unified Framework for Simultaneous Layout Decomposition and Mask Optimization](#)”, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), pp. 81–88, Irvine, CA, Nov. 13–16, 2017.
- [C64] Yuzhe Ma, Xuan Zeng, Bei Yu, “[Methodologies for Layout Decomposition and Mask Optimization: A Systematic Review](#)”, IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC), Abu Dhabi, UAE, Oct. 23–25, 2017. (**Invited Paper**)
- [C63] Cheng Zhuo, Bei Yu, Di Gao, “[Accelerating Chip Design with Machine Learning: From Pre-Silicon to Post-Silicon](#)”, IEEE International System-on-Chip Conference (SOCC), pp. 227–232, Munich, Germany, September 5–8, 2017. (**Invited Paper**)
- [C62] Haoyu Yang, Yajun Lin, Bei Yu, Evangeline F. Y. Young, “[Lithography Hotspot Detection: From Shallow To Deep Learning](#)”, IEEE International System-on-Chip Conference (SOCC), pp. 233–238, Munich, Germany, September 5–8, 2017. (**Invited Paper**)

- [C61] Subhendu Roy, Yuzhe Ma, Jin Miao, Bei Yu, “[A Learning Bridge from Architectural Synthesis to Physical Design for Exploring Power Efficient High-Performance Adders](#)”, IEEE International Symposium on Low Power Electronics and Design (ISLPED), Taipei, July 24–26, 2017.
- [C60] Haoyu Yang, Jing Su, Yi Zou, Bei Yu, Evangeline F. Y. Young, “[Layout Hotspot Detection with Feature Tensor Generation and Deep Biased Learning](#)”, ACM/IEEE Design Automation Conference (DAC), pp. 62:1–62:6, Austin, TX, June 18–22, 2017.
- [C59] Gengjie Chen, Jian Kuang, Zhiliang Zeng, Hang Zhang, Evangeline F. Y. Young, Bei Yu, “[Minimizing Thermal Gradient and Pumping Power in 3D IC Liquid Cooling Network Design](#)”, ACM/IEEE Design Automation Conference (DAC), pp. 70:1–70:6, Austin, TX, June 18–22, 2017.
- [C58] Soumi Chattopadhyay, Ansuman Banerjee, Bei Yu, “[A Utility-Driven Data Transmission Optimization Strategy in Large Scale Cyber-Physical Systems](#)”, IEEE/ACM Proceedings Design, Automation and Test in Europe (DATE), pp. 1619–1622, Lausanne, Mar. 27–31, 2017.
- [C57] Hang Zhang, Fengyuan Zhu, Haocheng Li, Evangeline F. Y. Young, Bei Yu, “[Bilinear Lithography Hotspot Detection](#)”, ACM International Symposium on Physical Design (ISPD), pp. 7–14, Portland, OR, Mar. 19–22, 2017. **(Best Paper Award)**
- [C56] Jiaojiao Ou, Bei Yu, Xiaoqing Xu, Joydeep Mitra, Yibo Lin, David Z. Pan, “[DSAR: DSA aware Routing with Simultaneous DSA Guiding Pattern and Double Patterning Assignment](#)”, ACM International Symposium on Physical Design (ISPD), pp. 91–98, Portland, OR, Mar. 19–22, 2017.
- [C55] Haoyu Yang, Luyang Luo, Jing Su, Chenxi Lin, Bei Yu, “[Imbalance Aware Lithography Hotspot Detection: A Deep Learning Approach](#)”, SPIE Intl. Symp. Advanced Lithography Conference, San Jose, CA, Feb. 26–Mar. 2, 2017.
- [C54] Chak-Wa Pui, Gengjie Chen, Wing-Kai Chow, Jian Kuang, Ka-Chun Lam, Peishan Tu, Hang Zhang, Evangeline F. Y. Young, Bei Yu, “[RippleFPGA: A Routability-Driven Placement for Large-Scale Heterogeneous FPGAs](#)”, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), pp. 67:1–67:8, Austin, TX, Nov. 7–10, 2016. **(Invited Paper)**
- [C53] Jian Kuang, Evangeline F. Y. Young, Bei Yu, “[Incorporating Cut Redistribution with Mask Assignment to Enable 1D Gridded Design](#)”, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), pp. 48:1–48:8, Austin, TX, Nov. 7–10, 2016.
- [C52] Hang Zhang, Bei Yu, Evangeline F. Y. Young, “[Enabling Online Learning in Lithography Hotspot Detection with Information-Theoretic Feature Optimization](#)”, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), pp. 47:1–47:8, Austin, TX, Nov. 7–10, 2016.
- [C51] Jin Miao, Meng Li, Subhendu Roy, Bei Yu, “[LRR-DPUF: Learning Resilient and Reliable Digital Physical Unclonable Function](#)”, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), pp. 46:1–46:8, Austin, TX, Nov. 7–10, 2016.
- [C50] Meng Li, Kaveh Shamsi, Travis Meade, Zheng Zhao, Bei Yu, Yier Jin, David Z. Pan, “[Provably Secure Camouflaging Strategy for IC Protection](#)”, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), pp. 28:1–28:8, Austin, TX, Nov. 7–10, 2016.
- [C49] Yibo Lin, Bei Yu, Xiaoqing Xu, Jih-Rong Gao, Natarajan Viswanathan, Wen-Hao Liu, Zhuo Li, Charles J. Alpert, David Z. Pan, “[MrDP: Multiple-row Detailed Placement of Heterogeneous-sized Cells for Advanced Nodes](#)”, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), pp. 7:1–7:8, Austin, TX, Nov. 7–10, 2016.
- [C48] Yibo Lin, Bei Yu, David Z. Pan, “[Detailed Placement In Advanced Technology Nodes: A Survey](#)”, IEEE International Conference on Solid -State and Integrated Circuit Technology (ICSICT), Hangzhou, Oct. 25–28, 2016. **(Invited Paper)**
- [C47] Hang Zhang, Haoyu Yang, Bei Yu, Evangeline F. Y. Young, “[VLSI Layout Hotspot Detection Based on Discriminative Feature Extraction](#)”, IEEE Asia Pacific Conference on Circuits and Systems (APCCAS), Jeju, Oct. 25–28, 2016. **(Invited Paper)**
- [C46] Derong Liu, Bei Yu, Salim Chowdhury, David Z. Pan, “[Incremental Layer Assignment for Critical Path Timing](#)”, ACM/IEEE Design Automation Conference (DAC), pp. 85:1–85:6, Austin, TX, June 5–9, 2016.
- [C45] Xiaotao Jia, Qiang Zhou, Yici Cai, Bei Yu, “[MCFRoute 2.0: A Redundant Via Insertion Enhanced Concurrent Detailed Router](#)”, ACM Great Lakes Symposium on VLSI (GLSVLSI), pp. 87–92, Boston, MA, May 18–20, 2016.
- [C44] Jiaojiao Ou, Bei Yu, David Z. Pan, “[Concurrent Guiding Template Assignment and Redundant Via Insertion for DSA-MP Hybrid Lithography](#)”, ACM International Symposium on Physical Design (ISPD), pp. 39–46, Sonoma, CA, April 3–6, 2016.
- [C43] Yibo Lin, Xiaoqing Xu, Bei Yu, Ross Baldick, David Z. Pan, “[Triple/Quadruple Patterning Layout Decomposition via Novel Linear Programming and Iterative Rounding](#)”, SPIE Intl. Symp. Advanced Lithography Conference, San Jose, CA, Feb. 21–25, 2016. **(Best Student Paper Award)**

- [C42] Tetsuaki Matsunawa, Bei Yu, David Z. Pan, “[Laplacian Eigenmaps and Bayesian Clustering Based Layout Pattern Sampling and Its Applications to Hotspot Detection and OPC](#)”, IEEE/ACM Asian and South Pacific Design Automation Conference (ASPDAC), pp. 679–684, Macau, Jan. 25–28, 2016.
- [C41] Yibo Lin, Bei Yu, Yi Zou, Zhuo Li, Charles J. Alpert, David Z. Pan, “[Stitch Aware Detailed Placement for Multiple E-Beam Lithography](#)”, IEEE/ACM Asian and South Pacific Design Automation Conference (ASPDAC), pp. 186–191, Macau, Jan. 25–28, 2016.
- [C40] Bei Yu, Derong Liu, Salim Chowdhury, David Z. Pan, “[TILA: Timing-Driven Incremental Layer Assignment](#)”, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), pp. 110–117, Austin, TX, Nov. 2–6, 2015.
- [C39] Yibo Lin, Bei Yu, Biying Xu, David Z. Pan, “[Triple Patterning Aware Detailed Placement Toward Zero Cross-Row Middle-of-Line Conflict](#)”, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), pp. 396–403, Austin, TX, Nov. 2–6, 2015.
- [C38] David Z. Pan, Lars Liebmann, Bei Yu, Xiaoqing Xu, Yibo Lin, “[Pushing Multiple Patterning in Sub-10nm: Are We Ready?](#)”, ACM/IEEE Design Automation Conference (DAC), pp. 197:1–197:6, San Francisco, CA, June 7–11, 2015. (**Invited Paper**)
- [C37] Xiaoqing Xu, Bei Yu, Jih-Rong Gao, Che-Lun Hsu, David Z. Pan, “[PARR: Pin Access Planning and Regular Routing for Self-Aligned Double Patterning](#)”, ACM/IEEE Design Automation Conference (DAC), pp. 28:1–28:6, San Francisco, CA, June 7–11, 2015.
- [C36] Yibo Lin, Bei Yu, David Z. Pan, “[High Performance Dummy Fill Insertion with Coupling and Uniformity Constraints](#)”, ACM/IEEE Design Automation Conference (DAC), pp. 71:1–71:6, San Francisco, CA, June 7–11, 2015.
- [C35] Wei Ye, Bei Yu, Yong-Chan Ban, Lars Liebmann, David Z. Pan, “[Standard Cell Layout Regularity and Pin Access Optimization Considering Middle-of-Line](#)”, ACM Great Lakes Symposium on VLSI (GLSVLSI), pp. 289–294, Pittsburgh, PA, May 20–22, 2015.
- [C34] Jiaojiao Ou, Bei Yu, Jih-Rong Gao, Moshe Preil, Azat Latypov, David Z. Pan, “[Directed Self-Assembly Based Cut Mask Optimization for Unidirectional Design](#)”, ACM Great Lakes Symposium on VLSI (GLSVLSI), pp. 83–86, Pittsburgh, PA, May 20–22, 2015.
- [C33] Tetsuaki Matsunawa, Bei Yu, David Z. Pan, “[Optical proximity correction with hierarchical Bayes model](#)”, SPIE Intl. Symp. Advanced Lithography - Optical Microlithography XXVIII, San Jose, CA, Feb. 22–26, 2015.
- [C32] Tetsuaki Matsunawa, Jih-Rong Gao, Bei Yu, David Z. Pan, “[A new lithography hotspot detection framework based on AdaBoost classifier and simplified feature extraction](#)”, SPIE Intl. Symp. Advanced Lithography - Design-Process-Technology Co-optimization for Manufacturability IX, San Jose, CA, Feb. 22–26, 2015.
- [C31] Xiaoqing Xu, Brian Cline, Greg Yeric, Bei Yu, David Z. Pan, “[A systematic framework for evaluating standard cell middle-of-line \(MOL\) robustness for multiple patterning](#)”, SPIE Intl. Symp. Advanced Lithography - Design-Process-Technology Co-optimization for Manufacturability IX, San Jose, CA, Feb. 22–26, 2015.
- [C30] Bei Yu, David Z. Pan, Tetsuaki Matsunawa, Xuan Zeng, “[Machine Learning and Pattern Matching in Physical Design](#)”, IEEE/ACM Asian and South Pacific Design Automation Conference (ASPDAC), pp. 286–293, Japan, Jan. 19–22, 2015. (**Invited Paper**)
- [C29] Jiwoo Pak, Bei Yu, David Z. Pan, “[Electromigration-aware Redundant Via Insertion](#)”, IEEE/ACM Asian and South Pacific Design Automation Conference (ASPDAC), pp. 544–549, Japan, Jan. 19–22, 2015.
- [C28] Bei Yu, Gilda Garretton, David Z. Pan, “[Layout Compliance for Triple Patterning Lithography: An Iterative Approach](#)”, SPIE/BACUS Photomask Symposium, Monterey, CA, Sept. 16–18, 2014. (**Invited Paper**)
- [C27] Bei Yu, David Z. Pan, “[Layout Decomposition for Quadruple Patterning Lithography and Beyond](#)”, SRC Techcon Conference, Austin, TX, Sept. 7–9, 2014.
- [C26] Jih-Rong Gao, Xiaoqing Xu, Bei Yu, David Z. Pan, “[MOSAIC: Mask Optimizing Solution With Process Window Aware Inverse Correction](#)”, ACM/IEEE Design Automation Conference (DAC), pp. 52:1–52:6, San Francisco, CA, June 1–5, 2014. (**Best Paper Award Nomination**)
- [C25] Bei Yu, David Z. Pan, “[Layout Decomposition for Quadruple Patterning Lithography and Beyond](#)”, ACM/IEEE Design Automation Conference (DAC), pp. 53:1–53:6, San Francisco, CA, June 1–5, 2014.
- [C24] Xiaoqing Xu, Brian Cline, Greg Yeric, Bei Yu, David Z. Pan, “[Self-Aligned Double Patterning Aware Pin Access and Standard Cell Layout Co-Optimization](#)”, ACM International Symposium on Physical Design (ISPD), pp. 101–108, Petaluma, CA, March 30–April 2, 2014.
- [C23] Jih-Rong Gao, Bei Yu, Duo Ding, David Z. Pan, “[Accurate lithography hotspot detection based on PCA-SVM classifier with hierarchical data clustering](#)”, SPIE Intl. Symp. Advanced Lithography - Design-Process-Technology Co-optimization for Manufacturability VIII, San Jose, CA, Feb. 23–27, 2014.
- [C22] Bei Yu, Jih-Rong Gao, Xiaoqing Xu, David Z. Pan, “[Bridging the Gap from Mask to Physical Design for Multiple Patterning Lithography](#)”, SPIE Intl. Symp. Advanced Lithography - Design-Process-Technology Co-optimization for Manufacturability VIII, San Jose, CA, Feb. 23–27, 2014. (**Invited Paper**)

- [C21] Jhih-Rong Gao, Bei Yu, David Z. Pan, “[Self-Aligned Double Patterning Layout Decomposition with Complementary E-Beam Lithography](#)”, IEEE/ACM Asian and South Pacific Design Automation Conference (ASPDAC), pp. 143–148, Singapore, Jan. 20–23, 2014.
- [C20] Bei Yu, Xiaoqing Xu, Jhih-Rong Gao, David Z. Pan, “[Methodology for Standard Cell Compliance and Detailed Placement for Triple Patterning Lithography](#)”, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), pp. 349–356, San Jose, CA, Nov. 18–21, 2013. (**William J. McCalla Best Paper Award**)
- [C19] Bei Yu, Yen-Hung Lin, Gerard Luk-Pat, Duo Ding, Kevin Lucas, David Z. Pan, “[A High-Performance Triple Patterning Layout Decomposer with Balanced Density](#)”, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), pp. 163–169, San Jose, CA, Nov. 18–21, 2013.
- [C18] Jhih-Rong Gao, Bei Yu, Duo Ding, David Z. Pan, “[Lithography Hotspot Detection and Mitigation in Nanometer VLSI](#)”, IEEE International Conference on ASIC (ASICON), pp. 1–4, Shenzhen, China, Oct. 28–31, 2013. (**Invited Paper**)
- [C17] Bei Yu, Kun Yuan, Jhih-Rong Gao, David Z. Pan, “[E-BLOW: E-Beam Lithography Overlapping aware Stencil Planning for MCC System](#)”, ACM/IEEE Design Automation Conference (DAC), pp. 70:1–70:7, Austin, TX, June 2–6, 2013.
- [C16] Bei Yu, Jhih-Rong Gao, David Z. Pan, “[Triple-patterning lithography \(TPL\) layout decomposition using end-cutting](#)”, SPIE Intl. Symp. Advanced Lithography, San Jose, CA, Feb. 24–28, 2013.
- [C15] Jhih-Rong Gao, Bei Yu, Ru Huang, David Z. Pan, “[Self-aligned Double Patterning Friendly Configuration for Standard Cell Library Considering Placement](#)”, SPIE Intl. Symp. Advanced Lithography, San Jose, CA, Feb. 24–28, 2013.
- [C14] Bei Yu, Jhih-Rong Gao, David Z. Pan, “[L-Shape based Layout Fracturing for E-Beam Lithography](#)”, IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), pp. 249–254, Japan, Jan. 22–25, 2013. (**Best Paper Award Nomination**)
- [C13] Bei Yu, Jhih-Rong Gao, Duo Ding, Yongchan Ban, Jae-Seok Yang, Kun Yuan, Minsik Cho, David Z. Pan, “[Dealing with IC Manufacturability in Extreme Scaling](#)”, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), pp. 240–242, San Jose, CA, Nov. 5–8, 2012. (**Embedded Tutorial paper**)
- [C12] Yen-Hung Lin, Bei Yu, David Z. Pan, Yih-Lang Li, “[TRIAD: A Triple Patterning Lithography Aware Detailed Router](#)”, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), pp. 123–129, San Jose, CA, Nov. 5–8, 2012.
- [C11] David Z. Pan, Jhih-Rong Gao, Bei Yu, “[VLSI CAD for Emerging Nanolithography](#)”, International Symposium on VLSI Design, Automation and Test (VLSI-DAT), pp. 1–4, 2012. (**Invited Paper**)
- [C10] Kevin Lucas, Chris Cork, Bei Yu, Gerry Luk-Pat, Ben Painter, David Z. Pan, “[Implications of triple patterning for 14 nm node design and patterning](#)”, SPIE Advanced Lithography Symposium Design for Manufacturability through Design-Process Integration VI (Conference 8327), Feb. 2012. (**Keynote Paper**)
- [C9] Duo Ding, Bei Yu, Joydeep Ghosh, David Z. Pan, “[EPIC: Efficient Prediction of IC Manufacturing Hotspots With A Unified Meta-Classification Formulatio](#)”, IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), pp. 263–270, Sydney, Australia, Jan. 30–Feb. 3, 2012. (**Best Paper Award**)
- [C8] Duo Ding, Bei Yu, David Z. Pan, “[GLOW: A Global Router for Low-Power Thermal-reliable Interconnect Synthesis using Photonic Wavelength Multiplexing](#)”, IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), pp. 621–626, Sydney, Australia, Jan. 30–Feb. 3, 2012.
- [C7] Bei Yu, Kun Yuan, Boyang Zhang, Duo Ding, David Z. Pan, “[Triple Patterning Lithography Layout Decomposition](#)”, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), pp. 1–8, San Jose, CA, Nov. 2011. (**William J. McCalla Best Paper Award Nomination**)
- [C6] Bei Yu, Sheqin Dong, Yuchun Ma, Tao Lin, Yu Wang, Song Chen, Satoshi Goto, “[Network Flow-based Simultaneous Retiming and Slack Budgeting for Low Power Design](#)”, IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), pp. 473–478, Japan, Jan. 2011.
- [C5] Wei Zhong, Bei Yu, Song Chen, Takeshi Yoshimura, Sheqin Dong, Satoshi Goto, “[Application-Specific Network-on-Chip Synthesis: Cluster Generation and Network Component Insertion](#)”, IEEE International Symposium on Quality Electronic Design (ISQED), pp. 144–149, Santa Clara, CA, March 14–16, 2011.
- [C4] Bei Yu, Sheqin Dong, Song Chen, Satoshi Goto, “[Floorplanning and Topology Generation for Application-Specific Network-on-Chip](#)”, IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), pp. 535–540, Taipei, Jan. 2010.
- [C3] Tao Lin, Sheqin Dong, Song Chen, Bei Yu, Satoshi Goto, “[A Revisit to Voltage Partitioning Problem](#)”, ACM Great Lakes Symposium on VLSI (GLSVLSI), pp. 115–118, Providence, RI, May 16–18, 2010.
- [C2] Bei Yu, Sheqin Dong, Satoshi Goto, “[Multi-Voltage and Level-Shifter Assignment Driven Floorplanning](#)”, IEEE International Conference on ASIC (ASICON), pp. 1264–1267, Changsha, Oct. 20–23, 2009.
- [C1] Bei Yu, Sheqin Dong, Song Chen, Satoshi Goto, “[Voltage-Island Driven Floorplanning Considering Level-Shifter Positions](#)”, ACM Great Lakes Symposium on VLSI (GLSVLSI), pp. 51–56, Boston, MA, May 10–12, 2009.

Books / Book Chapters

- [B4] Haoyu Yang, Yibo Lin, Bei Yu, “Machine Learning for Mask Synthesis and Verification”, in Machine Learning Applications in Electronic Design Automation, Mark Ren eds., Springer, 2022.
- [B3] Shiyun Hu, Bei Yu, “Big Data Analytics for Cyber-Physical Systems”, Springer, 2020.
- [B2] Bei Yu, David Z. Pan, “Design for Manufacturability with Advanced Lithography”, Springer, 2016.
- [B1] Bei Yu, David Z. Pan, “Layout Decomposition for Triple Patterning”, in Encyclopedia of Algorithms, M.-Y. Kao eds., Springer, 2015.

Dissertation

- [PHD] Bei Yu, “Design for Manufacturing with Advanced Lithography”, University of Texas at Austin, August 2014.
(EDAA Outstanding Dissertation Award)

Newsletters

- [N4] Qi Sun, Tinghuan Chen, Jin Miao, Bei Yu, “Power-Driven DNN Dataflow Optimization on FPGA”, IEEE TCCPS Newsletter, Volume 05, Issue 01, Mar. 2020.
- [N3] Bei Yu, “Design for Manufacturability: From Ad Hoc Solution To Extreme Regular Design”, VLSI Circuits and Systems Letter, Volume 1, Issue 2, Oct. 2015.
- [N2] Bei Yu, Gilda Garretton, David Z. Pan, “Layout Compliance for Triple Patterning Lithography: An Iterative Approach”, SPIE Newsroom.
- [N1] Kevin Lucas, Chris Cork, Bei Yu, David Z. Pan, Gerry Luk-Pat, Alex Miloslavsky, Ben Painter, “Triple patterning in 10nm node metal lithography”, SPIE Newsroom.

ADVISING AND SUPERVISORSHIP

Current Students:

| | | |
|--------------|-------|---------------------|
| Lu Zhang | MPhil | Fall 2018 – Present |
| Zhuolun He | Ph.D. | Fall 2019 – Present |
| Wanli Chen | Ph.D. | Fall 2019 – Present |
| Peiyu Liao | Ph.D. | Fall 2020 – Present |
| Wenqian Zhao | Ph.D. | Fall 2020 – Present |
| Yang Bai | Ph.D. | Fall 2020 – Present |
| Chen Bai | Ph.D. | Fall 2020 – Present |
| Binwu Zhu | Ph.D. | Fall 2020 – Present |
| Siting Liu | Ph.D. | Fall 2020 – Present |
| Yuxuan Zhao | Ph.D. | Fall 2021 – Present |
| Ziyi Wang | Ph.D. | Fall 2021 – Present |
| Hongduo Liu | Ph.D. | Fall 2021 – Present |
| Xufeng Yao | Ph.D. | Fall 2021 – Present |
| Xinyun Zhang | Ph.D. | Fall 2021 – Present |
| Guojin Chen | Ph.D. | Fall 2021 – Present |
| Ziyang Yu | Ph.D. | Fall 2021 – Present |
| Zixiao Wang | Ph.D. | Fall 2022 – Present |
| Peng Xu | Ph.D. | Fall 2022 – Present |
| Shixin Chen | Ph.D. | Fall 2022 – Present |
| Su Zheng | Ph.D. | Fall 2022 – Present |
| Yu Zhang | Ph.D. | Fall 2022 – Present |
| Shuo Yin | Ph.D. | Fall 2022 – Present |

Supervisions Completed:

| | | |
|---------------|------------|--|
| Qi Sun | PhD 2022 | Postdoc@Cornell |
| Ran Chen | PhD 2022 | Huawei Noah Lab |
| Hao Geng | PhD 2021 | Postdoc@CUHK → Assistant Professor @ShanghaiTech |
| Tinghuan Chen | PhD 2021 | Postdoc@CUHK |
| Wei Li | MPhil 2021 | PhD@CMU |
| Yuzhe Ma | PhD 2020 | Huawei → Assistant Professor @HKUST(GZ) |
| Haoyu Yang | PhD 2020 | Postdoc@CUHK → Cadence → nVIDIA |

Post-Doc Supervisions:

| | | |
|---------------|-------------------|-------------------------------|
| Tinghuan Chen | 2021/09 – | |
| Hao Geng | 2021/09 – 2022/03 | now Faculty @ShanghaiTech |
| Haoyu Yang | 2020/08 – 2021/03 | now Research Scientist@nVIDIA |

Ph.D. Defense Committees Served: 2016: Jian Kuang; 2017: Yannan Liu, Wen Zong; 2018: Lingxiao Wei, Wing-Kai Chow; 2019: Gengjie Chen, Chak-Wa Pui; 2020: Ye Tian; 2021: Shujun Wang, Yanning Zhou; Bentian

PROFESSIONAL SERVICE

University Committee Assignments

- Member, CUHK CSE Department Graduate Panel, 2016–present.
- Member, CUHK CSE Department Curriculum Committee, 2015–present.

Editorial Board

- **Editor**, Technical Committee on Cyber-Physical Systems (TC-CPS) Newsletter, 2019–present.
- Associate Editor, ACM Transactions on Design Automation of Electronic Systems (TODAES), 2020–present.
- Associate Editor, Integration, the VLSI Journal, 2016–present.
- Associate Editor, IET Cyber-Physical Systems: Theory & Applications, 2016–present.

Guest Editor

- IEEE Consumer Electronics Magazine Special Issue on ISVLSI
- IEEE Design & Test Special Issue on Machine Learning for CAD / EDA
- IEEE Transactions on Sustainable Computing (TSUSC) Special Issue on Sustainable Cyber-Physical Systems
- Integration, the VLSI Journal Special Issue on Emerging Technologies for System Level Design and Interconnects.
- Integration, the VLSI Journal Special Issue on ASP-DAC 2017.
- Journal of Parallel and Distributed Computing (JPDC) Special Issue on Scalable Cyber-Physical Systems

Selected Organizers

- **Chair**, IEEE Technical Committee on Secure and Dependable Measurement (TC-SDM), 2021–Present.
- **Chair**, ACM Student Research Competition at ICCAD, 2018, 2019.
- **Chair**, EDathon, 2022.
- Organizing Committee, IEEE CEDA Hong Kong Chapter, 2017–present.
- Organizing Committee, International System Design Contest at DAC, 2018, 2019.
- Organizing Committee, EDathon, 2017, 2018, 2019, 2020, 2021.

Selected PC Member

- AAAI Conference on Artificial Intelligence (AAAI), 2023.
- ACM/IEEE Workshop on Machine Learning for CAD (MLCAD), 2019 (TPC Co-Chair), 2020, 2021.
- ACM/IEEE Design Automation Conference (DAC), 2016, 2017, 2018.
- ACM International Symposium on Physical Design (ISPD), 2017, 2018, 2019, 2020, 2023.
- ACM Great Lakes Symposium on VLSI (GLSVLSI), 2016, 2017, 2018 (CAD Track Chair).
- IEEE/ACM International Conference On Computer Aided Design (ICCAD), 2016, 2017, 2018.
- IEEE/ACM Proceedings Design, Automation and Test in Europe (DATE), 2020, 2021.
- IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), 2018, 2019, 2020, 2021, 2022 (DFM Track Chair).
- IEEE International Conference on Computer Design (ICCD), 2021, 2022.
- International Joint Conference on Artificial Intelligence (IJCAI), 2020.