Bridging the Gap from Mask to Physical Design for Multiple Patterning Lithography

Bei Yu, Jhih-Rong Gao, Xiaoqing Xu, and David Z. Pan

ECE Dept. University of Texas at Austin, Austin, TX USA 78712
Email: {bei, jrgao, xiaoqingxu, dpan}@cerc.utexas.edu

ABSTRACT

Due to the delay of EUVL, multiple patterning techniques have been used to extend the 193nm lithography to 22nm/14nm nodes, and possibly further. There are many studies on MPL layout decompositions at the mask synthesis stage to resolve the coloring conflicts, minimize the stitches, balance the mask density, or even mitigate the undesirable overlay effects. Meanwhile, there are studies showing that it is very important to consider the multiple patterning implications at earlier physical design stages so that the overall design and manufacturing closure can be reached. In this paper, we will show some recent results and propose a unified physical design methodology for standard cell compliance, pin access, routing, and placement to bridge the gap from mask/layout decomposition to physical design, while accommodating various requirements from double/triple patterning lithography in certain "correct by construction" manner.

1. INTRODUCTION

Multiple patterning lithography (MPL) techniques have been used to extend the 193nm lithography to 22nm/14nm nodes, and possibly further,[1–4] due to the delay of extreme ultra violet lithography (EUVL)[5–8] and electric beam lithography (EBL).[9–11] Generally speaking, the MPL consists of double patterning lithography (DPL) and triple patterning lithography (TPL). There are two main types of DPL with different manufacturing processes: litho-etch-litho-etch (LELE) and self-align double patterning (SADP). Both of them can be extended for triple patterning. The most important issue for multiple patterning technique is how to successfully decompose the layout into several masks that can be manufactured under current 193nm optical lithography.[12–14] In general, when the pitch between two patterns is less than the lithography threshold, the patterns have to be separated into different masks. This process is called layout decomposition, or coloring. There are many studies on MPL layout decompositions at the mask synthesis stage to resolve the coloring conflicts, minimize the stitches, balance the mask density, or even mitigate the undesirable overlay effects.[12–36]

Meanwhile, there are studies showing that it is very important to consider the multiple patterning implications at earlier physical design stages so that the overall design and manufacturing closure can be reached.[37–48] Both multiple patterning aware standard cell library design and multiple patterning aware physical design flow are necessary to avoid undecomposable patterns in final layout. For example, if placement/routing techniques are not multiple patterning friendly, the final layout may introduce some conflicts. Since redesigning indecomposable patterns in the final layout requires high ECO efforts, generating multiple patterning friendly layouts, especially at the early design stage, becomes urgent and pivotal.

In this paper, we will show some recent results and propose a unified physical design methodology for standard cell compliance, pin access, routing, and placement to bridge the gap from mask/layout decomposition to physical design, while accommodating various requirements from double/triple patterning lithography in certain "correct by construction" manner.

The rest of the paper will be organized as follows: Section 2 gives an overview of our proposed multiple patterning aware design flow. Section 3 proposes standard cell level design to provide multiple patterning compliance. Section 4 and Section 5 present the methodologies in placement and routing, respectively. Section 6 shows some experimental results, followed by conclusion in Section 7.

Design-Process-Technology Co-optimization for Manufacturability VIII, edited by
John L. Sturtevant, Proc. of SPIE Vol. 9053, 905308 · © 2014 SPIE
CCC code: 0277-786X/14/$18 · doi: 10.1117/12.2048626

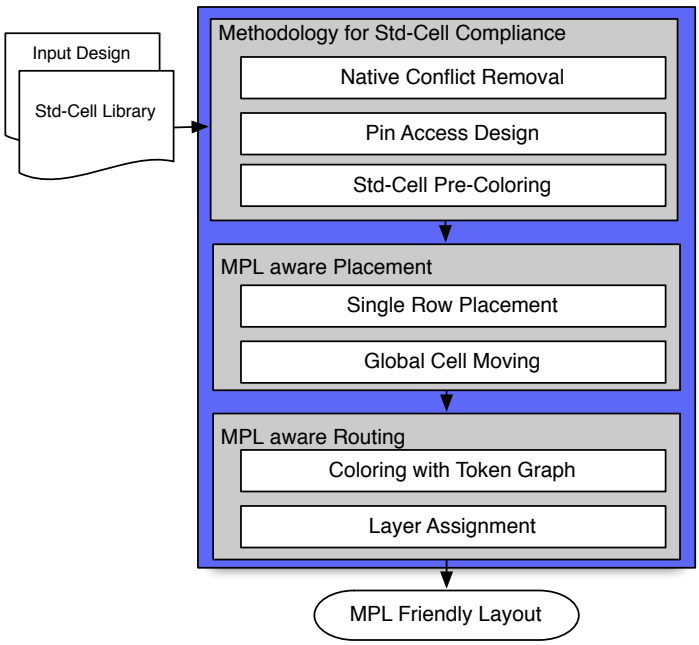

Figure 1. Our unified design flow for multiple patterning lithography.

2. OVERALL FLOW

The overall flow of our proposed framework is illustrated in Fig. 1. It consists of three stages: methodologies for standard cell compliance, MPL aware placement, and MPL aware routing. The first stage includes native conflict removal, pin access design, and standard cell pre-coloring. In the second stage, two techniques, i.e., single row placement and global cell moving, are provided to resolve cell placement and color assignment simultaneously. In the last stage, coloring and layer assignment techniques are applied to provide MPL friendly routing.

3. STANDARD CELL COMPLIANCE

The expectation to continue Moore's Law introduces new challenges into standard cell design. On one hand, without considering multiple patterning in standard cell design, the library may involve several cells with inner native conflicts. The inner native conflicts cannot be resolved through either cell shift or layout decomposition. Since one cell may be applied several times in one single design, one inner conflict may cause hundreds of coloring conflicts in final layout. On the other hand, the standard cell input/output (I/O) pins are accessed in more congested areas with increasingly restrictive rules. Unfortunately, the complex design rules and neighbor interactions that exist due to various multiple patterning techniques make human-driven layout almost impossible at 14nm technologies and below. Therefore, multiple patterning and I/O pins aware design are necessary in library design level. In this section we propose several techniques, including native conflict removal, pre-coloring, and pin access design, to achieve standard cell compliance.

3.1 Native Conflict Removal

Our first step to achieve standard cell compliance is the layout modification to resolve the native conflict for multiple patterning. For double patterning, odd-cycles are detected and resolved within cell. While for triple patterning, one typical native conflict, called 4-clique structure, is detected and modified. For example, we modify the contact layout into hexagonal close packing,[3] which also allows for the most aggressive cell area shrinkage for triple patterning friendly layout. From the layout analysis of different cells, we have various ways to remove such 4-clique conflict. As shown in Fig. 2, with slight modification to original layout, we can either choose to move contacts connected with power or ground rails or shift contacts on the signal paths of the cell. Note that after modification, the layout still needs to satisfy the design rules.

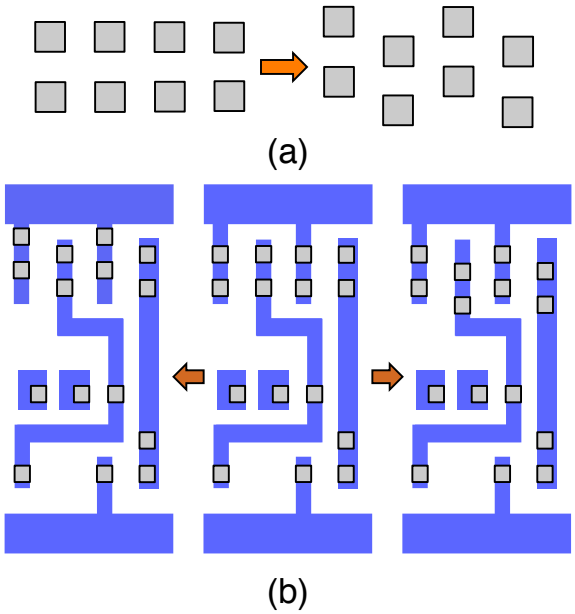

Figure 2. Contact layout modification to hexagonal packing.[3] (a) The principle for contact shifting; (b) Demonstration of two options for contact shifting, with original layout in the middle, case 1 on the left and case 2 on the right.

3.2 Standard Cell Pre-Coloring

After removing the native conflicts, our second step is to perform layout decomposition up front, and embed the coloring information in the cell library that can be used by the placer. With these pre-defined coloring solutions, during placement or even layout decomposition, checking the library can provide a quick coloring solution. It shall be noted that different from the conventional layout decomposition, pre-coloring could have more than one solution for each cell.

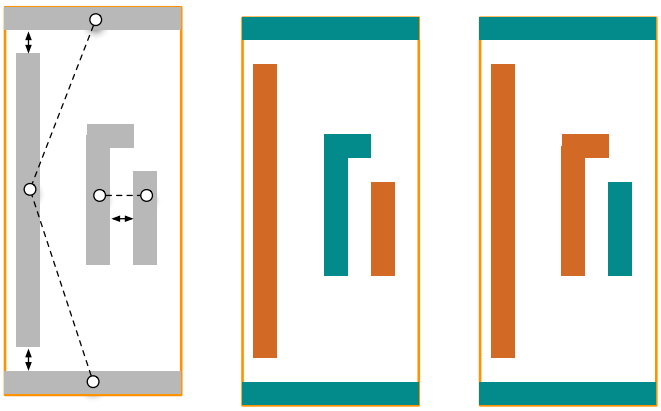

Figure 3. (a) Sample layout and its corresponding conflict graph in dashed lines. (b)-(c) Candidate coloring results for double patterning.

Given one cell, we build up a conflict graph to represent the topological relationship among patterns. Fig. 3 (a) shows a sample layout and its corresponding conflict graph. Based on the conflict graph, a set of graph coloring methodologies are presented to assign colors to all patterns.[47,48] For example, for both LELE-type and SADP-type double patterning, we traverse the conflict graph in DFS manner and apply two-coloring in the conflict graph. Note that the coloring assignment may not be unique. To achieve the most placement flexibility, we enumerate all possible coloring candidates (see Fig. 3 (b)-(c)).

3.3 Pin Access Design

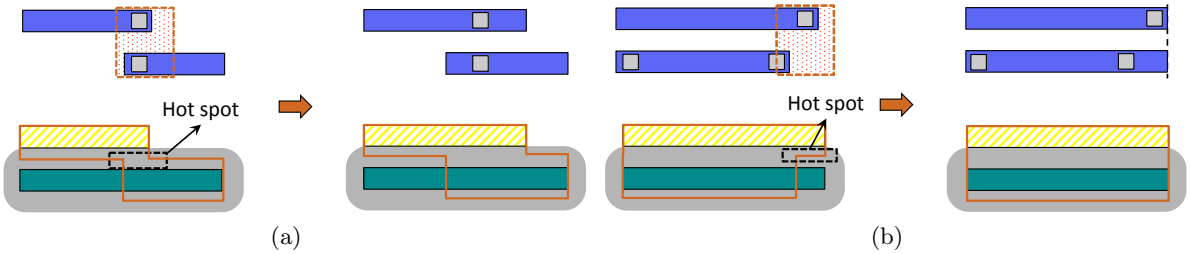

Figure 4. Line end extension techniques. (a) Anti-parallel line ends; (b) Parallel line ends.

Our third step for standard cell compliance is pin access design. Most modern-day designs primarily use Metal-1 for local connections and I/O pins, Metal-2 design is essential for I/O pin access. In addition, SADP is a viable candidate for lower layer metallization with regular patterns, due to better overlay and line edge roughness (LER) control. Therefore, currently our pin access design is targeting SADP-based Metal-2 wires. Specifically, because of the decomposition of SADP into the mandrel and trim masks, one cannot simply rely on via locations to determine line-end positions of Metal-2 wires. As shown in Fig. 4, SADP yield can be enhanced by simple line-end extensions that are dependent on both via placement and neighboring wire placement. For example, the parallel line-end alignment and extension of anti-parallel line ends both help to avoid hot spots on the trim masks. In general, the ideal location of geometries is not as straight-forward under SADP constraints and is more dependent on the neighborhood around the geometry in question. This means all SADP-based metal designs, including pin access and within-cell connections have to be optimized simultaneously during the pin access design phase.

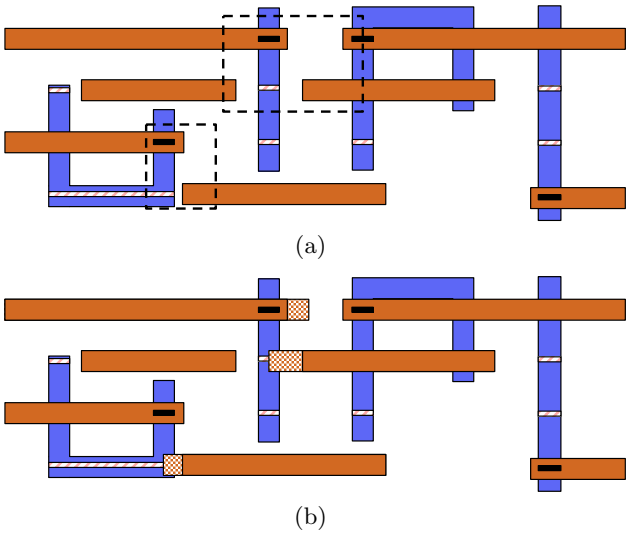

Figure 5. Pin access and cell connection co-optimization for one hit point combination. (a) Design rule violation in layout; (b) Optimization result.

Fig. 5 demonstrates a typical cell layout design in the 10nm technology node. The I/O pins for this cell are on the Metal-1 layer. Due to the complexity of this cell, Metal-2 wires are used for within-cell connections. Fig. 5(a) shows the Metal-2 layout design if we simply use *hit point* (Via-1) locations to determine the line end positions. A design rule check will reveal multiple violations in the dashed boxes. To resolve all the violations, we propose a pin access and Metal-2 wire co-optimization to enable SADP-friendly layout.[24] As illustrated in Fig. 5(b), the same Metal-2 wires for pin access and within-cell connections can be modified simultaneously. Our optimization also ensures the minimum amount of line end extension, while avoiding potential engineering efforts from design rule violation fixes.

4. MULTIPLE PATTERNING AWARE PLACEMENT

One grand challenge for placement under multiple patterning lithography is that there may be coloring conflict between adjacent cells. Actually the cell characterization itself may depend on its neighborhood and layout decomposition. Thus it will be very interesting to design new architecture of standard cells together with the coloring schemes to minimize the coloring conflict number. Also, it is still not universally agreed upon whether the cells shall be pre-colored (i.e., during the standard cell layout stage) or post-colored (i.e., flat after standard cell placement of of the entire chip). In the proposed framework, the cells are pre-colored. We believe that pre-coloring would be beneficial in achieving standard cell timing closure and cell level characterization.

4.1 Single Row Placement

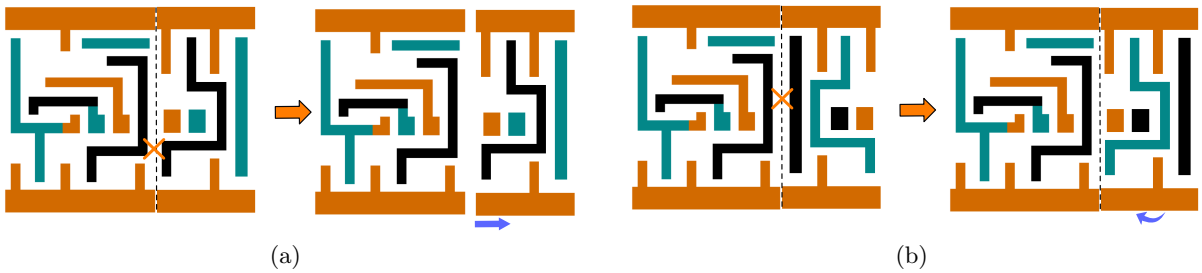

Figure 6. Two techniques for removing conflicts during placement.[48] (a) Flip the cell; (b) Shift the cell.

Firstly we solve a single row placement, where the orders of all cells on each row are determined. To resolve the coloring conflict between two abutted cells c_i, c_j, apart from picking up compatible coloring solutions, our MPL aware placement can seek to flip cells (see Fig. 6 (a)) or shift cells (see Fig. 6 (b)). We formulate this problem as a shortest path problem,[48] and solve it optimally. It shall be noted that compared with conventional color assignment problem, our solution space is much larger.

4.2 Global Cell Moving

In our overall placement scheme, all rows are sorted that the row with more cells occupied would be assign both colors and positions earlier. For one row, if there are some cells can not be assigned colors during single row placement, a stage called *Global Cell Moving* is applied to move the cells to other rows. The basic idea is to find the "optimal row and site" for a cell in the placement region, and resolve some local congestion.

5. MULTIPLE PATTERNING AWARE ROUTING

Routing is one of the most important stages in nanometer physical design, and it is oftentimes challenging multiple patterning conflicts reside. It is particularly serious in lower metal layers, e.g., Metal-2 and Metal-3, where routing density is very high. Thus upstream multiple patterning friendly routing will be important to obtain more flexibility and better quality. In this section we consider multiple patterning friendliness during routing in a correct-by-construction manner. Two techniques, coloring with token graph and layer assignment are proposed to assist router to search results with better multiple patterning friendliness.

5.1 Coloring with Token Graph

In double patterning the coloring conflicts can be detected by finding odd-cycles. However, detecting triple patterning or the more general multiple patterning coloring conflict during routing will be much more complicated, due to the higher complexity of conflict graph and higher flexibility for color assignment. We propose a general multiple patterning coloring techniques during routing stage.[44] A special data structure, token graph-embedded conflict graph (TECG) composed of token graph (TG) and conflict graph (CG), is presented to facilitate patterning conflict detection. During path searching, we adopts TECG to detect if any conflict occurs by the current routing wire segment. After detecting solvable conflicts, we utilize TECG to generate stitches in wire segments. With the assistance of TECG, our router can generate stitches which cannot be generated by adopting

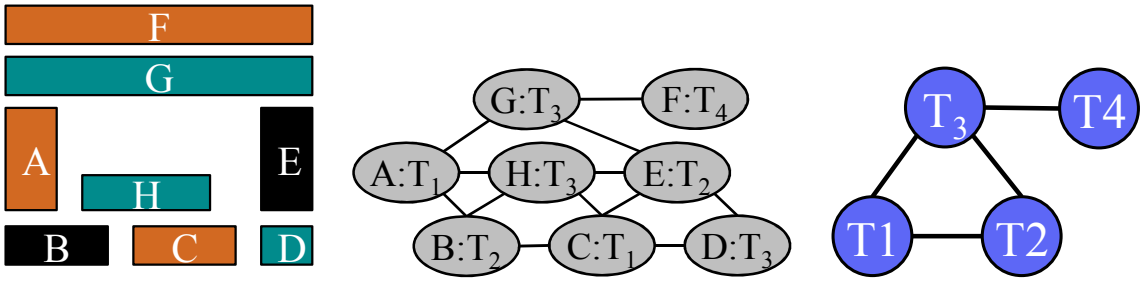

Figure 7. An example of token graph for triple patterning coloring. (a) Coloring solution; (b) Conflict graph and token assignment; (c) Token graph.

conventional double patterning stitch generation. TG is used to maintain the coloring relation among different vertex sets in CG. Instead of assigning physical colors into wire segments, tokens are used to represent the potential colors. In the case where three vertex comprise a three-clique, strictly colored component (SCC) is constructed to fix the coloring relation among these vertex sets in CG. Fig. 7(b) shows the TECG with one SCC $scc = (T_1, T_2, T_3)$ of the layout in (a). The coloring result in (a) can be obtained by assigning T_1, T_2, and T_3 to color c_1, c_2, and c_3, respectively, while T_4 can be assigned to c_1 or c_2. TG usually contains much less number of vertices than CG, making conflict detection more efficiently.

5.2 Layer Assignment

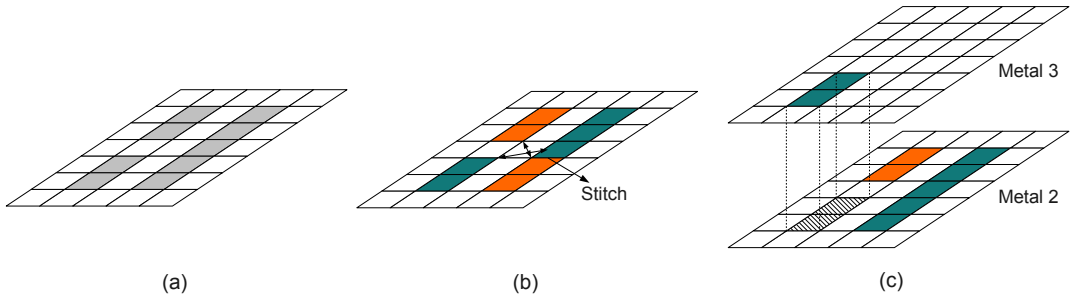

Figure 8. Prevent conflicts by prescribed layer assignment. (a) Target layout. (b) Conflicts (shown as arrows) remains even with stitch insertion. (c) Conflict removed by layer assignment.

Our second technique to resolve coloring conflicts during routing is *layer assignment*, which can be performed to separate conflicting patterns (see Fig. 8). By integrating the prescribed routing patterns together with the routing cost, our router can simultaneously perform multi-layer routing and layout decomposition in a correct-by-construction manner.

6. EXPERIMENTAL RESULTS

We have implemented our unified physical design flow in C++. All the experiments are performed on a Linux machine with 3.0GHz CPU.

6.1 Effectiveness of Pin Access Design

To gauge the effectiveness of our pin access design, we apply our methodologies in Section 3.3 to each cell in the library. We calculate the ratio of valid *hit point combinations* of our methodology over the conventional approach for each cell. Here a hit point combination is a set of hit points where each I/O pin in the standard cell is accessed exactly once. The histogram in Fig. 9 demonstrates the valid hit point combination ratio. We obtain 10x or more improvement for most cells and some cells achieve up to a 10000x increase in the number of valid hit point combinations. This means that our standard cell design has significantly improved the pin access flexibility for the routing stage.

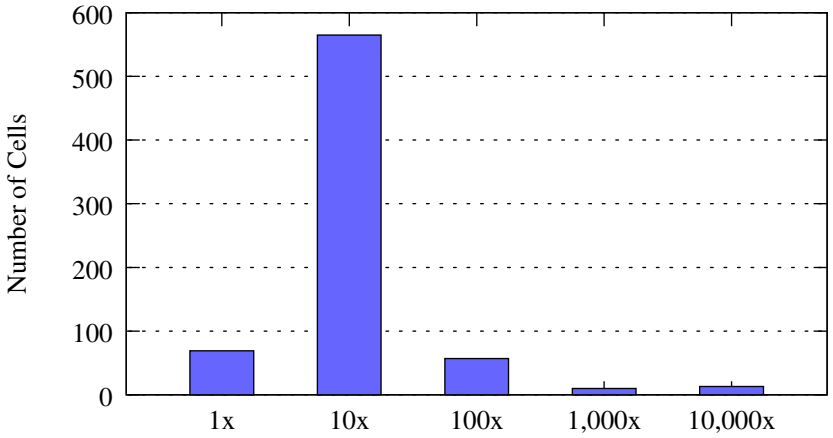

Figure 9. The increase in ratio on the number of valid hit point combinations across the entire cell library.

6.2 Effectiveness of MPL aware Placement

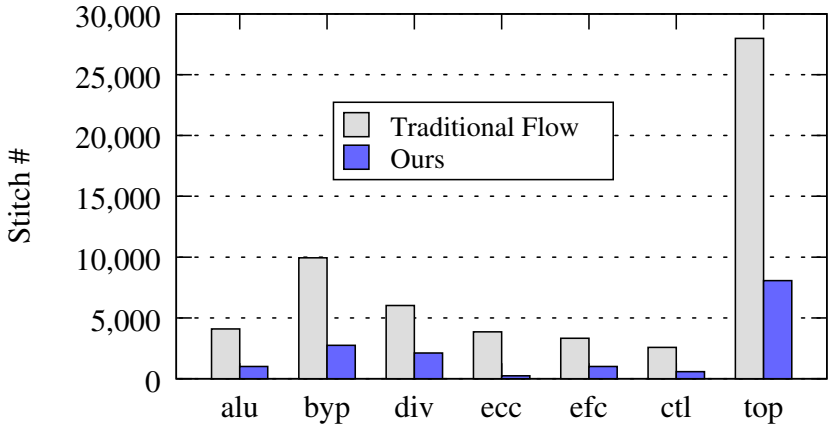

Figure 10. Effectiveness of MPL aware placement.

We further demonstrate the effectiveness of our MPL aware placement. We compare our new placer with conventional approach, where Encounter is chosen as the lacer and an academic decomposer[30] is applied for M1 layer layout decomposition. Note here the standard cell inner native conflicts have been removed through our compliance techniques (see Section 3.1). Under the conventional design flow, even each standard cell itself is multiple patterning friendly, averagely more than 1000 conflicts are reported in final decomposition. Our MPL aware placement can report zero conflict number. In addition, as illustrated in Fig. 10, our methodology can further reduce 72% of stitch number.

6.3 Effectiveness of MPL aware Routing

In the last experiment, we demonstrate the effectiveness of our MPL aware router against the conventional routing scheme with greedy color assignment approach.

For SADP, a set of two layer industrial designs (CK1-CK4) are scaled down to 22nm technology node for the experiment. As shown in Fig. 11, compared with greedy coloring method, our router achieves great improvement. It is worth mentioning that the benchmarks are quite dense and some areas contain congested pins which are difficult for multiple patterning techniques. Our approach outperforms wirelength-driven routing with much less conflicts.

We also test our MPL aware router on triple patterning benchmarks (S1-S6), as illustrated in Fig. 12, From this figure we can see that the average wirelength of our router is less than that of greedy method by 0.54%

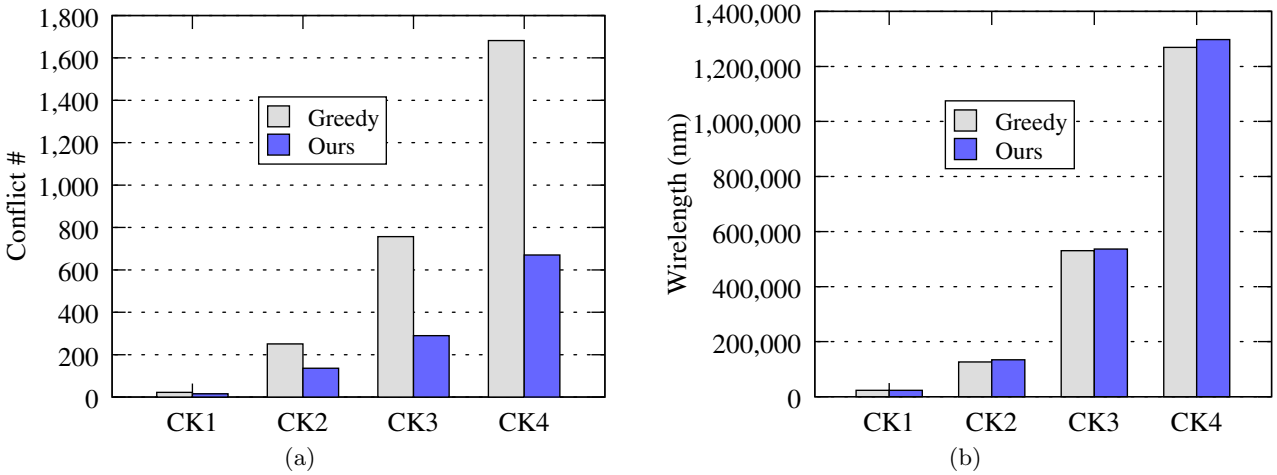

Figure 11. Effectiveness of our router for SADP.

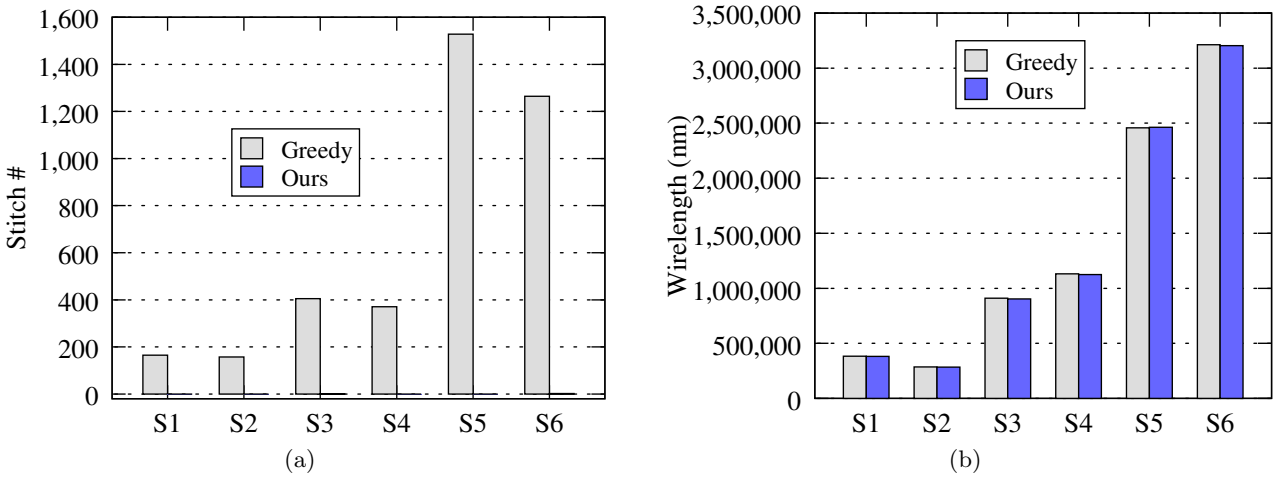

Figure 12. Effectiveness of our router for TPL.

because greedy method has to detour the routed colored wire segments to avoid conflicts. In addition, for these cases our router can generate conflict-free results, and with much less stitch number (see Fig. 12(a)).

7. CONCLUSION

In this paper, we propose a unified physical design flow for standard cell compliance, pin access, routing, and placement to bridge the gap from mask/layout decomposition to physical design. With further scaling of feature size into very deep sub-wavelength, the mask-level manipulation will be limited if the final layout after physical design is not lithography friendly. Therefore, it is necessary to integrate lithography awareness into nanometer physical design flow. Our preliminary results from such a unified flow are very promising. As multiple patterning lithography is being actively adopted by industry and it can also be used together with EUV, e-beam lithography, DSA, etc., we expect to see more research activies to bridge such gap.

Acknowledgment

This work is supported in part by NSF, SRC, NSFC, IBM and Intel.

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