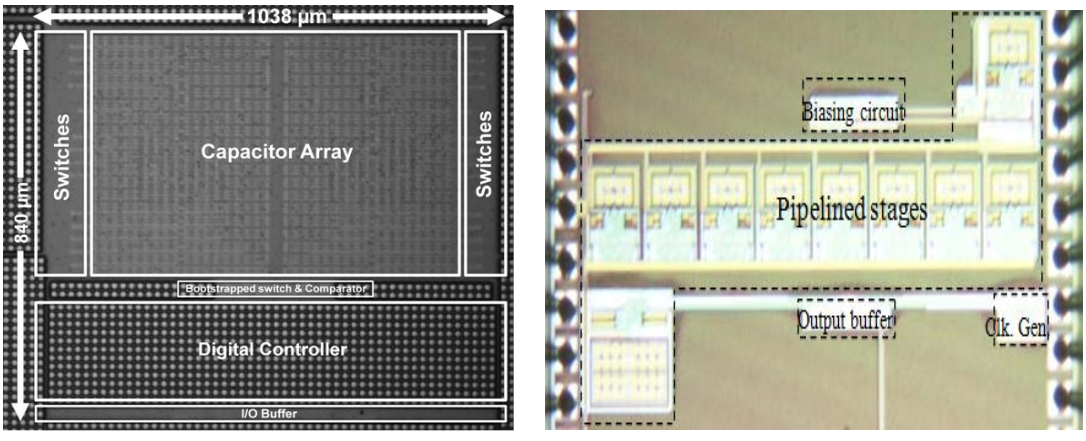
We are in the digital era more than any time in the history. Against the backdrop of the vast internet, unthinkable amount of digital data are being generated, transmitted, received, processed, displayed and stored everyday for applications touching virtually every part of our lives, from making a phone call, sharing a photo on a social network to remote baby monitoring. The digital world is so successful because it interacts lively and friendly with the human and the natural world. For example, a finger touch on a screen is sensed and translated for an intuitive interface; a stream of digital bits can be carried by radio wave or light with the shortest time and least bandwidth. A function of paramount importance to the success of the digital world is bridging together the digital world and the inherently analog human/natural world, namely, the analog-to-digital (A/D) and digital-to-analog (D/A) data conversion.

The performance of data converters are advancing in three fronts: speed, resolution and power efficiency. For battery-powered devices like smart phones, the power efficiency is of foremost importance. While users demand more features and functionality from their mobile devices, the battery capacity has seen very limited improvement. In order to prolong or at least keep the battery time, better energy efficiency is required for every part of a device, including the ubiquitous data converter. The power efficiency is even more decisive in applications where the power comes from the environment. For example, in some Internet-of-things (IoTs) hardware nodes the power is harnessed from radio waves.

One of the focuses of Prof. Pun's research group is improving the power efficiency of A/D converters. Three main types of A/D converters are being investigated: successive-approximation (SA), pipelined, and Delta-sigma modulator (DSM) - based. For the SA converter, the group has developed the world's most power-efficient technique [1] (Fig.1a) for its capacitive D/A converter, which is often its most power consuming block. For the pipelined A/D converter, the group has investigated a new school of circuits using stacked comparators and comparator-based buffering [2] (Fig.1b). For DSM-based converters, we, together with our collaborator at the Columbia University, have pioneered works in ultra-low voltage continuous-time converter circuits [3].

Looking ahead, we are searching for fundamentally different and better ways of realizing the converter functions in modern nano-scale CMOS technologies, with the aim of improving the converter's power efficiency for a more user-friendly and greener mobile digital world.



(a) (b)

Fig. 1. Chip photos of (a) an energy efficient SA converter [1] and (b) a pipelined converter [2].

[1] L. Sun, A. Wong, B. Li, W.T. Ng and K.P. Pun, “A charge recycling SAR ADC with a LSB-down switching scheme,” in press, IEEE Transactions on Circuits and Systems – I: Regular Papers, vol. 62, no. 2, p.p. 356-365, Feb. 2015.

[2] X. Tang, C.-T. Ko, and K.P. Pun, "A charge-pump and comparator based power-efficient pipelined ADC technique," Microelectronics Journal, vol. 43, no. 3, pp. 182-188, Mar. 2012.

[3] K.P. Pun, S. Chatterjee, and P. R. Kinget, "A 0.5-V 74-dB SNDR 25-kHz continuous-time delta-sigma modulator with a return-to-open DAC," IEEE Journal of Solid-State Circuits, vol. 42, no. 3, pp. 496-507, Mar. 2007.