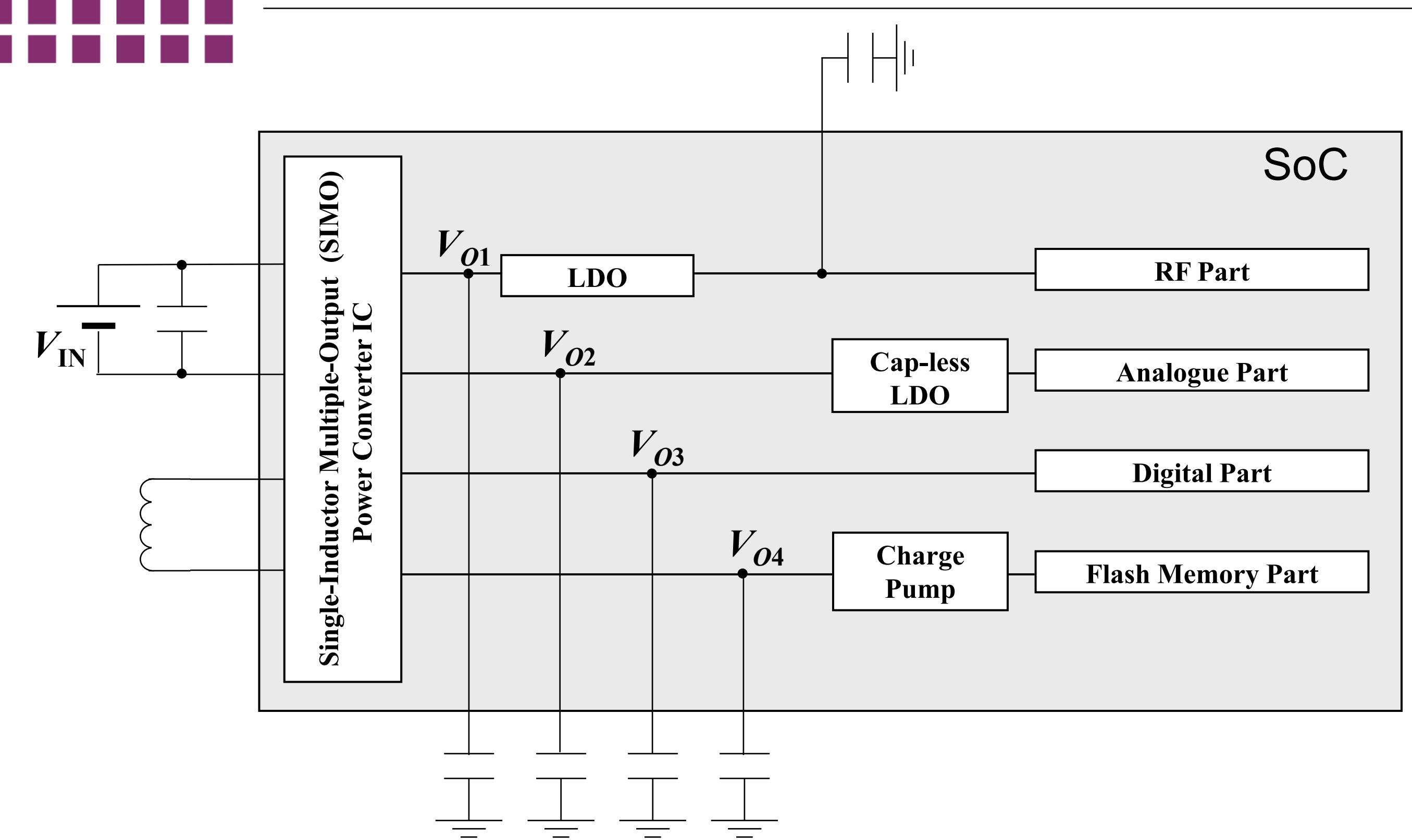




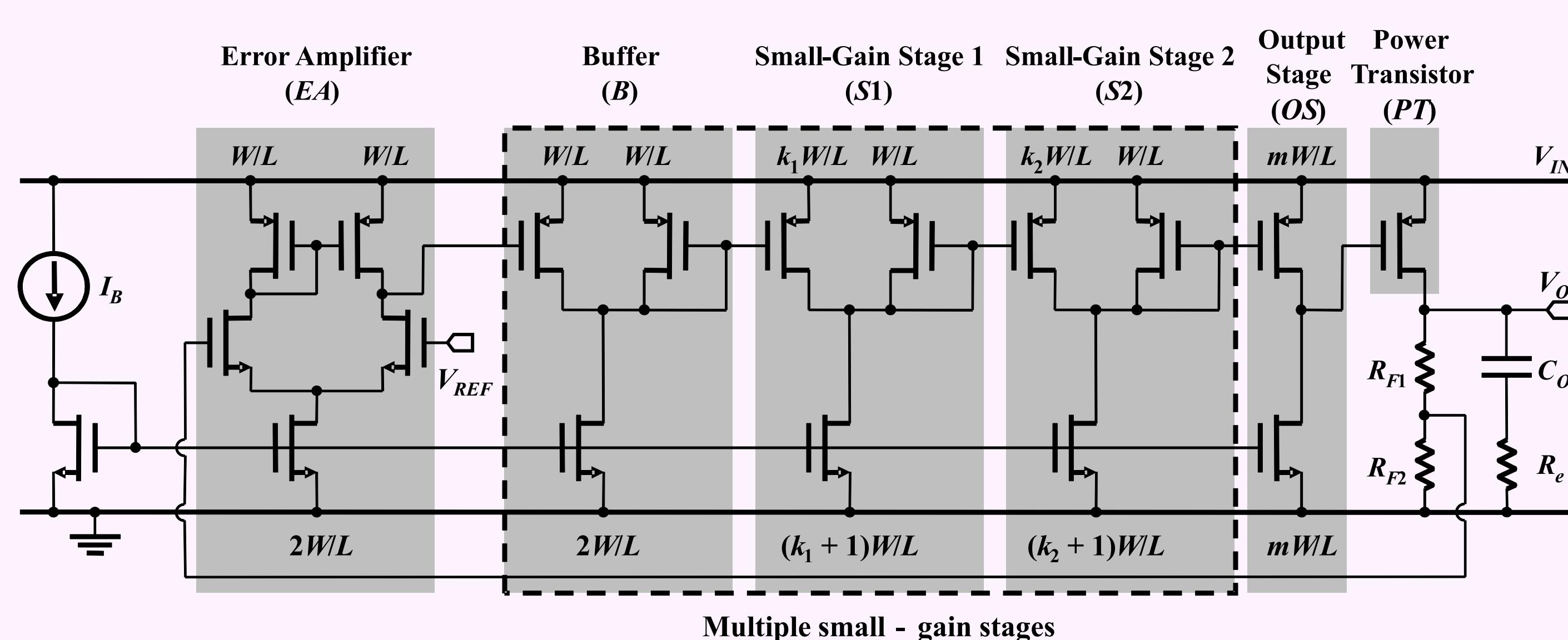
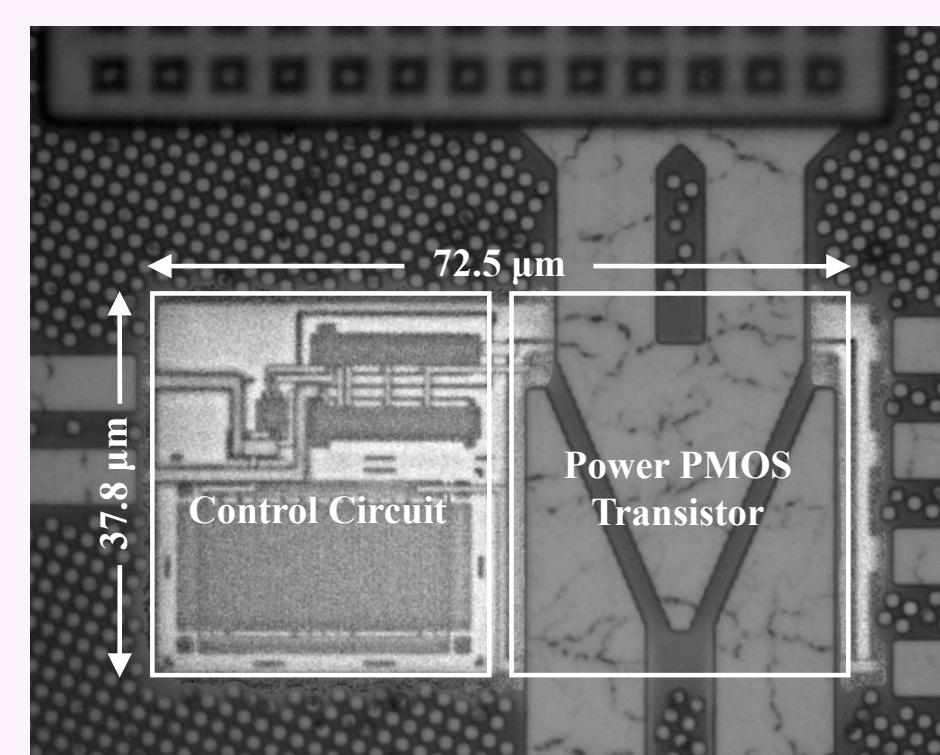
Main Stream Research Projects

- Fast-transient low-dropout regulators (LDOs)
- Output capacitor-less low-dropout regulators (LDOs)
- Single-inductor multiple-output (SIMO) switched-mode DC-DC converters
- High-efficiency charge pumps



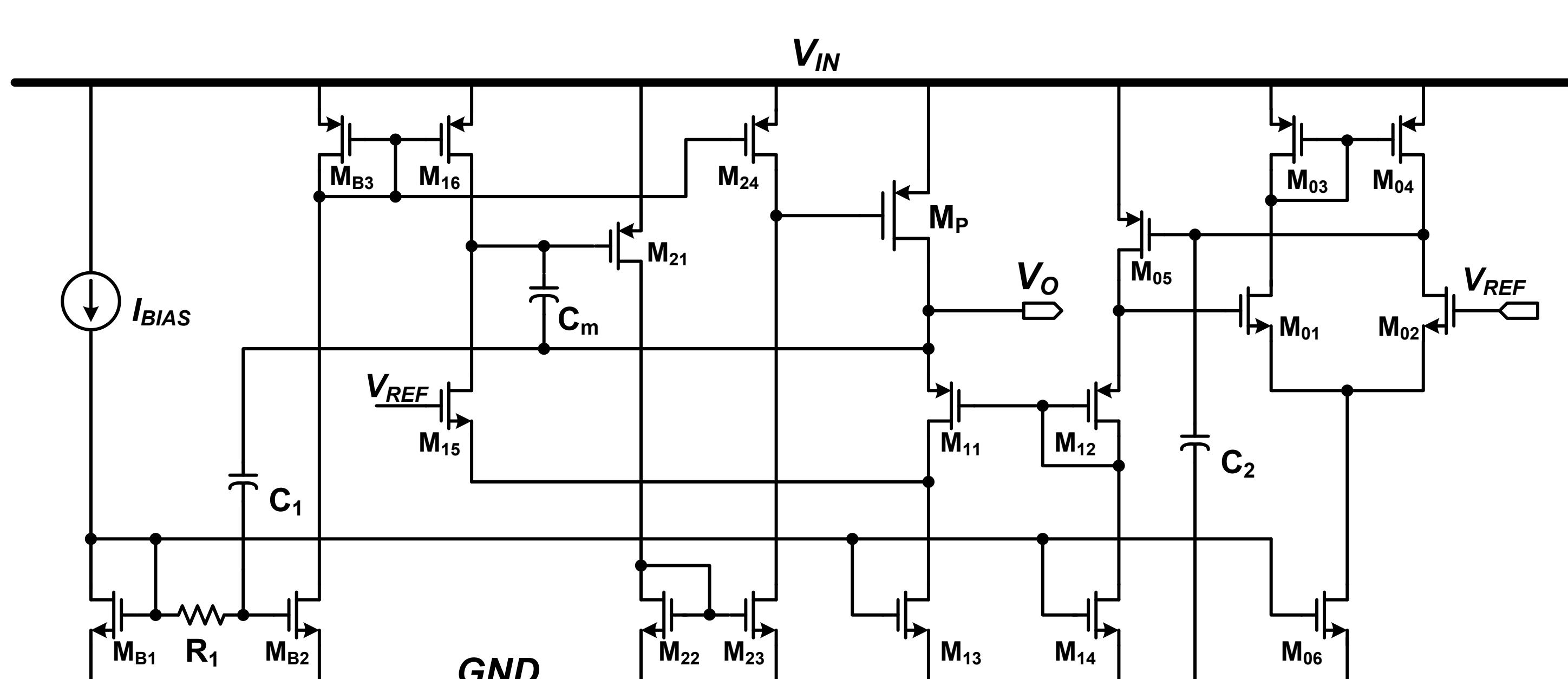
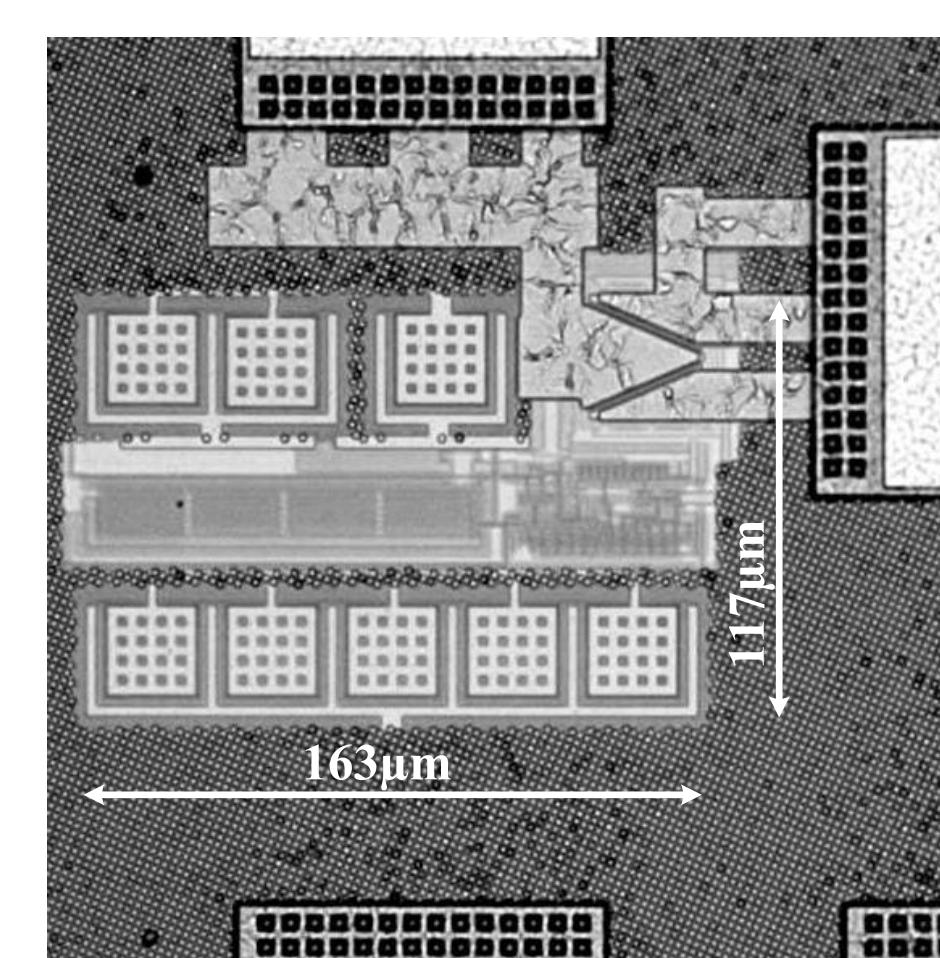
Fast-transient low-dropout regulators (LDOs)

- Loop-bandwidth enhancement
- Loop-gain enhancement
- Channel-resistance-insensitive small-gain-stage
- No on-chip compensation capacitor
- 9.3 μ A quiescent current



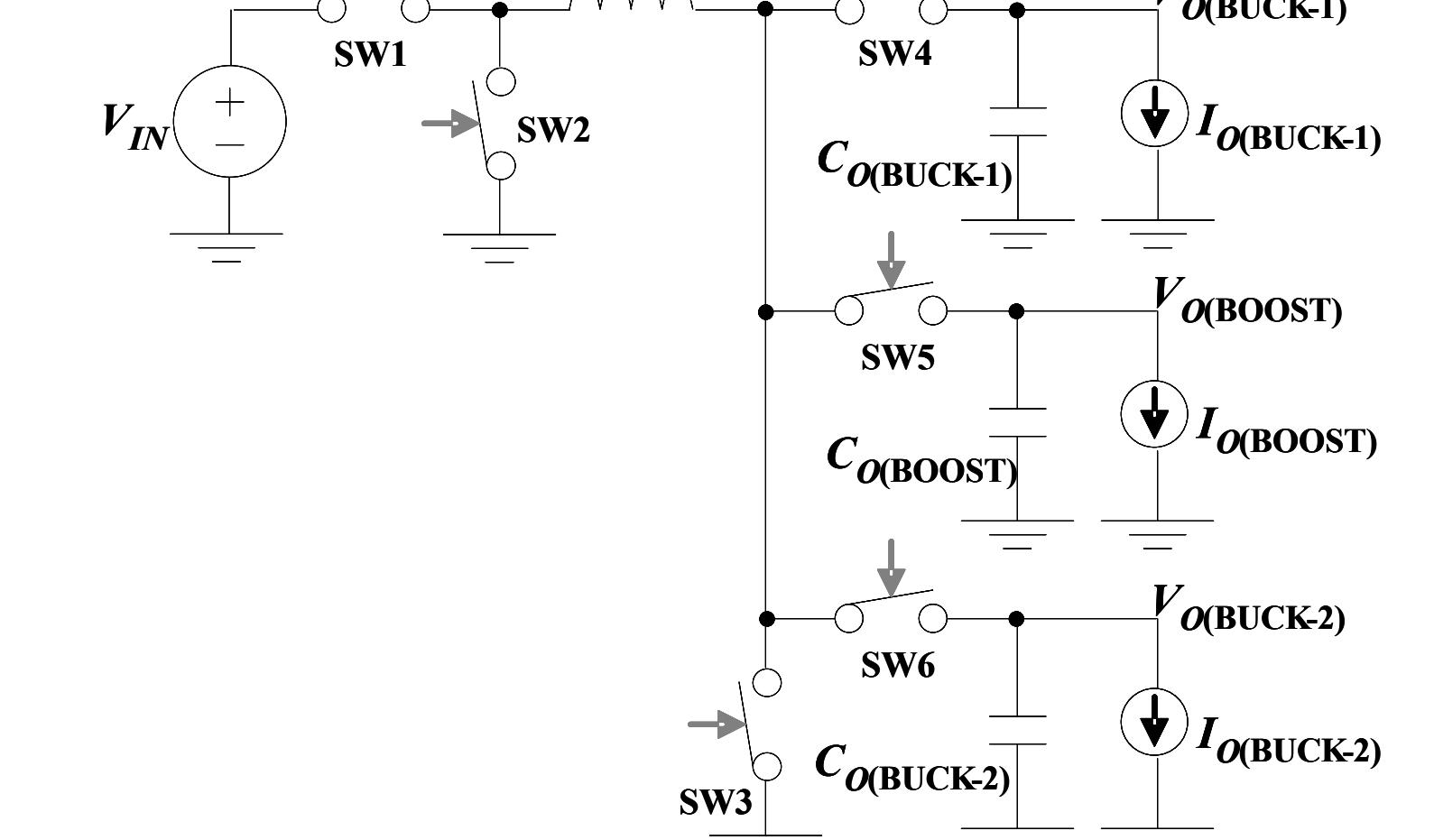
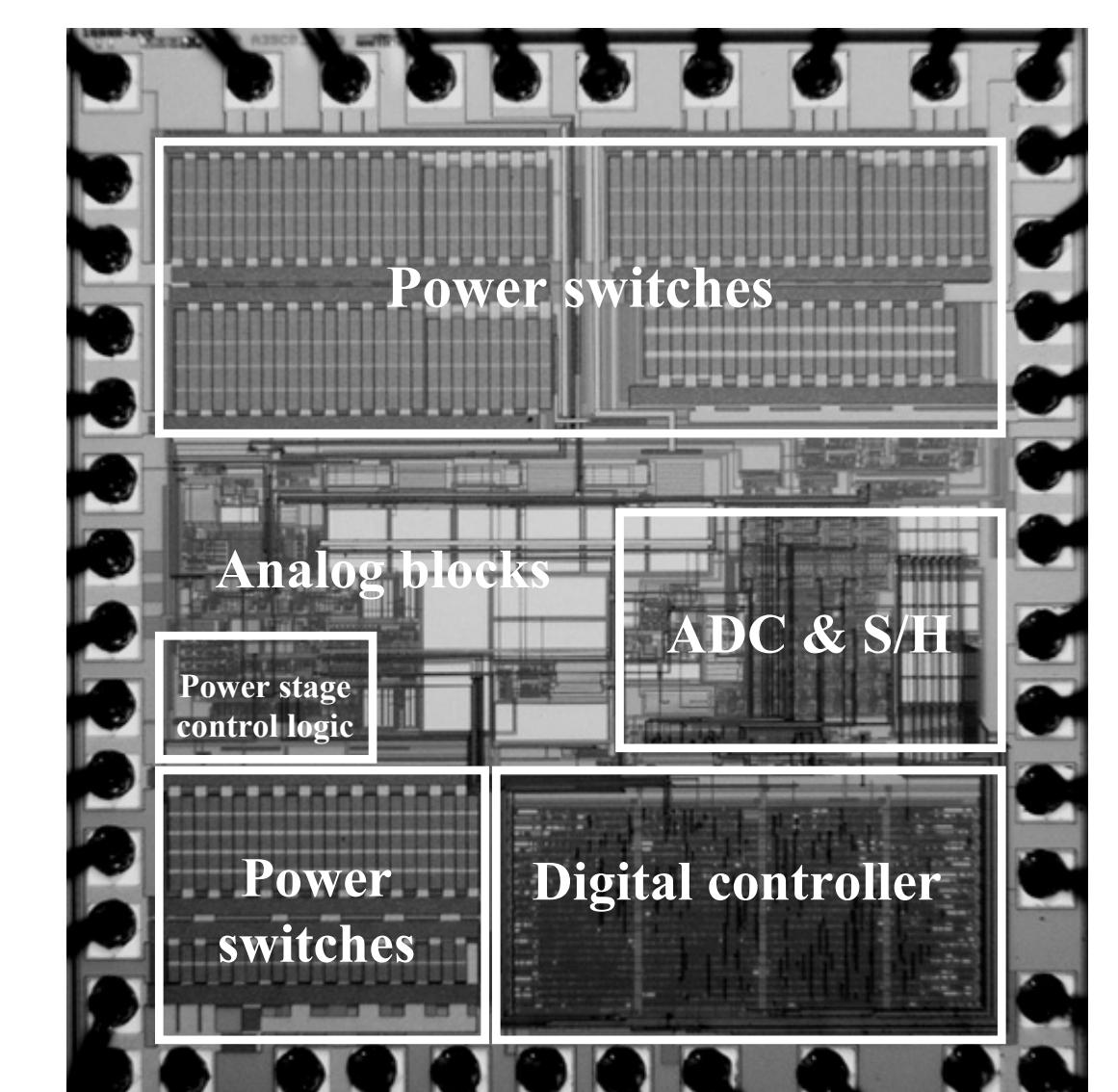
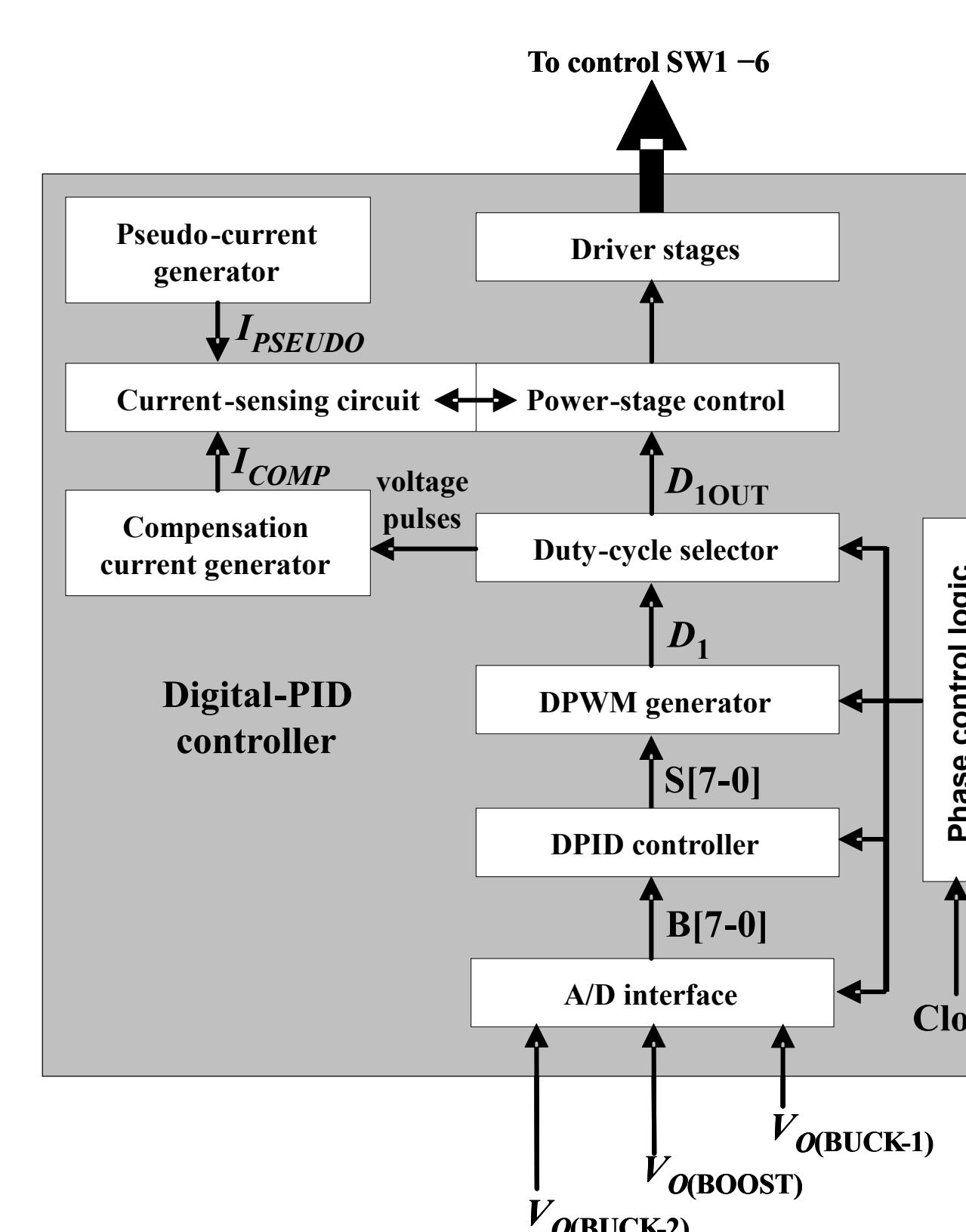
Output capacitor-less low-dropout regulators (LDOs)

- Single compensation capacitor for two-stage voltage flipped follower
- Dynamic biasing for slew rate enhancement
- Stable for capacitive load from 0 to 50 pF
- 100 mA load capability
- 6 μ W under a 0.75V supply



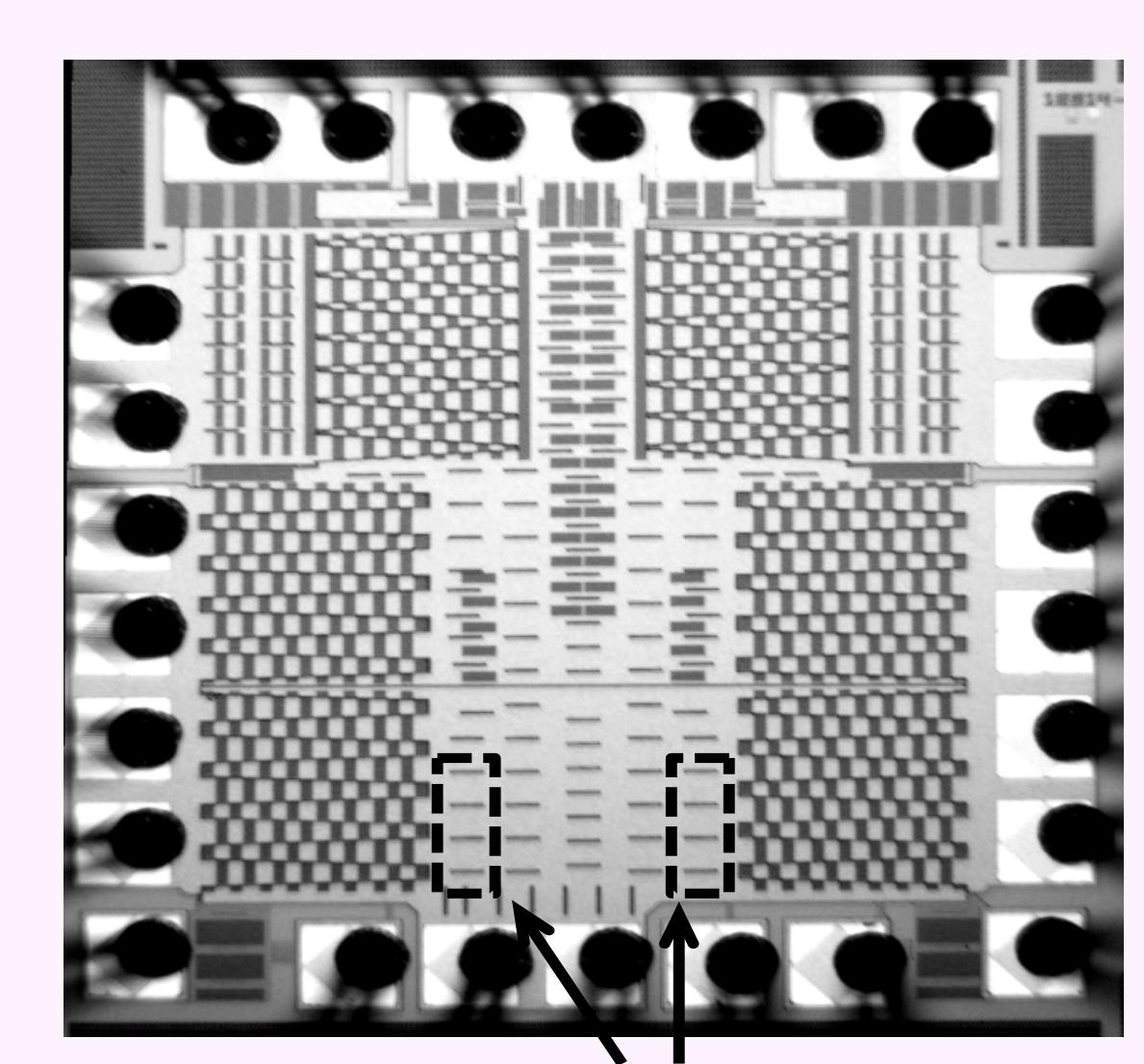
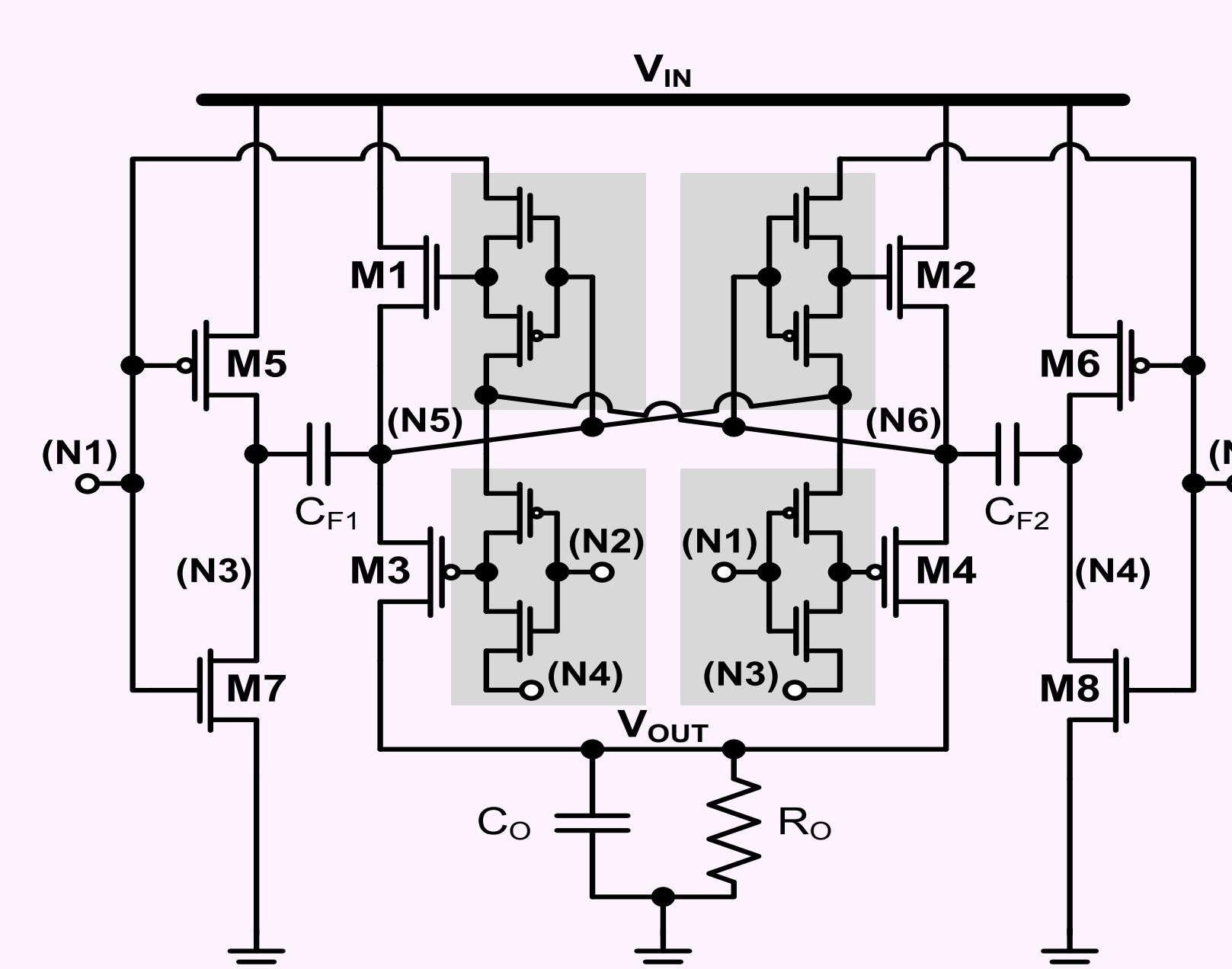
Single-inductor multiple-output (SIMO) switched-mode DC-DC converters

- Single-inductor triple-output
- 83.5% power efficiency
- Proposed pre-sub-period inductor-current control
- Two buck subconverters and one boost subconverter configurable



High-efficiency charge pumps

- No reversion loss using first-level gate-control
- Supports 0.8V Minimum voltage
- Higher than 90% power efficiency
- No area-consuming resistors or extra power MOSFETs and buffers required



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- J. P. Guo and K. N. Leung, "A 6-uW Chip-Area-Efficient Output-Capacitorless LDO in 90-nm CMOS Technology," *IEEE Journal of Solid-State Circuits*, Vol. 45, No. 9, pp. 1896-1905, Sept. 2010.
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