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Capture-power-aware test data compression using selective encoding

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ABSTRACT

Ever-increasing test data volume and excessive test power are two of the main concerns of VLSI testing. The "don't-care" bits (also known as X-bits) in given test cube can be exploited for test data compression and/or test power reduction, and these techniques may contradict to each other because the very same X-bits are likely to be used for different optimization objectives. This paper proposes a capture-power-aware test compression scheme that is able to keep capture-power under a safe limit with low test compression ratio loss. Experimental results on benchmark circuits validate the effectiveness of the proposed solution.

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1. Introduction

The test data volume for today's very large scale integrated (VLSI) circuits has been exploding with the ever-increasing integration capability of semiconductor technology [1]. In addition, besides the test vectors targeting traditional stuck-at faults, test patterns targeting delay faults and many other subtle faults are becoming essential to improve test quality for deep submicron designs. Large test data volume not only raises memory depth requirements for the automatic test equipment (ATE), but also prolongs ICs' testing time, thus significantly increasing test cost. To address this issue, various test compression techniques [2–24] have been proposed in the literature [25], and most of them exploited the "don't-care" bits (also known as X-bits) in given test cubes for effective test compression.[1] Generally speaking, the more X-bits in test cubes, the higher the test compression ratio can be achieved.

At the same time, power dissipation during scan-based testing of VLSI circuits can be significantly higher than that during normal operation [26]. Elevated average test power, dominated by scan shift-power may cause structural damage to the circuit under test (CUT); while excessive peak test power in the capture phase is likely to cause good circuit to fail test, thus leading to unnecessary yield loss [27]. There is a rich literature on reducing test power in shift mode, in which design-for-testability (DfT) based methods such as scan chain partitioning technique [28–33] are very effective (when compared to X-filling techniques such as [34]). Compared to shift-power, yield loss caused by excessive capture-power has become a more serious concern with technology scaling. There are, however, no such effective DfT-based techniques for capture-power reduction, and we mainly resort to X-filling techniques (e.g., [35–39]) to reduce the excessive capture-power in scan-based testing.

There is usually a significant percentage of X-bits in given test cubes (typically more than 95% [25]). With these X-bits, prior works either target test data compression only (e.g., [2–24]) or try to reduce shift- and/or capture-power only (e.g., [35–39]). This is unfortunate because both problems are addressed using the very same X-bits and hence they may contradict with each other.

As large test data volume and high capture-power are both major concerns for the industry today, it is essential to develop a holistic solution that can restrict the capture-power when using test compression scheme, which motivates this work.

To address the above issues, in this paper, we propose a novel capture-power-aware test compression scheme. One nonlinear code-based test compression framework: *selective encoding* [12] is selected as the base test compression scheme and the proposed X-filling technique is integrated into this architecture for capture-power reduction. With the proposed technique, the capture-power of given test cubes can be kept under the safe limit after X-filling, with little or no loss of compression ratio, as demonstrated in our experimental results on ISCAS'89 and ITC'99 benchmark circuits.

The remainder of this paper is organized as follows. Section 2 gives the preliminaries and motivates this work. The proposed

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[1] A test cube is a deterministic test vector in which the bits that test generation tool does not assign are left as don't-cares.

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capture-power-aware test compression technique is detailed in Section 3. Experimental results on benchmark circuits are presented and analyzed in Section 4. Finally, Section 5 concludes this paper and points out some future works.

2. Preliminaries and motivation

2.1. Test compression using selective encoding

Test data compression is widely used in the industry nowadays. With test compression, the test stimuli is stored in a losslessly compressed form in the ATE and decompressed to the original test set on-chip before being shifted into scan chains. On the other side, lossy-compaction schemes such as multiple-input signature register (MISR) are usually utilized to generate very small signatures for test responses.

A significant amount of research efforts have been conducted in test compression, resulting in a wide variety of techniques in the literature, which can be broadly classified into three categories: (i) nonlinear code-based schemes that use data compression codes to encode test cubes; (ii) linear decompressor-based schemes that decompress the data using linear operations (e.g., XOR network and/or linear feedback shift registers); and (iii) broadcasting-based methods. As pointed out in [25], the above techniques have their own pros and cons: code-based schemes (e.g., [2–12]) can efficiently exploit correlations in the specified bits and do not require ATPG constraints, while linear-decompressor-based techniques and broadcasting-based techniques (e.g., [13–24]) generally provide greater compression ratio.

In this work, we use one code-based test compression scheme, namely *selective encoding*, as the base test compression scheme and we apply our proposed technique for capture-power reduction in this compression environment. It is important to note, while the details of the proposed method is architecture-dependent, *the basic concept can be generalized and applied to other code-based schemes*. Since the selective encoding test compression scheme is well related to our work, we briefly describe it as follows, refer to [12] for details.

As can be observed from Fig. 1, a series of c-bit slice-codes imported from ATE are first decoded into N-bit scan slices[2] before they are fed to the scan chains, where $c=\lceil \log_2(N+1)\rceil+2$ and each slice-code contains 2-bit control-code and $\lceil \log_2(N+1)\rceil$-bit data-code. The N-bit scan slices are encoded into one or more c-bit slice-codes as follows:

To start coding a scan slice, the first control-code bit is set to be "0" and the second control-code bit indicates the "*default value*" for this scan slice, which is determined by comparing the numbers of 0- and 1-valued bits in the test stimuli: the default value will be "1" if there are more "1"s than "0"s in one scan slice; otherwise the default value is set to be "0".

As shown in Table 1, if the scan slice contains only one care-bit that has different logic value with the default value, the X-bits will be mapped to be the default value and the scan slice is encoded into one c-bit slice-code. If, however, the scan slice contains more care-bits that are different from the default value, the N-bit slice is divided into $\lceil N/K\rceil$ groups ($K=\lceil \log_2(N+1)\rceil$) and additional codes need to be introduced to encode the scan slice. For those groups wherein all bits are default values, we do not need to encode them. Otherwise, if a group contains one care-bit that is different from the default value, it can be encoded with the "single-bit-mode"; for the groups containing multiple care-bits

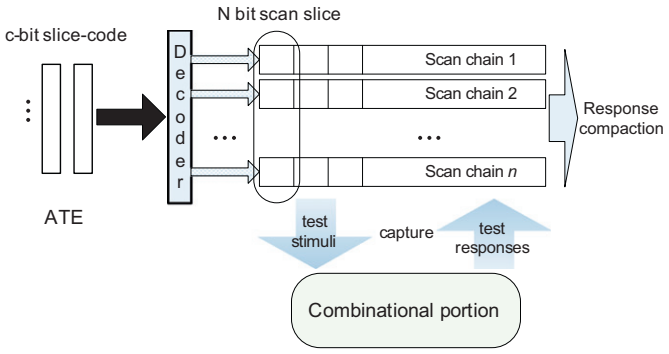

Fig. 1. Test compression using Selective Encoding [12].

Table 1
A Selective Encoding example.

Slice	Slice code		Description
	Control-code	Data-code	
X01X X0XX	00	0010	Start a new slice, default value: "0", set bit 2 to "1"
100X 0111	01	0100	Start a new slice, default value: "1", set bit 4 to "0"
	11	0000	Enter group-copy-mode, starting from bit "0"
	11	100X	The data is 100X

that are different from the default value, the so-called "group-copy-mode" is introduced, two or more codes are needed to encode this group (X-bits in this group can be mapped to any value in this case, see the encoding for scan slice "100X 0111" in Table 1).

The information contained in the data-code part is different according to different status of the control-codes: In the "single-bit-mode"(in the first slice-code for each scan slice, or in the following slice-codes whose second control-bits are set to "0"), the data-code part denotes the index of the care-bit that is different from the default value; Otherwise, in the "group-copy-mode"(when the second control-bits are set to "1" in slice-codes following the first code for each scan slice), wherein the data-code of the first slice-code represents the index of this group's first bit and the second slice-code gives the copy of this group. To further improve test compression ratio, adjacent groups can be merged into a *group-subslice* so that they can share the index code of the first group.

2.2. X-filling for test power reduction

Scan tests can increase the ICs' switching activities well beyond that of its normal operation. It is possible that the test power consumption exceeds the circuit's power rating in both shift and capture mode, and lots of research work has been dedicated to this area [26]. Within these techniques, X-filling techniques are introduced to manipulate X-bits in test patterns for shift-power or/and capture-power reduction (e.g., *Adjacent fill* [34], *Preferred fill* [35], *iFill* [39]), while DfT modification techniques [28–33] are presented to modify scan testing hardware for the same purpose. The DfT modification techniques are more efficient on shift-power reduction, on the other hand, effective capture-power reduction is usually resorted to X-filling techniques. Therefore, in this work, the shift-power issues are

[2] A scan slice is the set of test data applied to the scan chain inputs at a scan cycle.

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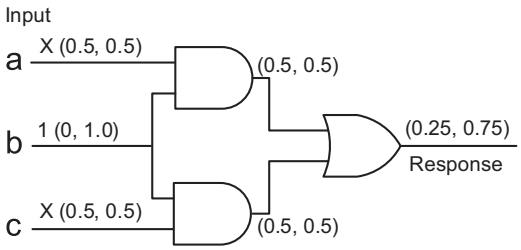

Fig. 2. Signal probability calculation for circuit nodes.

assumed to be handled with the DfT-based techniques, and capture-power is mainly considered during test compression in order to avoid test yield loss.

Prior works for capture-power reduction can be evaluated in two metrics: the effectiveness of capture-power reduction and the computational complexity. Wen et al. [36] firstly proposed to achieve low capture-power by filling the X-bits in the test stimuli to be the same as the known test responses as much as possible. The main limitation of that work is its high computational time, because the X-bits are filled incrementally and the time-consuming forward implications and backward justifications are extensively used. In [35], Remersaro et al. developed an efficient probability-based X-filling technique, namely *Preferred fill*, which tries to fill all X-bits in the test cube in one step, instead of using incremental fill and logic simulation. Signal probability of each circuit node can be calculated with the given initial scan slice and response probabilities calculation. As shown in Fig. 2, the input signals a, b and c are with logic values of X, 1 and X, respectively. Therefore, the probability of a, b and c to be logic "0" or "1" are (0.5, 0.5), (0, 1.0) and (0.5, 0.5), respectively. Correspondingly, the response is with the probability of (0.25, 0.75) in this circuit structure. With the information of response probabilities, we can calculate the transition probability for each scan cell as $P_1(s) \times P_0(r) + P_0(s) \times P_1(r)$, where $P_{1/0}(s/r)$ is the probability to have "1/0" as the logic value of test stimulus/response in this scan cell. Their technique, however, is inherently less effective as the available information for the probability calculation in their single-step filling is quite limited.

The above works try to reduce capture-power consumption as much as possible. This is however unnecessary because the correct operation of the circuits can be guaranteed as long as the peak capture-power does not exceed a certain threshold.

2.3. Motivation

As demonstrated in the previous subsections, since both test data compression and X-filling techniques for test power reduction need to utilize the very same X-bits in the given test cubes, to obtain both low test data volume and low test power simultaneously, it is important to develop a holistic solution that takes both problems into consideration [40–42]. As demonstrated in the prior subsection, X-filling techniques are usually adopted and are more efficient for capture-power reduction, and code-based test compression can exploit the X-bits for test compression more effectively and will bring no constraints to the ATPG progress; this paper focuses on capture-power-aware code-based compression with X-bits in given test cubes, and we use Selective Encoding as one example of code-based test compression schemes.

As can be observed in the example shown in Fig. 3, the scan slices in this figure are similar to those in Fig. 1, and the signal probabilities of test response bits can be obtained by calculating from the signal probabilities of test stimulus bits as in Fig. 2. There are two possible situations when capture-power can be

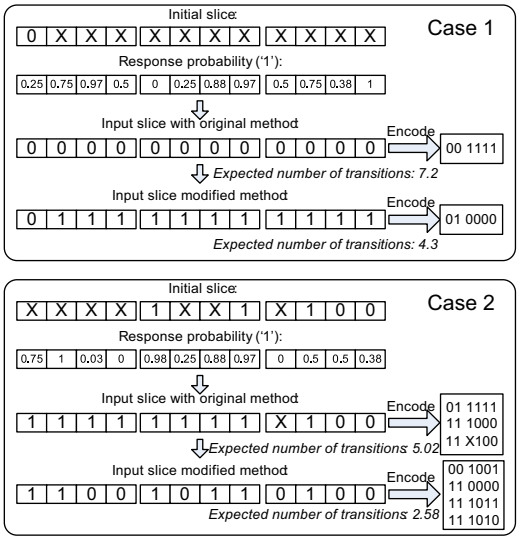

Fig. 3. Motivational example.

reduced with little or no compression ratio loss: in Case 1, with the original Selective Encoding scheme in [12], the scan slice will be filled as "0000 0000 0000" and encoded with one slice-code, then the expected number of transitions (i.e., the sum of all scan cells' transition probabilities) will be 7.2. If, however, we fill this slice as "0111 1111 1111", it can be also encoded with one single slice-code, but the expected number of transitions will be reduced to 4.3 in this case; consider another example scan slice with more care bits in Case 2, it will be filled as "1111 1111 X100" as the original Selective Encoding scheme in [12], which results in 5.02 expected transitions. Suppose we fill this slice to be "1100 1011 0100", the expected number of transitions can be dropped to 2.58, with only one more slice-code needed to encode this scan slice.

From the above example, we can see that X-filling decisions for the scan slices to be encoded have a large impact on both test compression ratio and capture-power consumption. With an effective X-filling strategy, we can reduce the capture-power significantly without much loss of compression ratio. At the same time, because it is not necessary to reduce the capture-power as much as possible, we can put more emphasis on test compressing when utilizing X-bits if the capture-power is under the safety limit. Therefore, the work studied in this paper tries to utilize the X-bits efficiently for capture-power reduction with minor impact on test compression ratio.

3. Proposed methodology

For a particular X-bit, its impact on test compression ratio can be easily obtained by checking whether we need more slice-codes to encode the scan slice after filling it, while its impact on capture-power can be estimated by the expected number of transitions in the test vector after filling it. Based on the above, we try to reduce the capture-power under the safe limit while keeping the compression ratio as high as possible.

The flowchart of the proposed algorithm is shown in Fig. 4. In the original selective encoding compression scheme, the default value for each scan slice is only decided by the counts of "1"s and "0"s without considering their locations in the test pattern, which may have a high impact on capture-power.

Therefore, in our procedure, we propose to choose a better default value considering both capture-power and compression ratio. Next, if filling X-bits with the default value selected by the proposed method cannot keep the capture-power under the

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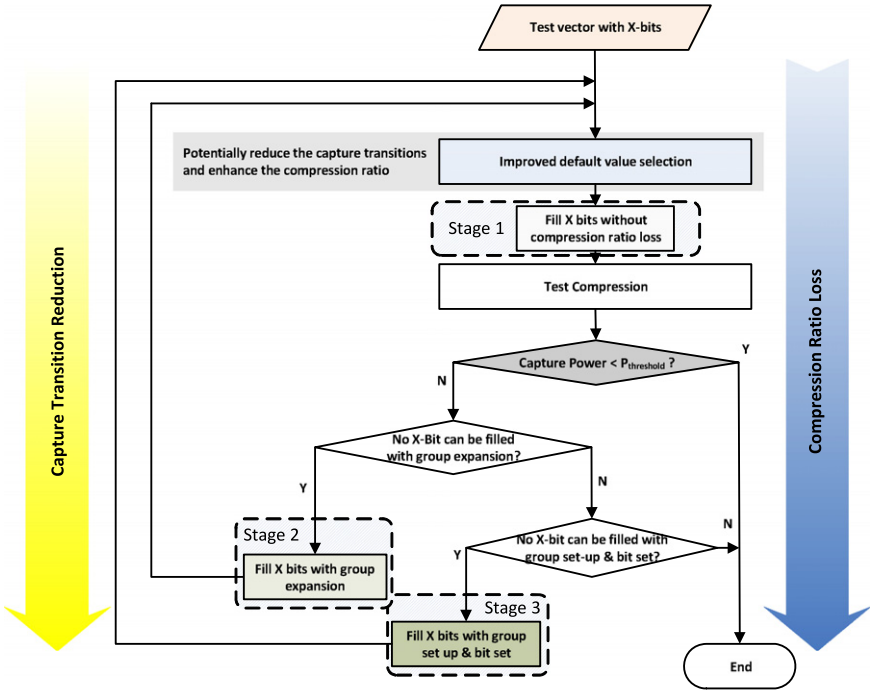

Fig. 4. Capture-power-aware test data compression flow.

safety limit, three more stages are needed to further cut down the capture transitions with no or little compression ratio loss: (1) Stage 1 tries to fill X-bits to reduce capture-power without test compression ratio loss; (2) if we cannot reduce the capture-power under the given safe limit with the above step, Stage 2 is performed at the cost of slight compression ratio loss, taking advantage of the group-subslice feature in [12]. (3) Finally, if the capture-power is still beyond the threshold, in Stage 3, more X-bits in the scan slice need to be filled by setting up new groups or setting bits with different logic values from the default value, resulting in lower test compression ratio. The above procedure is iterative, i.e., after Stage 3, Stages 1 and 2 will be conducted again to further reduce capture-power with less test compression ratio loss. The iterations are also helpful for the accuracy of capture-power estimation because we have more confidence for the probabilities of the responses once the values of more X-bits are determined. After every pass of X-filling, the remaining X-bits in the scan slice will be encoded with the method in [12], and the capture-power is checked to see if it violates the safety limit. The details of this flow will be discussed in detail in the following subsections.

3.1. *Improved default value decision for scan slices*

As illustrated in Section 2.1, [12] determines the default value merely by comparing the number of 0- and 1-valued bits in test stimuli. Such method, however, may cause large amount of capture transitions. As shown in the example in Fig. 5, wherein the scan slice contains eight bits and one bit is "0" while all others are X-bits. The original test compression scheme will set the default value to be "0" and fill all the X-bits with "0". With the probabilities for the test responses (calculated as in Fig. 2) as shown in the figure, the above default value "0" will cause at least five transitions in the capture cycle, which is quite high.

Moreover, the original compression scheme chooses the default value for each scan slice only based on the numbers of the care-bits, not their locations. However, when utilizing

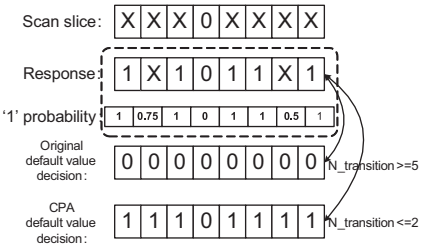

Fig. 5. Default value decision example.

"group-copy-mode", what affects the compression ratio is the number of "groups" need to be encoded, instead of the number of care-bits having different logic value from the default value. Hence if the default value is selected considering the locations of these care-bits, we can reduce the number of "groups" need to be encoded, thus enhancing compression ratio. Meanwhile, all the to-be-encoded X-bits in the "groups" can be filled for capture-power reduction freely. Since in the "group-copy-mode", care-bits are encoded in the unit of "group"s (whose length equals to the length of the data-code part), the default value for each scan slice should consider care-bits' appearance in each group.

From the above discussion, we can conclude that, when deciding default value, we need to take both response signal probabilities, logic-value of care-bits and their locations into account to achieve effective solutions.

To take the probabilities of response bits into account, we define a *probability threshold* P_{th} and we say a X-bit in the test responses is "*likely to be*" value "1"/"0" when its 1- or 0-probability is higher than P_{th}. For each "group", it is cataloged based on the number of "1"/"0"s in it, if it contains more "1"s (care-bits have the logic value "1" or X-bits are likely to be "1"), it is "O" (one) group, otherwise, it is "Z" (zero) group.

When deciding default value of the scan slice, first, we count numbers of the "O" and "Z" groups, if there are more "O" groups, "1" is chosen to be the default value, and vice versa. Next, if the

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number of "O" and "Z" groups are equal, we will use the logic value more care-bits and X-bits likely to be as the default value.

There are two groups in the example shown in Fig. 5. Suppose P_{th}=0.9, according to the signal probabilities of the test responses and the care-bits in the scan slice, we can find that they are both "O" groups, so the default value of this scan slice should be selected as "1", and the number of capture transitions will be no more than two with this default value, which is much lower than with the original default value.

3.2. X-filling for capture-power reduction without compression ratio loss

In Stage 1, capture-power can be reduced by filling X-bits without introducing any extra compression codes. The algorithm is shown in Fig. 6.

In each iteration, signal probabilities of the response bits are calculated first (line 3). Two types of X-bits can be filled in Stage 1: (1) X-bits with corresponding response bits that are "likely to have" the same value as the default value x_d (lines 4–5) and (2) X-bits that are kept intact in group-copy-mode during the encoding process, and they are filled as the logic value they are "likely to be" (lines 6–7). During each iteration, with more X-bits in the stimuli determined, it is expected that more test response bits are deduced to be "likely to have" "1"/"1", which enables us to fill more X-bits in the following iteration. Capture transitions are reduced in every iteration and the procedure ends when capture transitions are reduced to be less than the threshold value or no X-bits conforming to the filling rule in this stage exists.

The above X-filling process does not introduce any extra codes during the encoding process, as can be shown in the example in Fig. 7. For a scan slice {XXXX 011X 11X0 001}, wherein {011X 11X0} is to be coded in group-copy-mode, with both the encoding scheme in [12] and the proposed method, this scan slice will be encoded with four codes. Because the capture transitions are reduced in each iteration, our method achieves a much lower capture-power consumption without compression ratio loss.

Stage 1: X-filling without compression ratio loss

INPUT: $S = \{s_i\}$: Scan slices
OUTPUT: $S' = \{s'_i\}$: Scan slices with more filled x-bits

```
1.  while (more X-bit can be filled under the stage rule) {
2.    for each scan slice, s_i, {
3.      Compute the circuit's response, R_i;
4.      Search the bits in R_i that are "likely to have" default value x_d;
5.      Fill the corresponding bits in s_i with x_d to get s'_i;
6.      Search the X-bits in R_i in group-copy-mode;
7.      Fill the X-bits in group-subslices to get s'_i;
8.    }
9.  }
10. if (capture-power, CP_i ≤ threshold T_th) {
11.   Go to the end;
12. }
13. else Go to Stage 2;
```

Fig. 6. Procedure for X-filling without compression ratio loss.

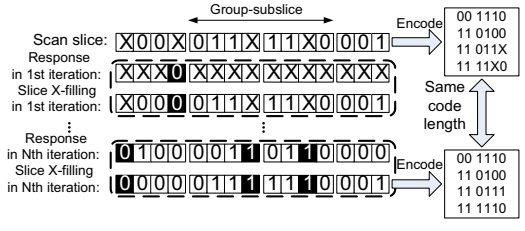

Fig. 7. X-filling without compression ratio loss.

Stage 2: X-filling with group expansion

INPUT: $S = \{s_i\}$: Scan slices
OUTPUT: $S' = \{s'_i\}$: Scan slices with expanded groups

```
1.  Initialize transition reduction expectation N_m;
2.  while (N_m >= 2) {
3.    for each scan slice, s_i {
4.      Calculate reduced transition in adjacent group N_ra;
5.      if (N_ra>=N_m){
6.          Expand current group-subslice with the group;
7.          Search the bits in R_i "likely to have" '0' or '1';
8.          Fill corresponding X-bits in new merged group to get s'_i ;
9.      }
10.   }
11.   Repeat the process of Stage 1;
12.   if (capture-power, CP_i ≤ threshold T_th) {
13.     Go to the end;
14.   }
15.   N_m = N_m − a, 1 <= a <= N_group;
16. }
```

Fig. 8. Procedure for X-filling with group expansion.

3.3. X-filling for capture-power reduction with compression ratio loss

3.3.1. X-filling for capture-power reduction with group expansion

If the capture-power cannot meet the constraint after filling X-bits in Stage 1, we have to tradeoff some compression ratio for further capture-power reduction.

One observation from the Selective Encoding scheme in [12] is that, when the *group-subslice* feature is utilized, we are able to expand a group to one of its neighbors (namely *group expansion*) and have ($N_{group}-N_{care\text{-}bits}$) free X-bits ($N_{group}$ and $N_{care\text{-}bits}$ are the number of bits in one group and the number of care-bits in this group, respectively) to fill by introducing only one additional code (the code indicates the *group-subslice* index can be shared with its neighboring group, and it may need to be modified).

Therefore we can fill the groups containing more X-bits "likely to be" logic value different from the default value, by expanding one existing group to reduce capture transitions with one additional code word. It can achieve more capture transitions reduction than filling one single X-bit with "single-bit-mode", which will also introduce one more code. Moreover, such strategy can also save the encoded code length compared to setting up a new group, which will cause two additional codes.

Fig. 8 shows the procedure of this stage inspired by the above observation. First, a group is selected to be expanded to its neighboring group-subslice, if this operation results in high capture transitions. With N_{group} bits in each group, we first initialize a so-called *transition reduction expectation* value as N_m[3] (line 1). If the expansion of a group can reduce more capture transitions than N_m, this group will be expanded and X-bits in this group are filled according to their corresponding test responses

[3] Since the maximum capture transition reduction that can be achieved with the group expansion technique is N_{group}, we typically initialize N_m=N_{group}.

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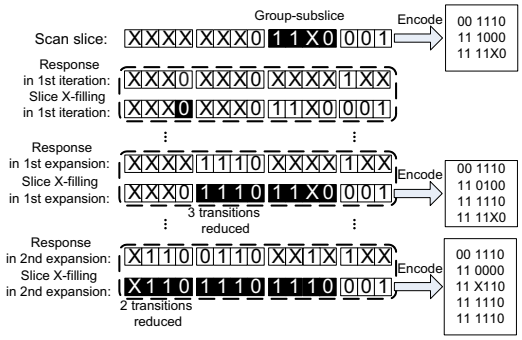

Fig. 9. X-filling with group expansion.

(lines 5–9). Since more X-bits have been determined and it is possible to be able to further reduce capture-power without test compression loss, Stage 1 should be conducted again. If no group in the test vector can be filled with the current N_m, N_m will be reduced by $a, 1 < a < N_{group}$ (higher a can reduce the number of iterations). Stage 2 terminates when capture transitions are under the safety limit or $N_m < 2$. In this stage, a large amount of X-bits can be exploited for capture-power reduction with little compression ratio loss.

The effectiveness of Stage 2 can be illustrated by the example shown in Fig. 9. After filling X-bits without compression ratio loss in Stage 1, the test responses will be updated as shown in "Response in the 1st pass of expansion", we can find that three capture transitions can be eliminated if the group "11X0" is expanded to its left neighboring group, and expanding this group will bring one more code word. After this expansion, more X-bits in test responses may turn into care-bits or have higher signal probability than P_{th} in their corresponding test response bits, therefore Stage 1 is conducted again to reduce the capture transitions without compression ratio loss. After this iteration, another group "X110" can be expanded from its right neighboring group once more, two more transitions can be reduced at the cost of one additional code in this expansion. This expansion can be continued until the capture-power constraint is meet or there is no more neighboring group to be expanded.

Since one iteration containing both Stages 1 and 2 is conducted after all groups containing $N_{ra} \geq N_m$ capture transition reduction are filled, and the capture-power will be checked once in each iteration to see if it is already under the safety limit, if not, another iteration should be conducted to further reduce the capture transitions.

3.3.2. *X-filling for capture-power reduction with group set-up and bit set*

If capture-power of the test vector is still higher than the safety limit after Stage 2, we have no other choice but to set up new groups or fill single X-bits for further capture transition reduction with more test compression ratio loss. According to [12], at least two additional codes are necessary to encode a new group. One of them is for the index and the other is for the data of the group to be set up. The group set-up can be efficient as long as the new group contains more than 2 bits "likely to be" logic value different from the default value, otherwise, we can just fill one X-bit with one additional code word. Note that, if there is already a group-subslice in the scan slice, one more code in single-bit-mode is required to differentiate from the two subslices.

The procedure for reducing capture-power with higher compression ratio loss in Stage 3 is shown in Fig. 10, which mainly consists of two parts: group set-up and bit set. In the part of group set-up, similar to Stage 2, the expected transition reduction is

Stage 3: X-filling with group set up & bit set

INPUT: $S = \{s_i\}$: Scan slices
OUTPUT: $S' = \{s_i'\}$: Scan slices with new groups

```
1.  Initialize transition reduction expectation N_m;
2.  while (N_m >= 2) {
3.   for each scan slice, s_i {
4.    Calculate transition reduction of each group in this slice: N_ng;
5.    if (N_ng >= N_m) {
6.       Search the bits in R_i "likely to have" '0' or '1' in this group;
7.       Fill corresponding X-bits in new set up group to get s_i';
8.    }
9.   }
10.  Repeat the process of Stage 1;
11.  if (capture-power, CP_i ≤ threshold T_th) {
12.   Go to the end;
13.  }
14.  Repeat the process of Stage 2;
15.  if (capture-power, CP_i ≤ threshold T_th) {
16.   Go to the end;
17.  }
18.  N_m = N_m − a, 1 <= a <= N_group;
19. }
20. while (There is X-bits in the test cube) {
21.  Search the bits in R_i "likely to have" '0' or '1';
22.  Fill corresponding X-bit to get s_i';
23.  Repeat the process of Stage 1;
24.  if (capture-power, CP_i ≤ threshold T_th) {
25.    Go to the end;
26.  }
27.  Repeat the process of Stage 2;
28.  if (capture-power, CP_i ≤ threshold T_th) {
29.    Go to the end;
30.  }
31. }
```

Fig. 10. Procedure for X-filling with group set-up and bit set.

initialized as $N_m = N_{group}$ in the beginning (line 1), and the part of setting up new groups will end when the expected capture transition reduction N_m is lower than 2 (line 2). For each group in each scan slice, its possible transition reduction N_{ng} is compared with N_m, if $N_{ng} \geq N_m$, this group can be set up by filling X-bits in this group according to their corresponding test response bits (lines 3–9). After one pass of group setting, Stage 1 can be run again to further reduce capture-power without compression loss. After that, capture-power of this test vector should be checked to see whether it is under the safety limit, if so, the filling procedure can be stopped, otherwise, Stage 2 should be performed again to further reduce the capture transitions (lines 10–17). After Stages 1 and 2 are performed to reduce capture transitions with less compression ratio loss, if the capture-power is still higher than the threshold, another round of group setting should be conducted with a lower N_m (line 18). If N_m is already lower than 2, the group set-up procedure ends and the bit setting procedure should be conducted (lines 20–31). Once after setting one bit, Stages 1 and 2 also should be repeated, this procedure will end until the capture-power constraint is satisfied (lines 24–26 and 28–30) or there is no X-bit in the test cube.

Fig. 11 shows the example for group set-up and bit set. First, since setting up the group wherein corresponding test responses are "1111" can reduce four transitions than filling them with the default value, two additional code words are introduced for this

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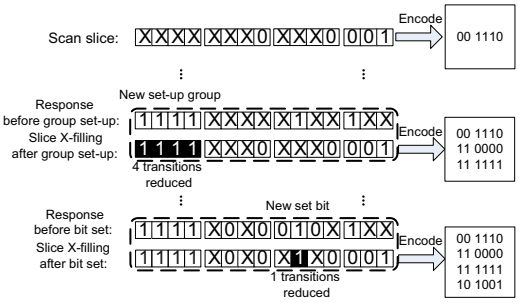

Fig. 11. X-filling with group set-up and bit set.

group. While in other groups, only one capture transition can be reduced in group "XXX0", therefore, we only need to fill that X-bit to "1" with one additional code word. Whenever one pass of group set-up or bit set is finished, Stages 1 and 2 should be performed once more for further capture-power reduction with lower compression ratio loss.

3.3.3. *Performance enhancement of the proposed technique*

From the introduction of the proposed X-filling technique above, we can see that the X-filling processes with compression ratio loss: "group expansion" and "group set-up" involves several times of iterations concerning the chosen threshold N_m (the minimum transition count can be reduced by expanding or setting-up a new group). Excessive iteration count may induce long execution time, to reduce the computational time, the expected transition reduction N_m can be initialized to a lower value in line 1 of Fig. 8, e.g., $N_{group}/2$ instead of N_{group}, and decreases more rapidly: $N_m = N_m - a$, $2 < a < N_{group}/2$ in line 16 of Fig. 8. Since the iteration count is decided by the value choice count of N_m, for example, if N_m is initialized as 4, where $N_{group}=8$, if $a=2$, N_m should be 2 after one iteration and 0 after the second iteration, so the total iteration count can be reduced to 2 now, which can significantly reduce the total computational time.

As analyzed above, if fewer N_m are selected during the X-filling processes, fewer iteration will be involved. Besides the reduction of computational time, fewer iterations may reduce the accuracy of the capture-power estimation and the filling decision, which means some loss of efficiency on capture-power reduction, but it should still outperform the one-pass X-filling procedures, e.g., *Preferred fill*, in terms of accuracy of capture-power estimation and effectiveness on capture-power reduction. On the other hand, since more X-bits would be filled in each iteration with fewer N_m, there might be slight increment on the compression ratio loss.

4. Experimental results

To verify the effectiveness of the proposed capture-power-aware test compression scheme, various experiments are conducted on larger ISCAS'89 and ITC'99 benchmark circuits and three industrial circuits. Table 2 presents the features of the experimental circuits, including the number of scan cells (*#dff*), the number of gates (*#gate*), the number of test patterns (*#pattern*) and the percentages of X-bits in the test cubes (X%). The test patterns targeting transition faults with LoC at-speed testing scheme are generated by a commercial ATPG tool.

The experimental results on compression ratio and capture-power of different X-filling strategies are given in Table 3, 4 and 5 for ISCAS'89 benchmark circuits, ITC'99 benchmark circuits and the industrial circuits, respectively. Five X-filling methods are adopted in our experiments: (1) filling the X-bits into "0"s (0-fill); (2) the original selective encoding X-filling method (Ori. [12]); (3) *Preferred fill* (Pref. [35]) which was proposed for low capture-power; (4) *Adjacent fill* (Adj. [34]) which was proposed for low shift power; (5) the proposed X-filling strategy (Prop.). The compression ratio (Compression Ratio) of these X-filling methods is obtained by

$$CR = \frac{D_{uc} - D_c}{D_{uc}} \times 100\%$$

where D_{uc} and D_c are the test data volume of the original test cube and the compressed codes.

The capture transition counts of these X-filling techniques are given in the columns under "Capture Transition" estimated by the transition count in the scan cells which has direct impact on capture-power in LoC at-speed testing scheme. The number of test vectors violating the threshold are given in the column under "Violation Count". Finally, the execution time of the proposed method with a 2.99 GHz CPU and 4 GB memory is shown in the column under "T(s)".

From Tables 3–5, several conclusion can be deduced:

1. Compared to simple "0-fill", the original Selective Encoding scheme [12] can usually achieve higher compression ratio with relatively high increment on capture-power.

Table 2
DFT profiles of the circuits under test.

Circuits	#dff	#gate	#pattern	X%
s15850	534	10540	238	80.72
s13207	638	8810	419	91.13
s38417	1636	23956	314	81.96
s38584	1426	21028	337	84.85
b20	490	9667	851	68.38
b21	490	10093	761	67.05
b22	735	15371	844	70.01
b17	1415	24808	2180	91.35
b18	2988	46743	1875	93.09
b19	5736	102769	3888	95.55
ckt_1	17079	170939	14727	99.73
ckt_2	28188	663379	12847	98.41
ckt_3	97811	569061	41530	99.90

Table 3
Experimental results for capture-power and compression ratio-1: ISCAS'89 circuits.

Circuit	Method	Compression ratio (%)	Capture transitions	Violation count	T (s)
s15850	0-fill	35.1	66	2	0.000
	Ori. [12]	42.0	121	43	0.001
	Pref. [35]	1.9	57	1	1.363
	Adj. [34]	11.6	153	81	1.351
	Prop.	40.2	108	1	2.392
s13207	0-fill	58.0	72	7	0.000
	Ori. [12]	65.4	157	91	0.005
	Pref. [35]	−20.1	163	2	1.667
	Adj. [34]	42.3	207	259	1.627
	Prop.	62.0	149	2	3.776
s38417	0-fill	36.2	202	2	0.000
	Ori. [12]	45.8	265	39	0.011
	Pref. [35]	−25.1	255	2	4.976
	Adj. [34]	32.4	318	69	4.941
	Prop.	45.4	256	2	9.240
s38584	0-fill	43.0	161	14	0.000
	Ori. [12]	50.5	392	92	0.011
	Pref. [35]	17.4	138	7	5.651
	Adj. [34]	26.0	531	279	5.585
	Prop.	45.5	332	7	18.691

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Table 4
Experimental results for capture-power and compression ratio-2: ITC'99 circuits.

Circuit	Method	Compression ratio (%)	Capture transitions	Violation count	T (s)
b20	0-fill	36.1	174	279	0.000
	Ori. [12]	42.6	180	418	0.005
	Pref. [35]	3.6	127	22	4.831
	Adj. [34]	27.4	181	423	4.791
	Prop.	37.7	162	16	26.785
b21	0-fill	40.3	147	21	0.000
	Ori. [12]	41.4	152	97	0.001
	Pref. [35]	5.0	95	5	4.625
	Adj. [34]	25.4	147	88	4.556
	Prop.	40.3	147	5	11.268
b22	0-fill	36.5	172	4	0.000
	Ori. [12]	42.9	194	20	0.016
	Pref. [35]	13.0	147	1	10.014
	Adj. [34]	27.7	207	62	9.934
	Prop.	42.7	192	0	15.241
b17	0-fill	65.9	238	1	0.000
	Ori. [12]	68.9	262	28	0.045
	Pref. [35]	41.5	191	0	43.627
	Adj. [34]	60.9	295	101	43.190
	Prop.	68.8	261	0	66.736
b18	0-fill	65.3	177	3	0.000
	Ori. [12]	70.1	220	25	0.084
	Pref. [35]	56.3	132	0	83.372
	Adj. [34]	59.6	232	53	82.909
	Prop.	70.0	220	0	141.172
b19	0-fill	60.3	352	3	0.000
	Ori. [12]	73.3	418	50	0.294
	Pref. [35]	60.3	267	0	431.587
	Adj. [34]	64.7	447	172	429.587
	Prop.	73.2	416	0	718.804

Table 5
Experimental results for capture-power and compression ratio-3: industrial circuits.

Circuit	Method	Compression ratio (%)	Capture transitions	Violation count	T (s)
ckt_1	0-fill	77.7	15732	14713	0.000
	Ori. [12]	77.9	15663	14604	3.040
	Pref. [35]	−35.8	8640	2	3316.530
	Adj. [34]	76.6	12913	4939	3277.310
	Prop.	77.4	9421	2	9470.840
ckt_2	0-fill	75.6	2093	9	0.000
	Ori. [12]	76.5	2360	599	4.800
	Pref. [35]	54.3	1913	4	12876.670
	Adj. [34]	70.9	4620	10815	12802.820
	Prop.	76.3	2342	4	24017.730
ckt_3	0-fill	77.9	1461	4	0.000
	Ori. [12]	78.0	1595	71	46.710
	Pref. [35]	75.2	1078	4	36327.100
	Adj. [34]	77.4	6400	41150	35677.620
	Prop.	78.0	1595	4	57009.560

2. If the X-bits in the test cubes are filled with "*Preferred fill*" [35] targeting at reducing capture-power, the compression ratio will be severely affected: in some cases (s13207, s38417, etc.), the test data volume would not be reduced if the X-bits are filled by "*Preferred fill*" in Selective Encoding scheme.
3. Additionally, "*Adjacent fill*" [34] targeting at shift-power reduction can usually cause the highest capture-power in LoC at-speed testing scheme, and it also cannot achieve high compression ratio in Selective Encoding test compression scheme. Since shift-power can usually be reduced by DfT-based schemes, it would be better to utilize the "X-bits" for capture-power reduction as verified in these results.
4. The proposed X-filling can always achieve the minimum capture-power violations count[4] with low compression ratio loss among all of these X-filling techniques.

Moreover, with significant test compression ratio loss, *Preferred fill* still cannot achieve the highest capture power reduction in some circuits, e.g., s13207. That is because of the inherent inaccuracy of one-pass X-filling strategy in *Preferred fill*, while in the proposed technique, X-bits are filled incrementally by several passes.

To enhance the performance of the proposed X-filling technique, N_m is initialized as 2 in the "group expansion" and "group set-up" processes of the conducted experiments to achieve the shortest runtime. From our experimental results, we can see that the proposed procedure can usually achieve satisfying capture violation reduction and compression ratio in no more than twice runtime as *Preferred fill* or *Adjacent fill* in larger circuits. When the runtime is not critical issue, higher N_m can be selected to enhance the capture-power reduction efficiency with slightly lower compression ratio loss.

To show the feature of the proposed approach on capture-power reduction more clearly, the capture-power transitions of different X-filling approaches are summarized in Fig. 12 for circuit b20, where the x-axis shows the id of the test vectors of this circuit. From this figure we can see that, among these X-filling techniques, the original Selective Encoding scheme (o_trans) and "*Adjacent fill*" (a_trans) usually produce the highest capture transitions, and "*Preferred fill*" (pr_trans) usually can give the bottom line for capture power reduction. Different from the capture transition count profile of all the other X-filling techniques which spread irregularly among different test vectors, the capture transition count of the proposed X-filling technique varies closely around the selected safety limit. Moreover, different from other X-filling techniques which arbitrarily fill all the X-bits in one pass, and the capture transition count would not change as the safety limit changes, the proposed X-filling technique has the ability to make the capture transition count more close to different safety limit settings, which will also be verified later.

Still using b20 as the example, we have also compared the effectiveness of the above X-filling approaches on capture transition reduction, violating vector reduction and compression ratio as shown in Fig. 13. It can be clearly seen that though the proposed X-filling technique does not achieve the lowest capture transition value, it has similar (lower) violating test vector count as "*Preferred fill*", and more importantly, the compression ratio maintains similarly as that of original Selective Encoding which has both high capture transition count and violating vector count.

This trend maintains similar in the other experimental circuits as summarized in Figs. 14 and 15 for the ISCAS'89 circuits and the ITC'99 circuits, respectively. In these figures we can see that among all these X-filling techniques, the proposed method is always with the minimum violating vector count (Vios. prop) and maintains similar compression ratio (CR prop) as the original Selective Encoding scheme(CR ori).

To evaluate the effectiveness of the proposed technique under different threshold settings, we have also conducted another set of experiments as shown in Table 6. For each benchmark circuit, besides the threshold used in Tables 3–5, another higher threshold is selected to check the effectiveness of the proposed X-filling

[4] Some violations are unavoidable due to the high capture transition count of the initial test cube. Under such circumstance, such test vectors should be discarded and new test cubes need to be generated to cover those faults that are solely detected by these patterns.

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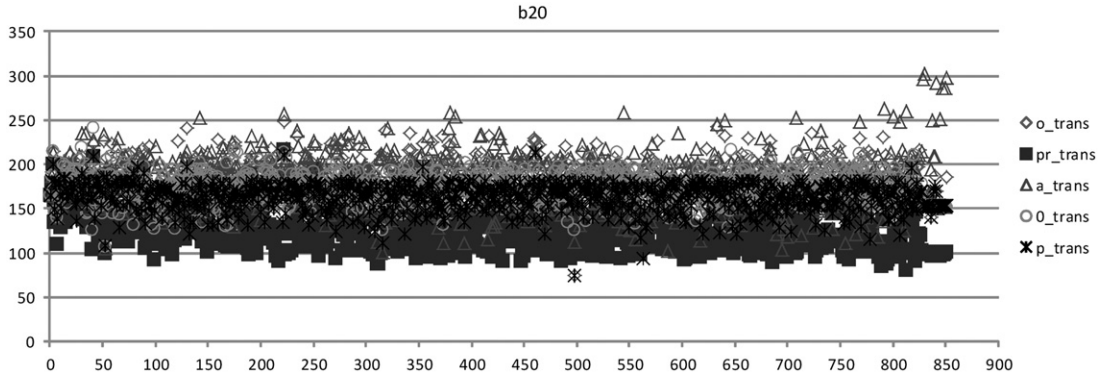

Fig. 12. Capture transition reduction of different filling approaches.

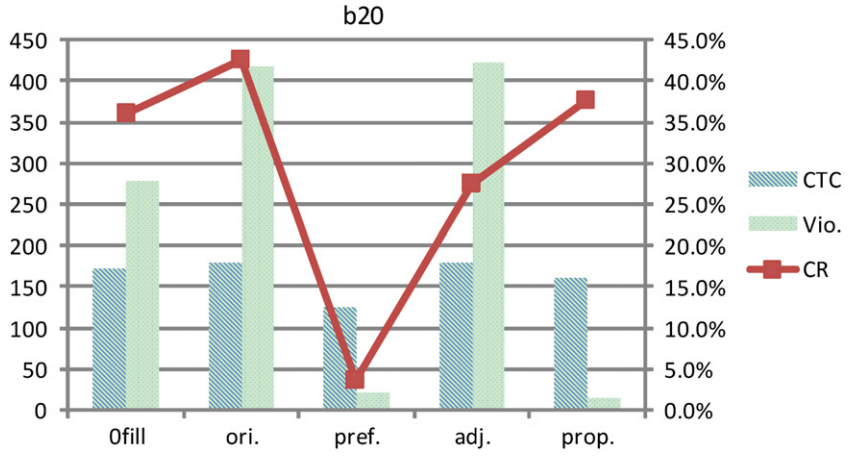

Fig. 13. Capture power and violation reduction vs. compression ratio loss.

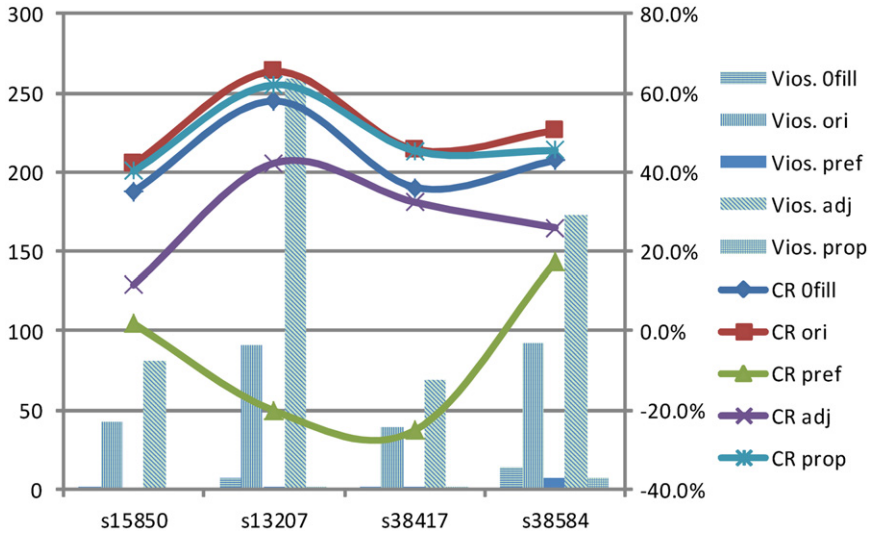

Fig. 14. Capture violation reduction vs. compression ratio loss-1: ISCAS'89 circuits.

technique. These two settings of the threshold of these circuits are denoted in the column under "*Thres.*": "1" represents the threshold selected in Tables 3–5, while "2" represents the other higher threshold setting. The compression ratio (*CR*%), capture transition count (*CTC*) of the proposed X-filling, and the capture transition violations of the original test compression and the proposed technique ("V_{ori}" and "V_{prop}") under these two different threshold settings are all given in this table. We can see that as the threshold becomes more stringent, higher capture transition reduction can be achieved by the proposed X-filling with some loss of compression ratio, but the compression ratio is still relatively high. Moreover, the violating vector count of the

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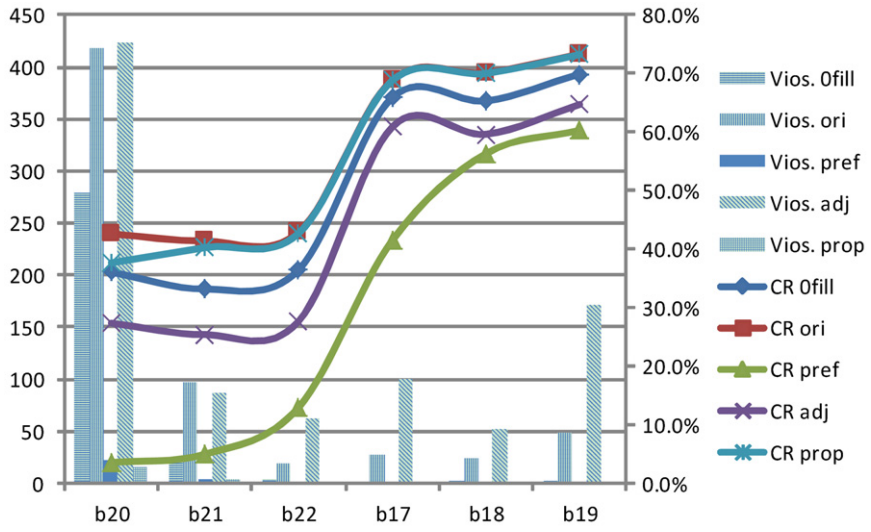

Fig. 15. Capture violation reduction vs. compression ratio loss-2: ITC'99 circuits.

Table 6
Experimental results for different threshold settings.

Circuits	*Thres.*	*CR%*	*CTC*	$V_{ori.}$	$V_{prop.}$
s15850	1	40.2	108	121	1
	2	36.5	94	105	6
s13207	1	62.0	149	91	2
	2	51.9	127	186	14
s38417	1	45.4	256	39	2
	2	43.4	233	123	10
s38584	1	45.5	332	92	7
	2	42.0	297	113	13
b20	1	37.7	162	418	16
	2	34.3	156	574	37
b21	1	40.3	147	97	5
	2	37.4	133	340	17
b22	1	42.7	192	20	0
	2	39.7	175	389	25
b17	1	68.8	261	28	0
	2	68.1	238	323	2
b18	1	70.0	220	25	0
	2	69.9	177	62	1
b19	1	73.2	416	50	0
	2	73.1	414	154	0
ckt_1	1	77.5	9439	14604	2
	2	77.4	9421	14727	8
ckt_2	1	76.3	2342	599	4
	2	75.8	2303	1113	6
ckt_3	1	78.0	1595	71	4
	2	77.9	1573	156	7

original Selective Encoding would rise rapidly as the threshold becomes more stringent, while that count of the proposed method can always be much lower than that of the original Selective Encoding scheme.

5. Conclusion

Large test data volume and high capture-power are two of the major concerns for the industry when testing large integrated circuits. With given test cubes in scan-based testing, different from prior work, which usually targets only one of these two issues, this paper studies the impact of different X-bits on capture-power and test compression ratio, and fills the X-bits with lower impact on test compression ratio iteratively for capture-power reduction to achieve a capture-power-aware test compression scheme.

By analyzing the impact of X-bits on test compression ratio, we observe that the test compression ratio is not only related to the count but also the location of the care-bits, the observation is utilized in the proposed X-filling strategy for enhancing the test compression ratio of the original test compression scheme. On the other hand, to reduce the capture-power, X-bits with less impact on compression ratio are filled until the capture-power of the given test vector is under the safety limit. Note that, although the proposed technique is based on the framework of Selective Encoding compression, the flow of the proposed technique can also be performed to other test compression schemes. Experimental results on larger ISCAS'89 and ITC'99 benchmark circuits validates that, under different threshold settings, the proposed technique can always achieve the minimum capture-power violation count with no or little test compression ratio loss.

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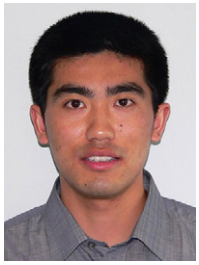

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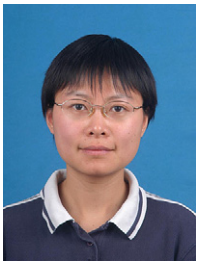

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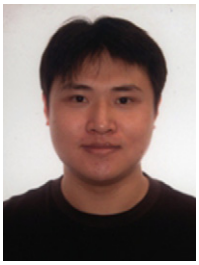

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