Test-Wrapper Designs for the Detection of Signal-Integrity Faults on Core-External Interconnects of SoCs

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Abstract

As feature sizes continue to shrink for newer process technologies, signal integrity (SI) is emerging as a major concern for core-based system-on-a-chip (SoC) integrated circuits. To effectively test SI faults on core-external interconnects, core test wrappers need to be able to generate appropriate transitions at a wrapper output cell (WOC) on the driving side and detect the signal integrity loss at a wrapper input cell on the receiving side. In current wrapper designs, the WOCs for a victim interconnect and its aggressors make transitions at the same time with a common test clock signal in test mode, which is different from the functional mode. This is not adequate for SI test because the time elapsed between the transition of the victim and the transitions of its aggressors significantly affects the behavior of SI-related errors. To address this problem, we propose new IEEE Std. 1500-compliant wrapper designs that are able to apply SI test at functional mode or make transitions with various pre-defined skews between a victim line and its aggressors. We also introduce a novel overshoot detector inside the proposed wrapper. Experimental results show that the proposed wrapper designs are more effective for detecting SI-related errors when compared to existing techniques, with a moderate amount of DFT overhead.

1 Introduction

Due to continuing advances in VLSI technology, integrated circuits (ICs) nowadays integrate hundreds of millions of transistors, and they can operate at Gigahertz frequencies. However, test problems are greatly exacerbated by the increasing complexity of ICs. For example, signal-integrity (SI) loss due to cross-coupling capacitance and inductance among interconnects, IR drop, ground bounce, and environmental variations may lead to overshoot, undershoot, glitches, ringing, inter-symbol interference, excessive signal delay or even signal speedup. These SI-related problems are aggravated in core-based system-on-a-chip (SOC) designs [17, 19], as interconnects carrying signals between embedded cores tend to be long and hence suffer more from parasitic effects. In addition, due to the complexity of the SOC interconnect topology and close proximity of long interconnects between multiple cores, signal integrity loss may involve several cores at the same time in core-based SOCs. If the noise-induced voltage swing and/or timing skew depart from the immune region, functional error may occur. A number of physical design and fabrication solutions (e.g., [3, 8]) have been proposed in the literature to tackle signal integrity problems during design and manufacture, but none of them guarantee that the problem can be completely solved. In addition, process variations and manufacturing defects aggravate the coupling problem between interconnects and render the above techniques less effective [1]. Since it is unacceptable to over-design the circuit to tolerate all possible process variations and it is impossible to predict the occurrence of physical defects, manufacturing test strategies are essential for the detection of SI-related errors [9, 22, 23].

Some SI-related errors can be detected by applying functional patterns at rated speed, but such a functional test strategy is often inadequate because it is dificult to determine appropriate functional test sequences that target all possible SI faults. The IEEE 1500 standard wrapper [11] can potentially support SI interconnect test if two-pattern at-speed signal transition capability is provided at the core test wrapper of the interconnect driving side (e.g., every wrapper output cell is equipped with two flip-flops), while at the same time integrity loss sensor (ILS) cells (e.g., [24]) are added at the wrapper of the interconnect receiving side. Unfortunately, such a design is unlikely to provide an acceptable quality level for interconnect SI test. Compared to the test for interconnect opens/shorts, SI test is very sensitive to how the test patterns are applied. The time between the signal transition of the victim lines and the transitions of its aggressor lines significantly affects the behavior of SI-related errors, as stressed in [18, 19]. Therefore, care must be taken during test application so that the dedicated SI test is applied as close to the functional mode of operation as possible. If this goal cannot be achieved, core-external SI test must be carried out to cover the worst-case scenario so as to ensure that low-quality parts are not shipped to customers.

For effective SI testing, we need to activate the worst-case crosstalk effect by aligning the switching times for all the involved interconnects, and address the worst-case effects on the victim line due to IR drop and process/environmental

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variations. To the best of our knowledge, prior work (e.g., [2, 5, 14, 24]) has not taken these issues into consideration. The approach employed in prior work is to simply let all involved core wrapper cells transit concurrently with the same test clock signal [6].

To address the above problem, we present two IEEE Std. 1500-compliant wrapper designs in this paper. These wrappers are able to either apply the core-external interconnect SI test in functional mode, or address the worst-case SI loss scenario, respectively. Note that the proposed wrappers facilitate the test application scheme to be more effective for SI-related errors, which is independent of the test patterns provided by the SoC integrators.

While overshoots lead to functional errors if only if they occur during latching windows, their adverse impact on chip reliability is a major concern [13]. In this paper, at the interconnect receiving side, we also design a new overshoot detector, which, compared to the one introduced in [20], is able to detect overshoots in all possible situations.

The remainder of this paper is organized as follows. Section 2 reviews prior work and motivates the work described in this paper. Section 3 presents the new overshoot detector. In Section 4, the proposed wrapper designs for testing interconnect SI faults are detailed. Next, in Section 5, we present experimental results based on a 90 nm process technology. Finally, Section 6 concludes this paper.

2 Related Prior Work

The *aggressor alignment problem* refers to the alignment of the switching times for multiple aggressors that results in the worst-case delay (WCD) and/or worst-case noise (WCN) on a victim interconnect. This problem has been well studied in recent years in the context of static timing analysis. It has been shown that the WCD or WCN on the victim line usually does not occur when all its aggressor lines make transitions at the same time with it, especially when there are timing-window constraints for these transitions [4, 6, 10]. Unfortunately, this problem has not been taken into account in manufacturing test solutions targeting core-external interconnects.

Built-in self-test (BIST) has been advocated to detect SI-related errors on core-external interconnects. At the driver side, test generators are embedded to generate transitions on the victim and its aggressors. Bai et al. [2] and Tehranipour et al. [24] introduced on-chip test generators based on the maximum aggressor (MA) fault model [9] and the multiple transition (MT) fault model, respectively. Li et al. [14] presented an oscillation-ring-based test scheme for SOC interconnects. None of the above techniques, however, considers the aggressor alignment issue. They apply all transitions with the same test-clock signal in test mode, which may be significantly different from the victim's functional behavior. As a result, the test outcomes can be misleading, and result in either test escapes or yield loss. Therefore, there is a need for wrapper designs that can target core-external interconnect SI test.

On the receiver side, various types of ILS cells have been proposed to detect SI-related errors. An XOR-network-based

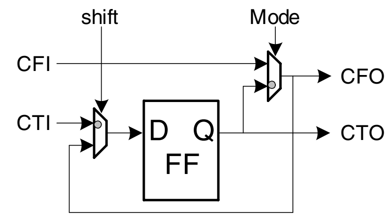
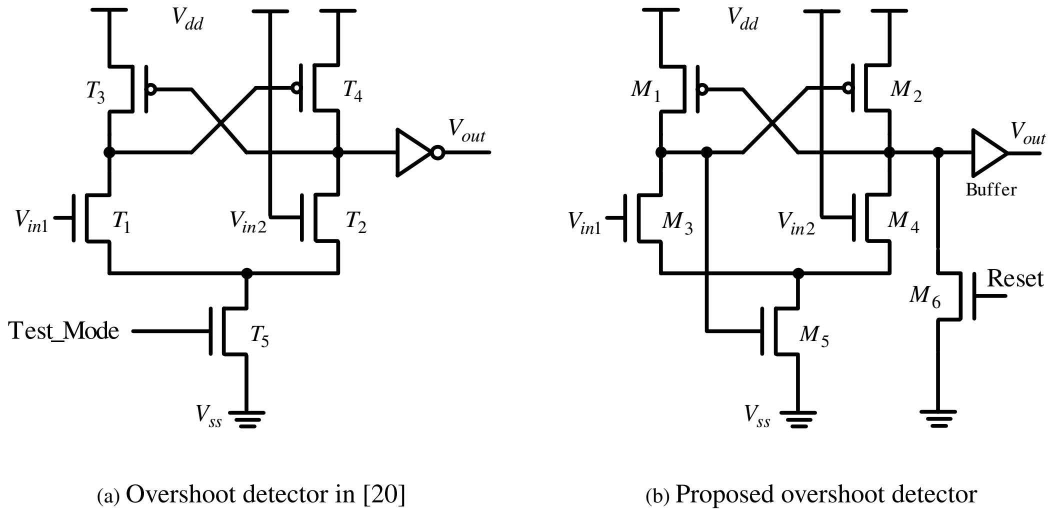


Figure 1. Regular wrapper cell design [16].

error-detector was described in [2]. However, this design is not area-efficient because it contains a local test generator to compare with test responses. Zhao et al. [25] presented an on-line testing technique that captures noise-induced logic failures by sampling the input data into two flip-flops during a given time interval and checking whether they are consistent with each other. Tehranipour et al. [23] proposed an ILS cell design to detect timing violations. However, these ILS cells cannot detect signal overshoots. Nourani and Attarha presented an ILS cell design to address this problem [20]. Their overshoot detector, however, cannot detect overshoots that occur in all situations, as described in Section 3.

The test architecture for interconnect SI faults should not invalidate the existing SOC test methodologies, i.e., it should be compatible with IEEE Std. 1500, which defines module-level test wrappers for embedded cores and allows inter-core and intra-core tests to be carried out via test access mechanisms that link the test source/sink (e.g., tester) with the test wrapper. The wrapper has three main modes [16]: (*i*) functional operation, in which the wrapper is transparent; (*ii*) an *inward-facing* test mode (also called *INTEST* mode), in which test access is provided to the core itself; and (*iii*) an *outward facing* test modes (also called *EXTEST* mode), in which test access is provided to the circuitry outside the core. Wrapper cells are introduced to the wrapper to provide controllability and observability for all core functional terminals. In the INTEST mode, used for testing the core's internal logic, the wrapper input cells (WICs) act as primary inputs to the core under test (CUT), while the wrapper output cells (WOCs) act as primary outputs. In the EXTEST mode, when all the embedded cores are wrapped, the goal is to test the interconnect wires or logic between the cores. Thus the wrapper output cells provide stimuli and the wrapper input cells capture responses from the interconnect that are blocked in them and do not get propagated to the core's internal logic.

A typical wrapper cell implementation is shown in Figure 1, which has four standard terminals: the cell functional input (CFI), the cell functional output (CFO), the cell test input (CTI), and the cell test output (CTO) [11]. The meaning of the dark circle in each multiplexer is to indicate that the corresponding path will be selected when the control signal is '1'. Note that the IEEE Std. 1500 wrapper targets only the interface, i.e., the manner in which the core communicates with its surroundings in various modes of operation. Hence, the internal structure of an IEEE Std. 1500-compliant wrapper cell can be adapted to the specific SOC test requirements, e.g., the detection of SI errors.



(a) Overshoot detector in [20]

(b) Proposed overshoot detector

Figure 2. Comparison of the proposed overshoot detectors with [20].

3 Proposed Overshoot Detector

Overshoot, the physical phenomenon in which a signal exceeds V_{dd} momentarily, seldom results in any logic error to the circuit. A logic error is likely only if the overshoot occurs during a latching window. Repeated overshoots, however, are known to be able to cause hot-carrier damage in MOS transistors [12]. These hot-carriers might penetrate the gate oxide, leading to permanent changes in the oxide charge distribution, and creating serious reliability concerns for the circuit over time [7, 13]. It is therefore important to detect the occurrences of overshoots in all possible situations as part of the manufacturing test flow.

Figure 2 compares the overshoot detector presented in [20] with the one proposed in this paper. As shown in Figure 2(a), the overshoot detector in [20] is composed of a cross-coupled differential amplifier (T_1–T_5) and an inverter (used to stabilize the output voltage). The input V_{in1} takes the signal from the victim interconnect and compares it with the other input V_{in2}, which is connected to power supply V_{dd}. Transistor T_5 that connects to the source terminal of transistors T_1 and T_2 serves as a current source to the differential amplifier. It is controlled by the SI test mode signal, so that it can be bypassed in other test modes. If the transistors are sized properly, the detector exhibits the hysteresis (Schmitt-trigger) property [21]. The output V_{out} takes logic value '0' when the voltage level of the input signal exceeds the pre-defined positive threshold voltage V_+ (say 1.1 V for a technology with supply voltage 1 V), and changes back to logic value '1' only when the voltage level of the input signal is lower than a pre-defined negative threshold voltage V_- (say 0.8 V for a technology with supply voltage 1 V). This temporary storage behavior is very useful for capturing overshoots that are of a short duration. The design in [20] is therefore very effective for detecting overshoots that occur when there is low-to-high transition for the input signal. However, due to hysteresis, once the output signal V_{out} detects an overshoot and stays at logic '0', it cannot detect the overshoots that happen when the input signal stays at logic '1' or has a high-to-low transition. This is unfortunate because overshoots may often occur in such situations.

To address the above problem, we introduce an extra transistor M_6 in our overshoot detector, as shown in Fig. 2(b). Whenever an SI error on the victim interconnect is captured, the *Reset* signal is asserted (controlled locally in the wrapper cell; see Figure 3) and the output signal is forced to return to the error-free state. Therefore, we are now able to detect overshoots that occur in all situations. In addition, we also modify the amplifier to be self-biased. The current source is provided by transistor M_5, whose gate terminal is controlled by a signal changing in the opposite direction of V_{out}, so that less current is supplied when V_{out} is logic '1', and larger current is supplied for logic '0' output. This self-biased amplifier needs no external signal for the current source and it has stronger feedback; as a result, it has a larger voltage gain and higher resolution. Finally, the buffer in the detector enables the output signal to be at the standard voltage level, corresponding to the logic value, thereby improving the driving capability for the following stages.

Figure 3 shows the IEEE Std. 1500-compliant wrapper input cell, which has been enhanced with the proposed overshoot detector. To detect timing errors and other voltage violations out of the noise-immune region, we simply use a flip-flop (FF1 in Fig. 3) in our design, but it can be replaced by other integrity-loss sensors (e.g., [23, 25]). The proposed WIC functions as the standard WIC in [16] when signals "SiTest" and "sicapt" are de-asserted. When the wrapper is in core-external interconnect SI test mode (*SiTest* ='1'), during the capture phase (*sicapt* ='1'), the test response is captured in the detector and then saved in flip-flops FF2 and FF3. After the test responses are obtained, signal *sicapt* is de-asserted while signal *shift* is asserted, and the test responses are shifted out, as shown in the timing diagram of Figure 4.

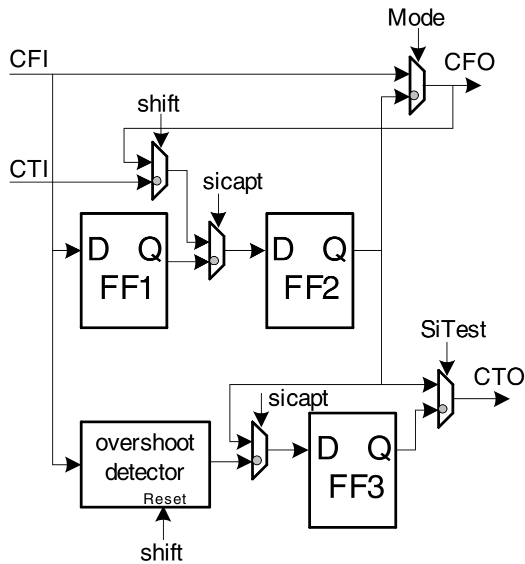


Figure 3. Wrapper input cell design with the proposed overshoot detector.

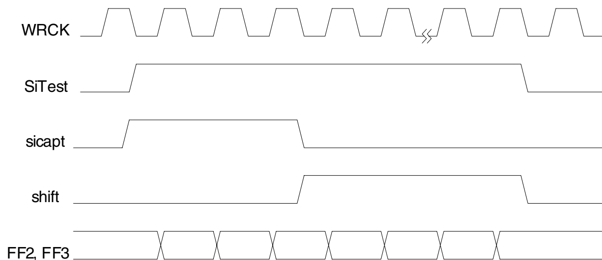


Figure 4. Timing diagram for the wrapper input cell in SI test mode.

4 Wrapper Designs for Core-External Interconnect SI Tests

As discussed in Section 2, the differences in transition times between a victim and its aggressors determine the magnitude and impact of the SI error. Previous work does not take this issue into consideration; the SI test is applied concurrently at all the involved wrapper cells with the same test-clock signal. This approach may result in over-testing or under-testing of the signal integrity loss on core-external interconnects. In this section, we present two methods and the associated wrapper designs to tackle this problem for different types of cores. We assume that the test stimuli are loaded from an external tester. BIST pattern generators are not considered in this work.

For interconnect SI tests involving only "soft cores", for which we have detailed structural information, we propose to apply the SI test patterns in normal functional mode during the capture phase. In other words, we load patterns into the wrapper input cells and the internal scan chains of the cores, and apply the patterns in functional mode in consecutive functional clock cycles to generate the test stimuli on the victim interconnect and its aggressors. There are two main advantages of this SI test strategy: (i) since the SI test is conducted in functional mode, it captures accurate SI-related errors and does not result in over-testing or under-testing; (ii) we can simply use a standard wrapper output cell as shown in Fig. 1 to apply SI test with small design-for-test (DFT) area overhead. A difficulty with this test application strategy however lies in the fact that we have to justify the test patterns on the core outputs through its inputs and internal memory elements, i.e., we need to run automatic test pattern generation (ATPG) to generate the *indirect* patterns to be loaded into the core's wrapper input cells and the internal scan chains, instead of directly loading patterns into the core's wrapper output cells and applying onto interconnects. This approach is not feasible for cores for which we do not have knowledge about their detailed internal structures (e.g., "hard cores"). Moreover, it requires relatively long test application time since we need to load the SI test patterns into core wrapper input cells and core internal scan chains, instead of directly loading them into the wrapper output cells. Finally, a new wrapper instruction needs to be introduced to apply the proposed interconnect SI test methodology.

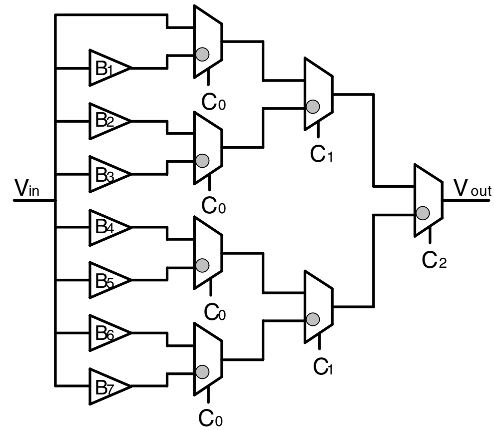


Figure 5. Controlled-delay element obtained by adding buffers with various delays.

For interconnect SI tests involving cores whose internal structure is not known or if system integrators are not willing to incur the complexity of applying the SI test in functional mode, we propose a new WOC design that is able to enforce different transition times on victims and aggressors.

It is hard to accurately predict crosstalk between SOC interconnect wires early in the design phase and it is even more difficult to accurately calculate the (temporal) skews between a victim and its aggressors that result in the maximum SI effects. We propose to realize the skewed transitions by adding buffers with different delay values in the WOC, and apply them iteratively or selectively to target the worst-case scenario during test application.

Figure 5 shows an example that adds eight different kinds of transition delays. The signal V_{out} will make a transition after V_{in} passes a buffer controlled by C_2,C_1 and C_0 and some multiplexers. The delays through the multiplexers do not affect the test procedure because all paths between V_{in} and V_{out} go through the same number and type of multiplexers. The

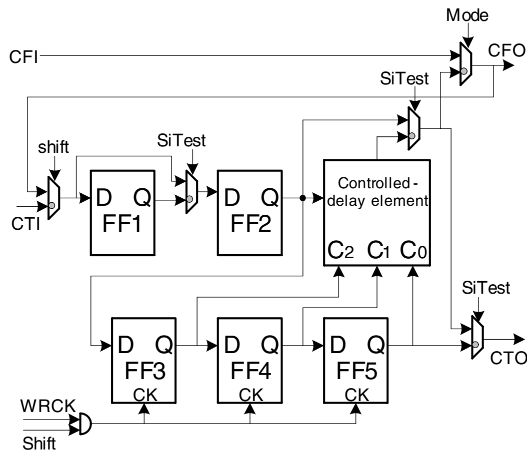


Figure 6. Wrapper output cell design with skewed-transition capability.

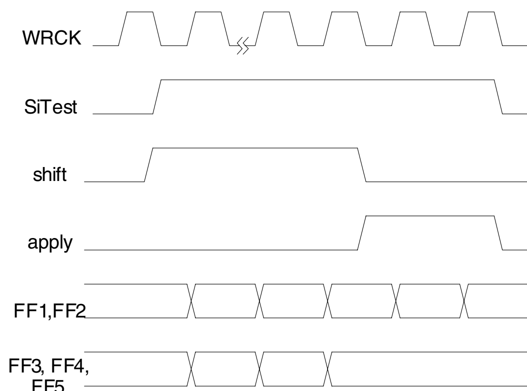


Figure 7. Timing diagram for the wrapper output cell in SI test mode.

wires connecting the components in Figure 5 are very short and their delay is neglectable. Therefore, the transition skews between the different V_{out} signals are determined only by the buffers that they pass through.

The proposed WOC with skewed transition capability is shown in Figure 6. Flip-flops FF1 and FF2 are used to store the transition to be applied to the core-external interconnect, while FF3, FF4 and FF5 are used to control the delay unit. In SI test mode, both the test vectors and the control signals are shifted into the wrapper cell first. The test patterns are then applied with skewed transition times on the victim and the aggressor interconnects. In order to prevent the control signals for the delay element to change during the capture phase, their clock signals are generated by 'ANDing' the test clock signal with the 'Shift' signal. The timing diagram of the WOC in operation is shown in Figure 7.

In practice, we expect the designers to estimate the time windows between functional mode and test mode, and the possible worst-case noise from IR drop, environmental fluctuations, and process variations. These compound noise effects can be mapped into possible skewed transitions between the victim and its aggressors, which can then be used to determine the number and the sizes of the buffers that cover worst-case scenarios to avoid the under-testing of devices. More buffers imply better and more fine-grained resolution and hence more accurate test results, but they result in larger DFT area overhead, longer testing time, and possibly some yield loss as a side-effect. For example, consider a victim interconnect with four aggressors and the maximum skew between the victim and any aggressor of 300 ps. If we introduce three types of buffers with delays 100 ps, 200 ps and 300 ps, respectively, the skew resolution is 100 ps and the test time for one SI pattern is at most $4^4 = 256$ cycles. If, however, only one type of buffer with delay 300 ps is introduced, the test time for one test pattern is at most $2^4 = 16$ cycles; however, the skew resolution for the test is significantly reduced. As a result, designers need to trade-off test quality, testing time and DFT area overhead in determining the number of buffers to be introduced in the wrapper cells.

It should be also noted that, because the proposed wrapper output cells add delay values that might not be coincident with the ones in functional mode, it is likely that the interconnect SI faults are over-tested. We rely on the designers to carefully select delay elements added into the wrapper cells to solve this problem. After all, the proposed methodology gives the designers the flexibility to achieve quality tests in line with their guidelines, which is not possible with traditional wrapper cells and is particularly important for SoCs with high reliability requirements.

5 Experimental Results

In this section, we report SPICE simulation results for a 90 nm process technology with nine metal layers. The results demonstrate the effectiveness of the proposed methods for interconnect SI testing. We use Synopsys HSPICE tool for the simulations.

5.1 Results for the Overshoot Detector

The power-supply voltage V_{dd} for the 90 nm technology is $1V$, and we set the overshoot limit as 10% more than V_{dd}, i.e., $V_+ = 1.1$ V. Figure 8 compares the simulation waveforms for the detector in [20] with those for the proposed overshoot detector. As can be observed from Figure 8(a), the input signal to the wrapper input cell, CFI, has a low-to-high transition in the first SI test and stays at logic '1' in the next two SI tests, followed by a high-to-low transition after the third SI test and transits back to logic '1' for the last two SI tests. Overshoots occur in the first, the third, the fourth, and the fifth SI tests, in which the amplitude and breadth of the overshoot happened in the fourth SI test (i.e., VO_3) is smaller than the others. We carefully fine-tuned the design of the proposed detector and the detector proposed in [20] so that they are of similar size and activate detection when the overshoot signal exceeds V_+.

As shown in Figure 8(d), the overshoot detector of [20] successfully identifies the first overshoot, but its output subsequently remains in the error state (logic '0' in this detector) until CFI changes to logic '0' before the fourth SI test. This response is clearly incorrect for the second SI test. For the proposed overshoot detector, however, every time before the

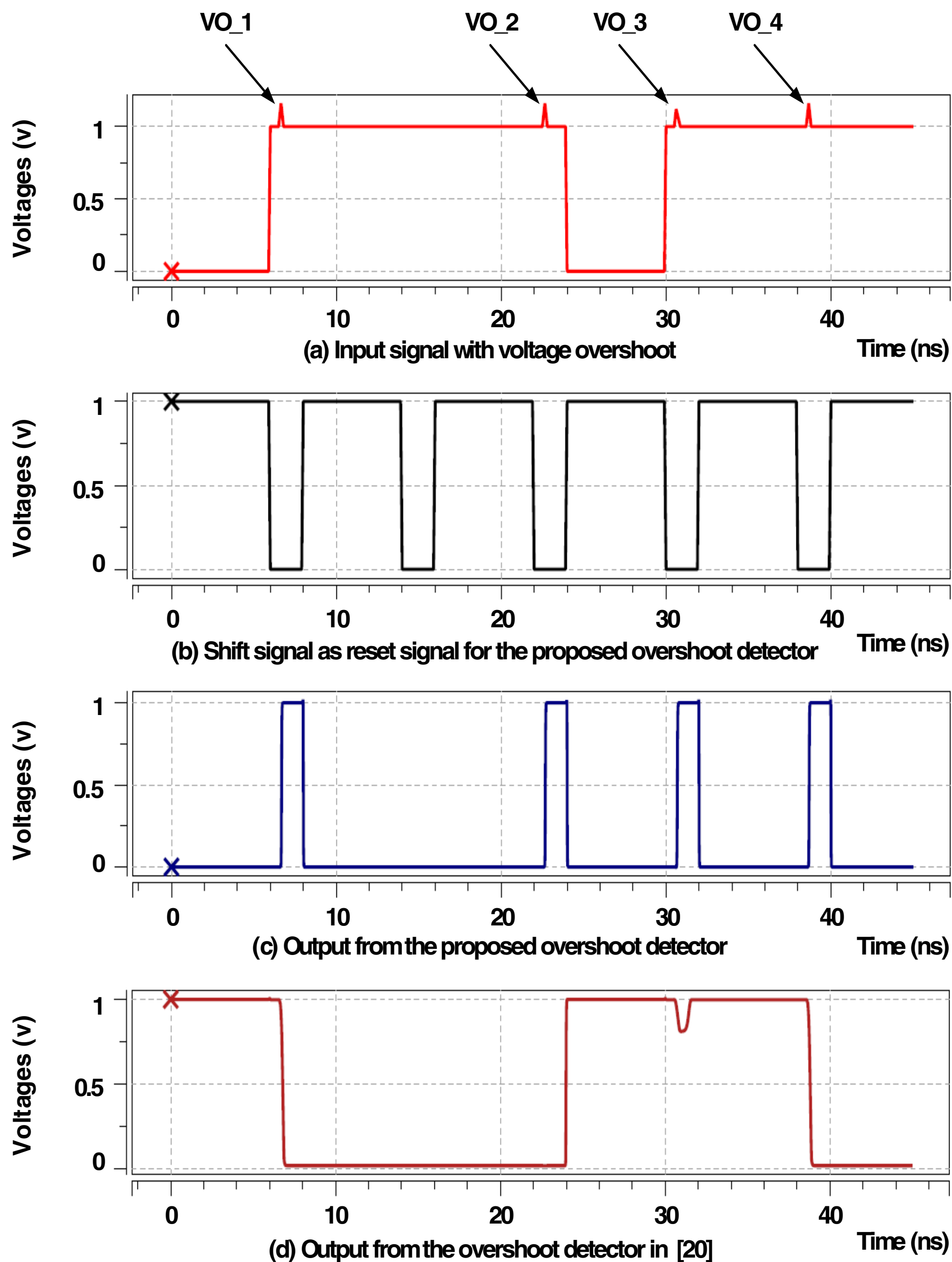


Figure 8. Comparison of the overshoot detection results.

SI test pattern is actually applied to the interconnects (i.e., during the shift phase), the 'Shift' signal inside the wrapper input cell stays at logic '1' and resets the detector back to the error-free state. During the capture phase, as shown in Fig. 8(c), whenever the input signal has a overshoot violation, our wrapper input cell is able to capture it (logic '1' in this detector). That is, with the property that the proposed overshoot detector is able to reset itself in the beginning of every SI test cycle, we can correctly identify all overshoots at the cost of only one transistor. In addition, for the overshoot happened in the fourth SI test, the breadth of the overshoot is not large enough for the overshoot detector of [20] to catch. Because our overshoot detector has a larger voltage gain and higher resolution with the self-biased amplification property resulting from the circuit topological advantage, however, it successfully detects this overshoot using similar size as the one in [20].

5.2 Results for the Proposed Wrapper Output Cell

To evaluate the effectiveness of the proposed wrapper output cell for detecting core-external SI errors, we set up the simulation environment shown in Figure 9. The victim interconnect is assumed to be 5 mm long and we also assume that there are five aggressors coupled with it. These five aggressors couple with the victim line at different sites with 0.5 mm length on the eighth metal layer of the technology and the distance be-

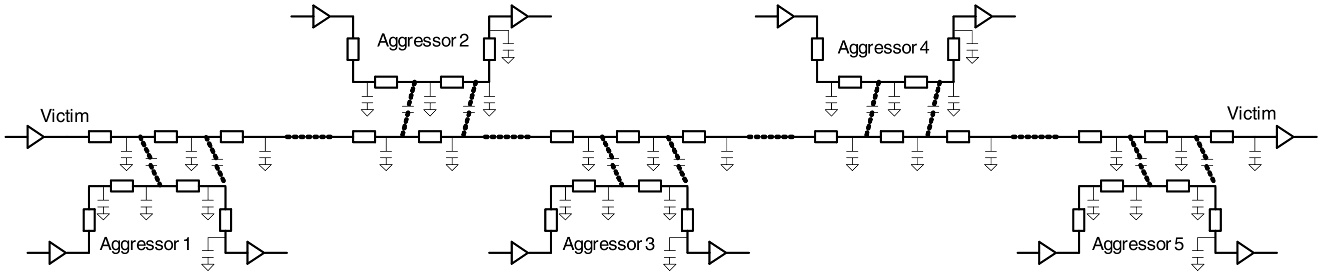


Figure 9. Experimental setup for SPICE simulations.

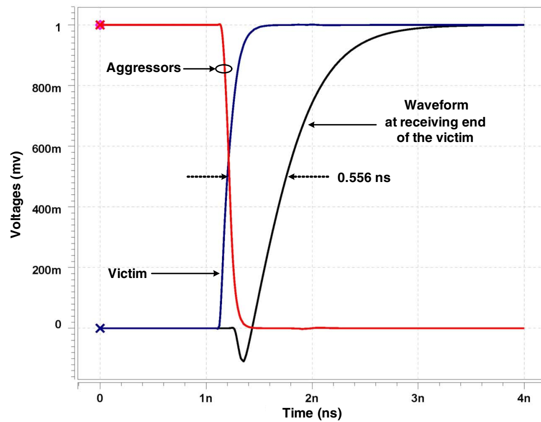


Figure 10. Timing diagram for SI tests with the regular IEEE Std. 1500 WOC.

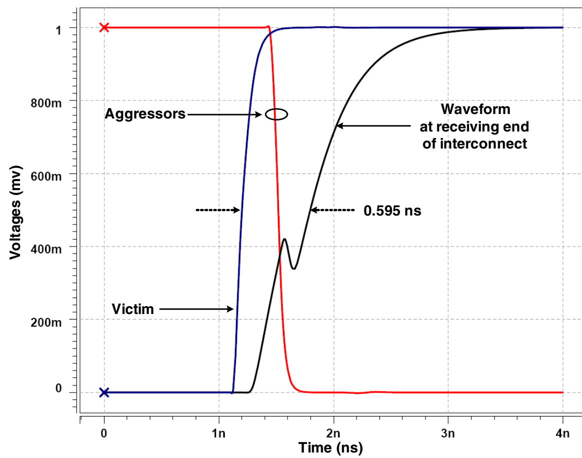
tween every aggressor and the victim is 0.28 μm. In addition, all the wires are assumed to be 0.84 μm wide. The resistances, wire self capacitances and the coupling capacitances are calculated based on the parameters from the technology provider. For SPICE simulation, we use a distributed RC model with each segment of length 0.05 mm long. At the driving side, the WOC connects to a buffer composed of two inverters (with the first one minimum-sized and the second one four times larger) to drive the interconnects. At the receiving side, the interconnect directly connects to the wrapper input cell.

Figure 10 presents the timing diagram for the case that the regular IEEE 1500 Std. wrapper output cells in [16] are used to apply the signal integrity test. As can be observed from the figure, all the five aggressors make the high to low transitions at the same time with the victim's transition, and the propagation delay from the driving end of the victim interconnect to its receiving end is 0.556 ns. Figure 11 shows the timing diagrams for the case when the proposed wrapper output cells are utilized, with the number of buffers to be 2, 4, 6, and 8, respectively. When the aggressors make transitions at different time with 8 buffers, as shown in Fig. 11(d) (three lines are shown because aggressors 1 and 2, and aggressors 3 and 4 go through the same buffer), the propagation delay from the driving end of the victim interconnect to its receiving end is 0.627 ns, which is close to 13% larger than the case with regular wrapper output cells. Clearly, without skewed-transition capability, the regular wrapper output cells is not able to detect timing errors that may happen in functional mode on the victim interconnect, thus leading to under-testing of the device. The proposed WOC design is able to detect such errors and hence allows us to ship high-quality products to the customer.

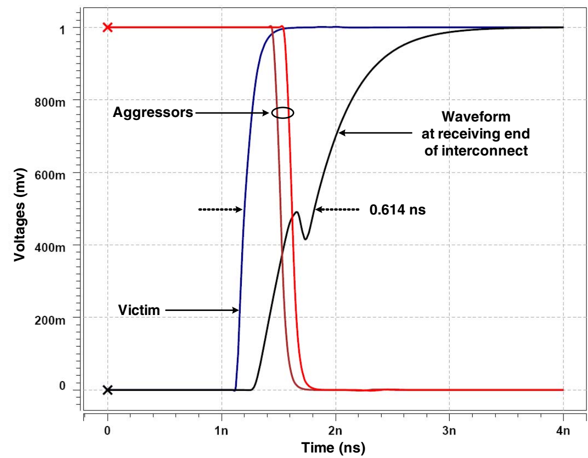
Figure 11 also compares the effectiveness of the SI tests when the number of buffers inside the proposed WOC is varied. As can be observed from the figure, when only 2 buffers are used in the WOC, the propagation delay is 0.595 ns, which is 5 percent less than the case when 8 buffers are used in the WOC. When 4 or 6 buffers are employed, however, the propagation delay is quite similar to the one with 8 buffers. More buffers in the WOC implies larger DFT area overhead and longer testing time; therefore, although the test resolution is higher for 8 buffers, the DFT engineers may opt to use 4 or 6 buffers based on their test requirements.

5.3 DFT Area Overhead for the Proposed Wrapper Output Cell

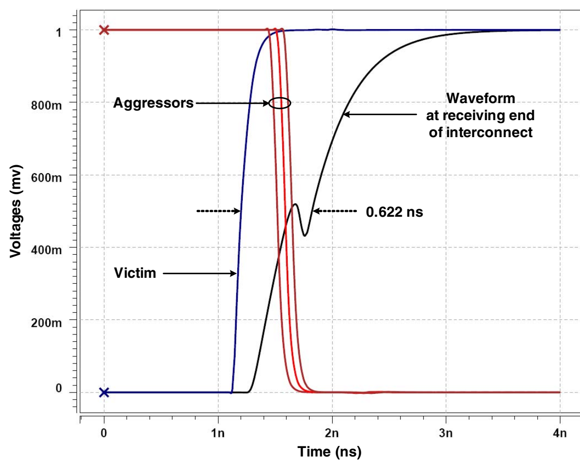
Finally, we discuss the area overhead of the proposed wrapper designs. Compared to a IEEE Std. 1500 wrapper cell, the new wrapper input cell contains two more flip-flops, three additional multiplexers and a new overshoot detector and hence is about 30∼40 two-input NAND-equivalent gates larger than the standard wrapper input cell. The new wrapper output cell contains four more flip-flops, three extra multiplexers and a new controlled-delay element. The size of the delay unit is determined by the number and the sizes of the buffers. With the example design in Fig. 5, the new WOC has 60∼80 additional two-input NAND gates compared to the regular wrapper output cell. The DFT area overhead is hence potentially quite high if all the core outputs are supplied with the proposed wrapper cells. For example, for a large industrial benchmark SoC s34392 with 997 core output terminals [15], the DFT area overhead is around 60k∼80k two-input NAND gates. In practice, however, the proposed wrapper cells can be used only for those interconnects that are estimated to have larger coupling effects with other wires (typically long wires and those not adequately protected/shielded for SI-related errors). Suppose 20 percent of these core outputs are equipped with the proposed WOC. In this case, the DFT area is only 15k gates, which is acceptable considering the improved test quality.



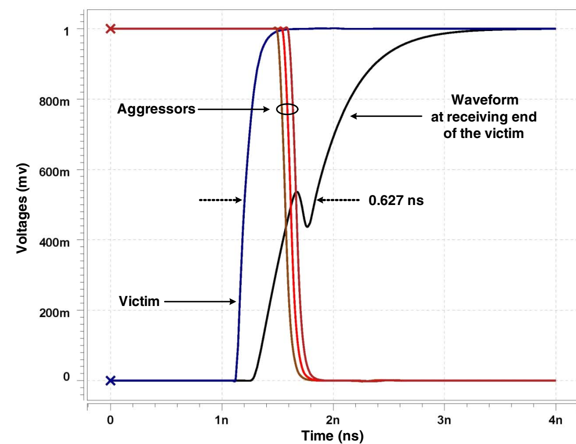
(a) SI test applied with 2 buffers in the WOC



(b) SI test applied with 4 buffers in the WOC



(c) SI test applied with 6 buffers in the WOC



(d) SI test applied with 8 buffers in the WOC

Figure 11. Timing diagrams for SI tests using the proposed WOC with different buffer counts.

6 Conclusion

Signal integrity is a major concern for today's complex system-on-a-chip integrated circuits. In this paper, we have presented two IEEE 1500-compatible wrapper designs to effectively test SI-related faults on core-external interconnects. These wrappers can apply signal integrity tests in functional mode or enforce transitions on interconnects with various predefined skews between a victim line and its aggressors. We have also introduced a novel overshoot detector inside the proposed wrapper, which is able to detect the occurrences of overshoots in all possible situations. SPICE Simulation results for a 90 nm technology show that the proposed wrapper design is more effective for detecting SI-related errors when compared to existing techniques, with a moderate amount of DFT overhead.

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