



CENG4480

Lecture 10: Clock

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(Latest update: December 3, 2020)

Fall 2020



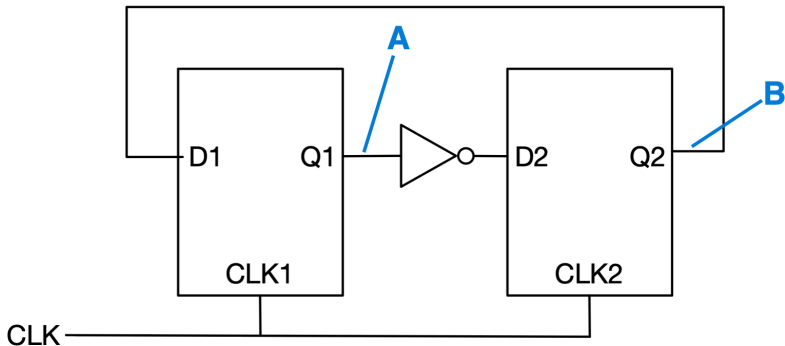
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A 2-bit ring counter example

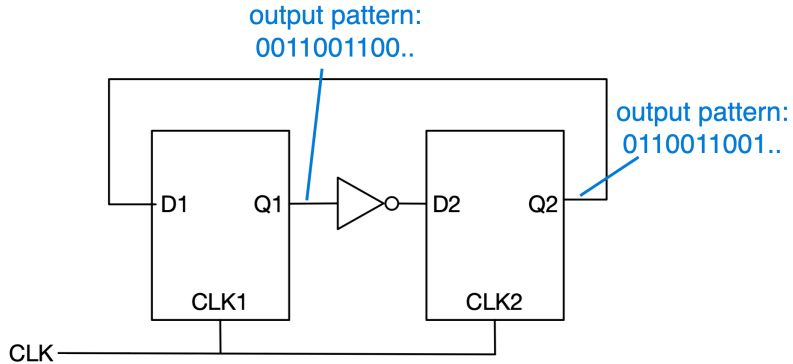
- ▶ 2-bit ring counter
- ▶ Initially $A = B = 0$; $A = 0011001100$
- ▶ What is B ?





A 2-bit ring counter example

- ▶ The result is Okay when clock is slow
- ▶ But, when clock is TOO fast, get some problem



Setup Time and Time Margin

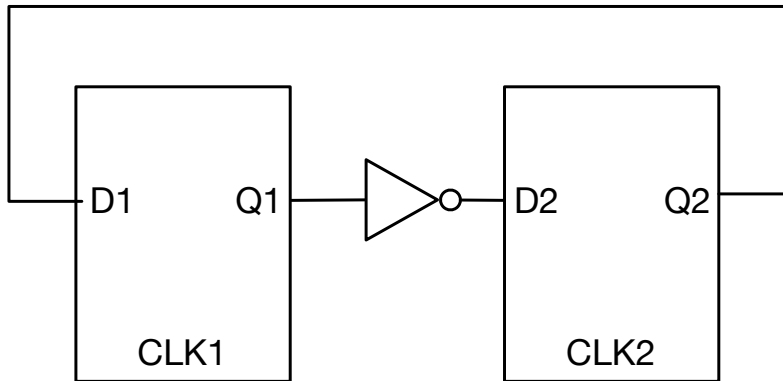


- ▶ **Setup Time:** The time that the input data must be stable before the clock transition of the system occurs
- ▶ **Time Margin:** measures the slack, or excess time, remaining in each clock cycle
 - ▶ Protects your circuit against signal cross-talk, miscalculation of logic delays, and later minor changes in the layout
 - ▶ Depends on both time delay of logic paths and clock interval

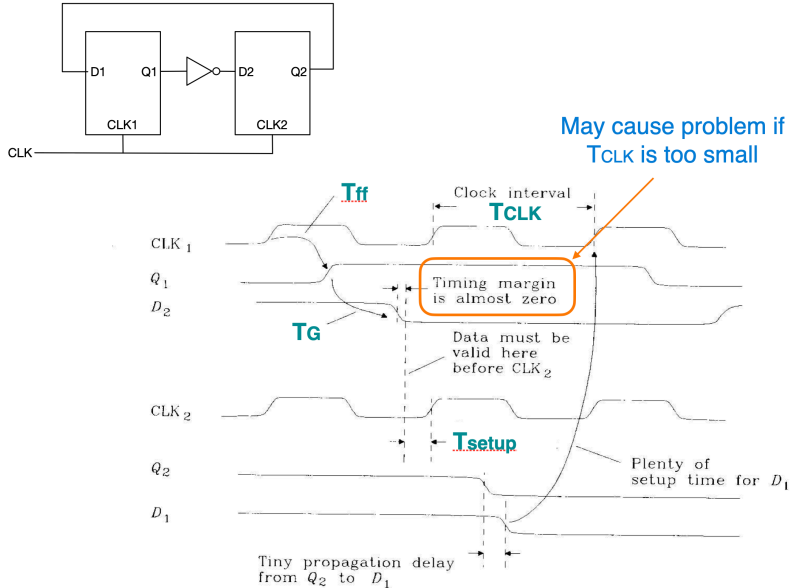
Notations in Clock Skew Calculation



- ▶ T_{ff} : delay of flip-flop (FF)
- ▶ T_G : delay of gate G, including track delay
- ▶ T_{setup} : worst-case setup time required by FF2, data at D2 must arrive at least T_{setup} before CLK_2



May cause problem if T_{CLK} is too small

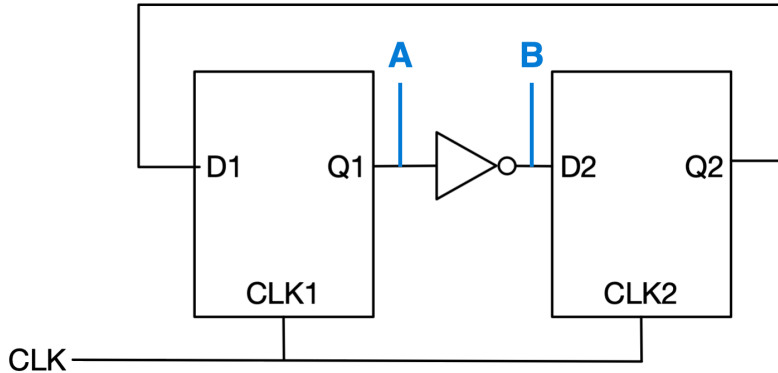




EX. B2-1

$CLK1 = CLK2 = 20MHz$; $T_{ff} = 8ns$; $T_{setup} = 5ns$; $TG = 10ns$.

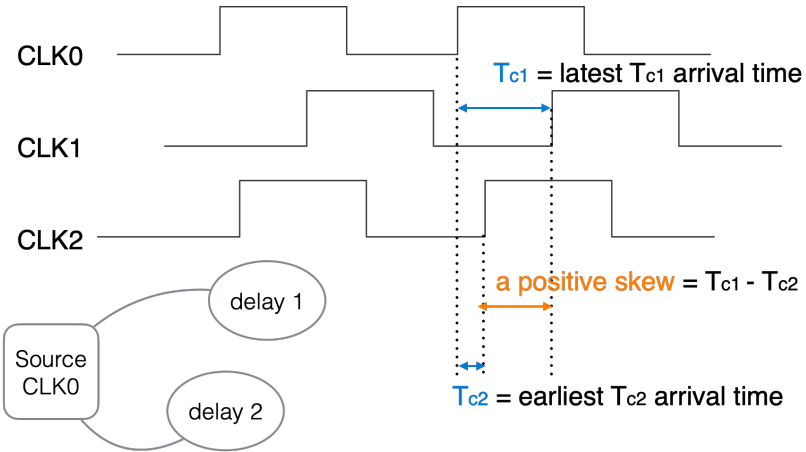
- ▶ Find time margin
- ▶ How many delay G gates can you insert between A and B without creating error?



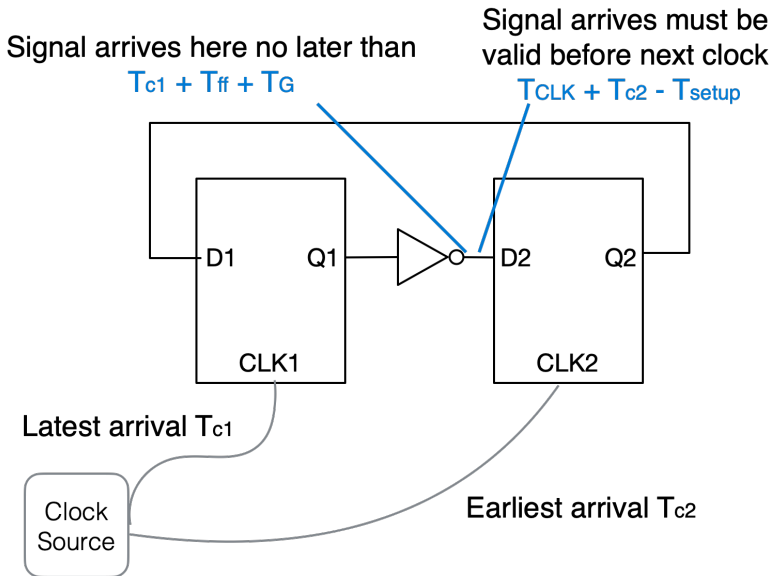
Clock Skew



▶ The clock does NOT reach FF1, FF2 at the same time



Why Care Clock Skew?



Why Care Clock Skew?



- ▶ $T_{delay} = T_{c1} + T_{ff} + T_G$
- ▶ $T_{clk'} = T_{CLK} + T_{c2} - T_{setup}$
- ▶ Since $T_{delay} < T_{clk'} \Rightarrow$

$$T_{CLK} > T_{ff} + T_{setup} + T_G + T_{c1} - T_{c2}$$

Constant
Delay

Logic
Delay

Skew
Impact



EX. B2-2

Given

- ▶ $T_{ff} = 7\text{ns};$
- ▶ $T_G = 5\text{ns};$
- ▶ $T_{setup} = 4\text{ns};$
- ▶ $T_{CLK} = 40\text{MHZ};$

What's the biggest time skew allowed?

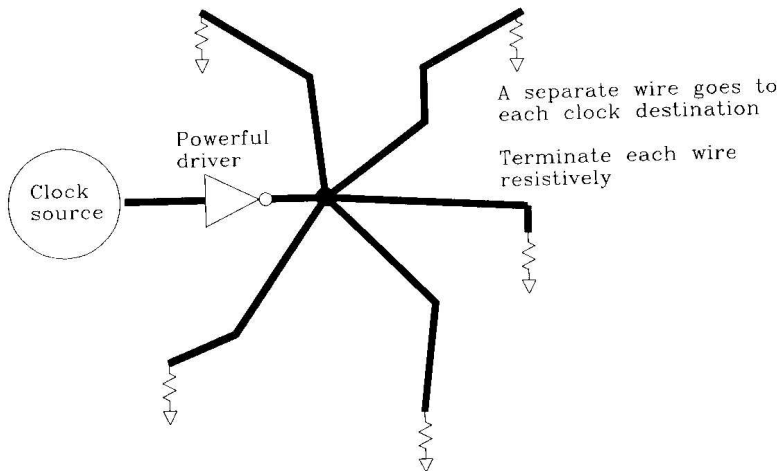
Answer:

Strategies to reduce clock skew

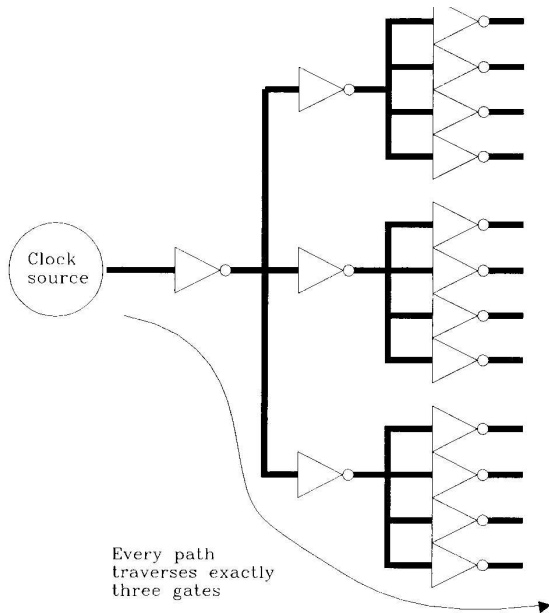


- ▶ Drive them from the same source & balance the delays
- ▶ **Style 1:** Spider-leg distribution network
 - ▶ use a power driver to drive N outputs.
 - ▶ Use load (R) termination to reduce reflection if the traces are long (distributed circuit).
Total load = R/N .
 - ▶ Two or more driver outputs in parallel may be needed.
- ▶ **Style 2:** Clock distribution tree

Style 1: Spider-leg Clock

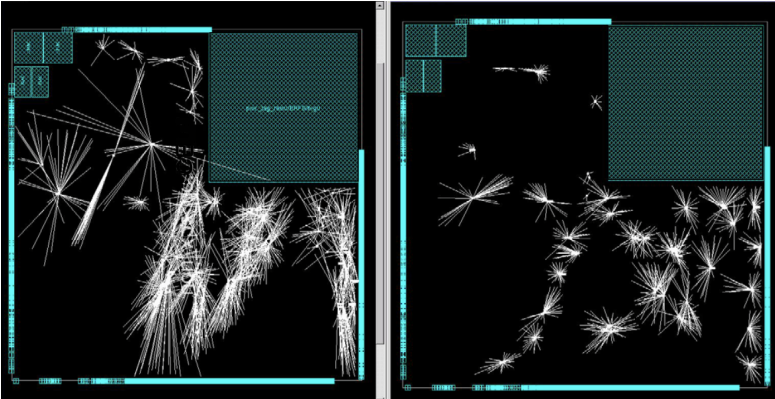


Style 2: Clock Tree

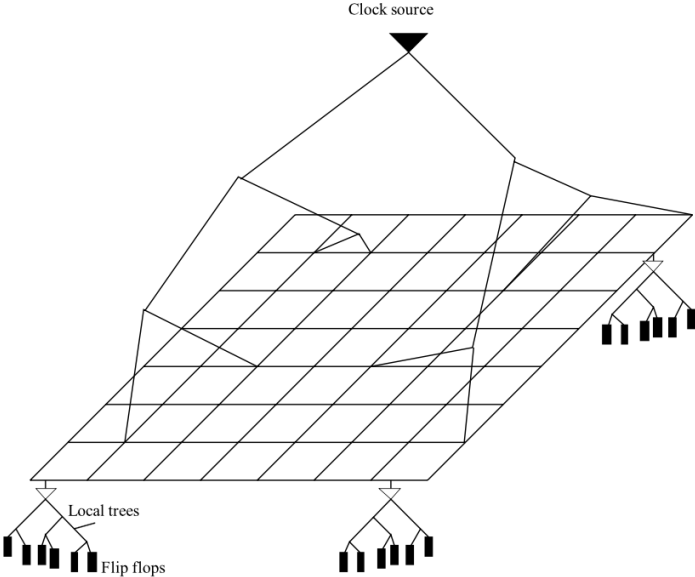


Every path
traverses exactly
three gates

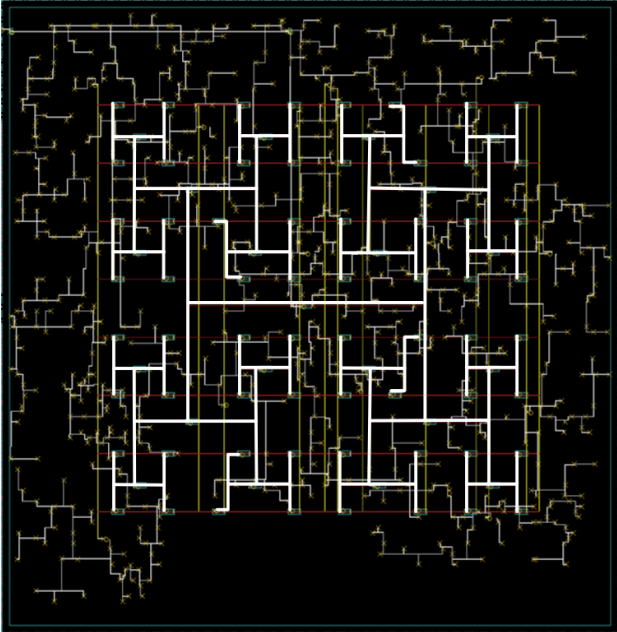
Modern Clock Design 1



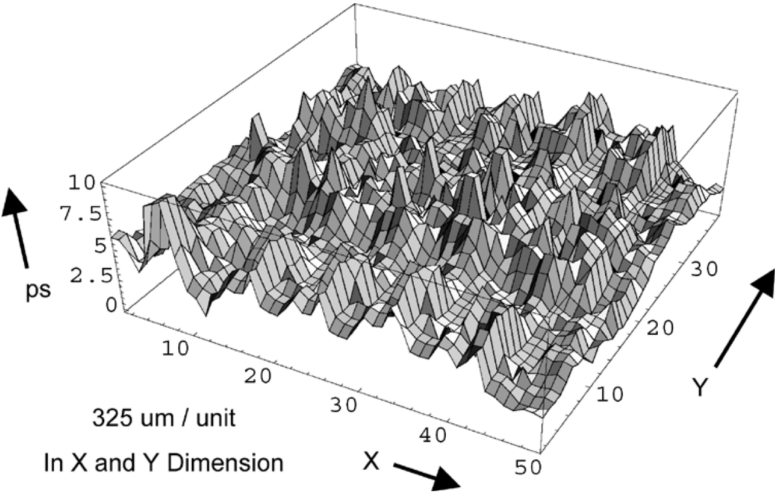
Modern Clock Design 2



Modern Clock Design 3



Clock Skew Distribution



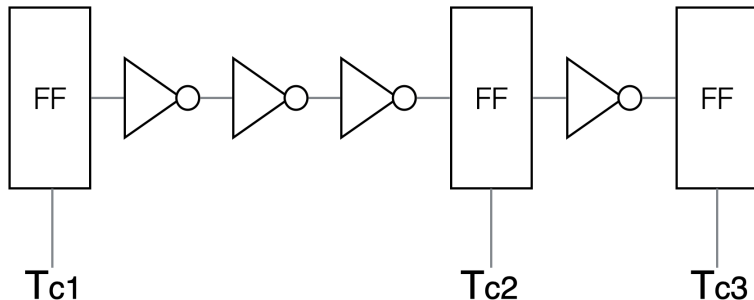
EX. Skew Optimization



Instead of Zero-Skew, take advantage of Skew.

Question:

Given $T_G=6\text{ns}$, $T_{ff}=10\text{ns}$, $T_{setup}=2\text{ns}$, what's the minimal T_{CLK} ? Assume $T_{c3} = 0$.





Thank You :)