CENG4480 Homework 3

Q-1 Given

- $T_{ff} = 8ns$;
- $TG = 6ns$;
- $T_{setup} = 4ns$;
- $T_{CLK} = 40MHz$;

What's the biggest time skew allowed?

Q-2 Given the logic circuit as shown in Figure 1, please write down outputs s and c_{out} w. r. t. inputs a, b and c. What the function of this circuit?

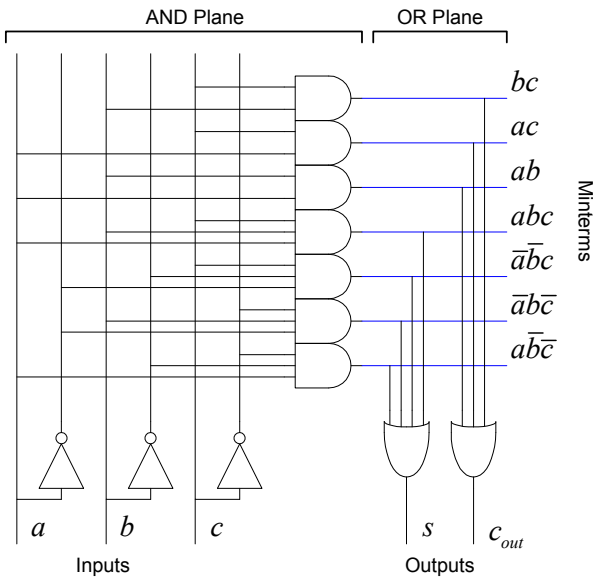


Figure 1: The Logic Circuit for Question 3

Q-3 Analysis the properties of SRAM, DRAM, SDRAM and DDR-SDRAM.

Q-4 What is the modern memory hierarchy? Plz draw the figure and Analyze the corresponding properties of each hierarchy level.

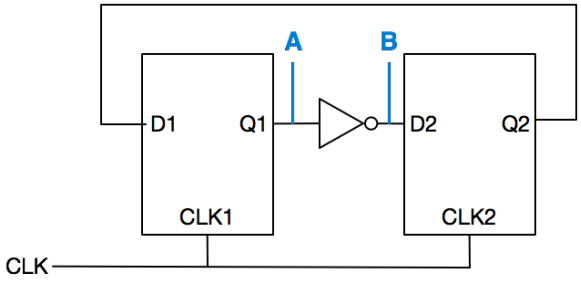
Q-5 The general equation of a liner estimate system is like $\mathbf{x}_{t+1} = \mathbf{A}\mathbf{x}_t + \mathbf{w}_{t+1}$. Given a second-autoregression random series:

$$x(t) = 2.32x(t-1) - 0.76x(t-2) + \omega_t \tag{1}$$

Kalman Filter is used to estimate $x(t)$ (Here $x(t)$ is a scalar). Try to give the formulations of state transition matrix $\mathbf{A}$ and noise vector $\mathbf{w}_t$.

Q-6 A digital clock is important in circuit design. Please answer the following **three** questions.

(a) Given the following circuit, CLK1 = CLK2 = 25MHz; Tff = 5ns; Tsetup = 5ns. The gate delay TG = 10ns. Please calculate the time margin. Note: Tff= delay of a flip flop, Tsetup=setup time of a flip flop, and TG is delay of a gate.



(b) In the above circuit, currently there is already one delay gate with delay TG. How many more similar delay gates can you insert between A and B without creating error?

(c) Sometimes we can take advantage of clock skew. For the above circuit, if the delay from CLK to CLK2 is 4ns, calculate the minimal clock period of the clock CLK.

Q-7 Given the 6T-SRAM cell as in Figure 2, discuss the reading behavior (i.e., reading steps) if originally A = 1, A_b = 0.

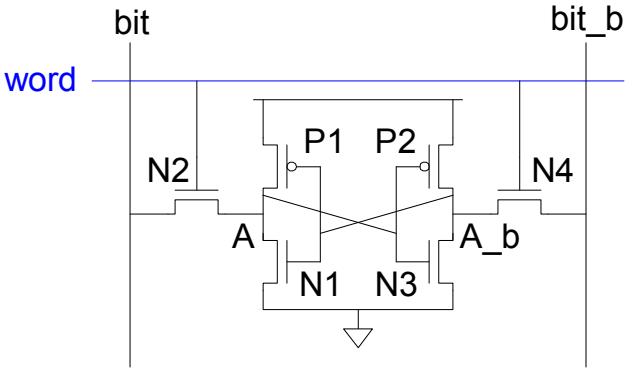


Figure 2: 6T-SRAM cell structure.