# CENG4480 Homework 3

## Solutions

**Q-1** Given

- $T_{ff} = 8ns$;
- $TG = 6ns$;
- $T_{setup} = 4ns$;
- $T_{CLK} = 40MHz$;

What's the biggest time skew allowed?

**A1** 25-8-6-4=7ns.

**Q-2** Given the logic circuit as shown in Figure 1, please write down outputs $s$ and $c_{out}$ w. r. t. inputs $a$, $b$ and $c$. What the function of this circuit?

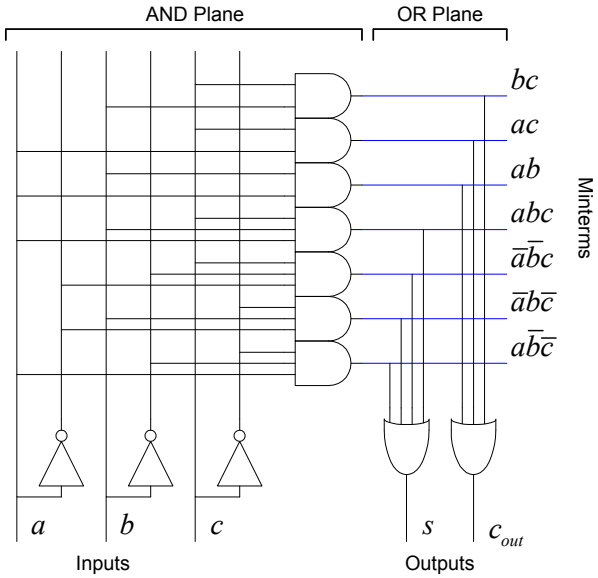



Figure 1: The Logic Circuit for Question 3

**A2** $s = a\bar{b}\bar{x} + \bar{a}b\bar{c} + \bar{a}\bar{b}c + abc$; $c_{out} = ab + bc + ac$; Full Adder.

**Q-3** Analysis the properties of SRAM, DRAM, SDRAM and DDR-SDRAM.

**A3** **Static RAM (SRAM)**

1. Capable of retaining the state as long as power is applied.

2. They are fast, low power (current flows only when accessing the cells) but costly (require several transistors), so the capacity is small.
3. They are the Level 1 cache and Level 2 cache inside a processor, of size 3 MB or more.

**Dynamic RAM (DRAM)**

1. store data as electric charge on a capacitor.
2. Charge leaks away with time, so DRAMs must be refreshed.
3. In return for this trouble, much higher density (simpler cells).

**SDRAM**

1. The common type used today as it uses a clock to synchronize the operation.
2. The refresh operation becomes transparent to the users.
3. All control signals needed are generated inside the chip.
4. The initial commercial SDRAM in the1990s were designed for clock speed of up to133MHz.
5. Today's SDRAM chips operate with clock speeds exceeding 1 GHz.

**DDR-SDRAM**

1. normal SDRAMs only operate once per clock cycle.
2. Double Data Rate (DDR) SDRAM transfers data on both clock edges.
3. DDR-2 (4x basic memory clock) and DDR-3 (8x basic memory clock) are in the market.
4. They offer increased storage capacity, lower power and faster clock speeds.
5. For example, DDR2 can operate at clock frequencies of 400 and 800 MHz. Therefore, they can transfer data at effective clock speed of 800 and 1600 MHz.

**Q-4** What is the modern memory hierarchy? Plz draw the figure and Analyze the corresponding properties of each hierarchy level.

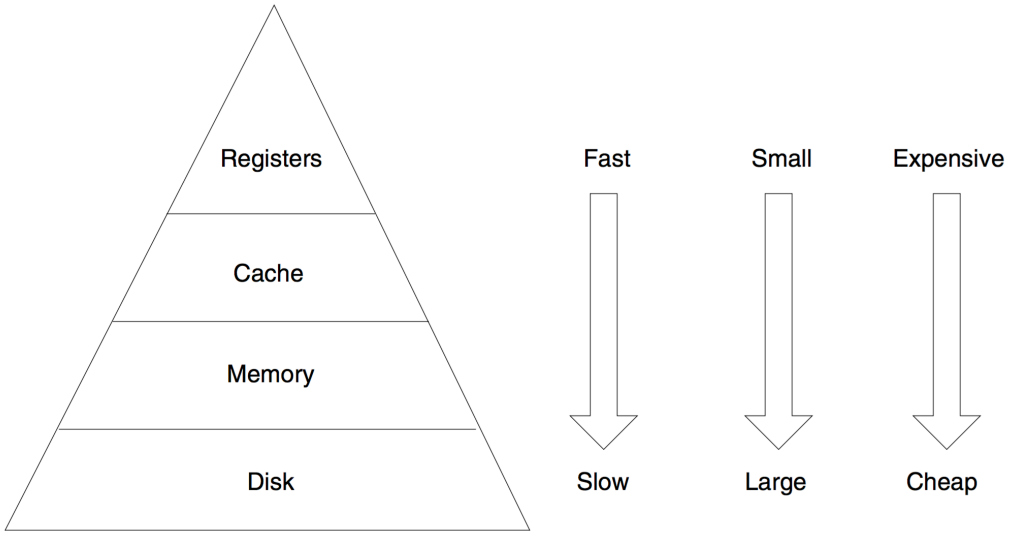
**A4** (Analyze based on the following figure:)

1. On-Chip Register; L1, L2 Cache; Main Memory; Secondary Storage (Disk).
2. Working speed decrease and storage size increase along above hierarchy level.

**Q-5** The general equation of a liner estimate system is like $\mathbf{x}_{t+1} = \mathbf{A}\mathbf{x}_t + \mathbf{w}_{t+1}$. Given a second-autoregression random series:

$$x(t) = 2.32x(t-1) - 0.76x(t-2) + \omega_t \tag{1}$$

Kalman Filter is used to estimate $x(t)$ ( Here $x(t)$ is a scalar). Try to give the formulations of state transition matrix $\mathbf{A}$ and noise vector $\mathbf{w}_t$.




**A5** The random series is extended as:

$$\begin{cases} x(t-1) &= 0 \cdot x(t-2) &+ 1 \cdot x(x-1) &+ 0 \\ x(t) &= -0.76 \cdot x(t-2) &+ 2.32 \cdot x(t-1) &+ \omega_t \end{cases} \tag{2}$$

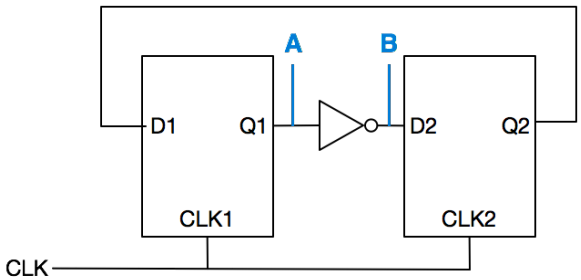
Its matrix form is

$$\begin{bmatrix} x(t-1) \\ x(t) \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ -0.76 & 2.32 \end{bmatrix} \cdot \begin{bmatrix} x(t-2) \\ x(t-1) \end{bmatrix} + \begin{bmatrix} 0 \\ \omega_t \end{bmatrix} \tag{3}$$

Let $\boldsymbol{\chi}(t) = \begin{bmatrix} x(t-1) \\ x(t) \end{bmatrix}$, $\boldsymbol{\chi}(t-1) = \begin{bmatrix} x(t-2) \\ x(t-1) \end{bmatrix}$, $\mathbf{A} = \begin{bmatrix} 0 & 1 \\ -0.76 & 2.32 \end{bmatrix}$ and $\mathbf{w}_t = \begin{bmatrix} 0 \\ \omega_t \end{bmatrix}$, (3) is equivalent to $\boldsymbol{\chi}(t) = \mathbf{A} \cdot \boldsymbol{\chi}(t-1) + \mathbf{w}_t$.

**Q-6** A digital clock is important in circuit design. Please answer the following **three** questions.

**(a)** Given the following circuit, CLK1 = CLK2 = 25MHz; Tff = 5ns; Tsetup = 5ns. The gate delay TG = 10ns. Please calculate the time margin. Note: Tff= delay of a flip flop, Tsetup=setup time of a flip flop, and TG is delay of a gate.




**(b)** In the above circuit, currently there is already one delay gate with delay TG. How many more similar delay gates can you insert between A and B without creating error?

**(c)** Sometimes we can take advantage of clock skew. For the above circuit, if the delay from CLK to CLK2 is 4ns, calculate the minimal clock period of the clock CLK.

**A6** 1. Period = $\frac{1}{25\text{M}} = 40\text{ns}$. Margin = $40 - 5 - 5 - 10 = 20\text{ns}$

2. Max #gate = $\frac{20}{10} = 2$. So 2 more gates can be inserted.

3. Since we are searching for minimal period, no slack is desired.

$$\text{Tc1} + \text{Tff} + \text{TG} + \text{Tsetup} = \text{TCLK} + \text{Tc2} \tag{4}$$

From Equation (4) we have $\text{TCLK} = 20 + \text{Tc1} - \text{Tc2}$. We set Tc1 = 0, then we can obtain TCLK = 16ns

**Q-7** Given the 6T-SRAM cell as in Figure 2, discuss the reading behavior (i.e., reading steps) if originally A = 1, A_b = 0.

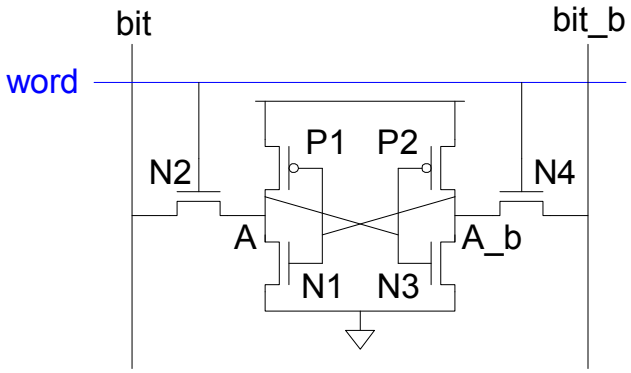



Figure 2: 6T-SRAM cell structure.

**A7** (Please follow the the notes in slides)