CENG 3420 Quiz 2

Name: _____
ID: _____

Q1 [30 points] Pipelined MIPS processor contains 5 stages: IF, ID, EX, MEM, and WB. Pipelline hazards consist of structural hazards, data hazards, and control hazards. The following code is run on a 5-stage MIPS pipeline with full forwarding.

```
lw   $t0, 0($a0)
add  $t0, $t0, 1
sw   $t0, 0($a0)
add  $a0, $a0, 4
```

1. List all the data hazards.
2. Which data hazards can NOT be resolved with forwarding?
3. Rewrite the code to eliminate stalls on the 5-stage pipeline with full forwarding.

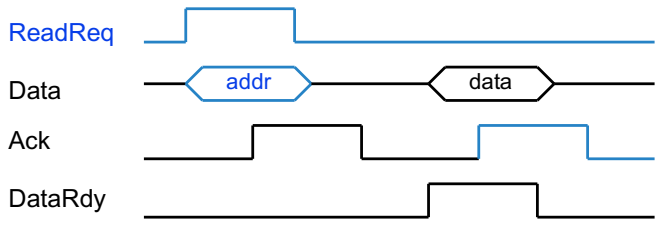
Q2 [20 points] A memory hierarchy includes a TLB and a cache. A memory reference can encounter three different types of misses: TLB miss, page table miss, and cache miss. The following table lists all combinations of three types of misses. Please complete the last colum on whether each combination can actually occur.

TLB	Page Table	Cache	Possible? Under what circumstances?
Hit	Hit	Hit	
Hit	Hit	Miss	
Hit	Miss	Hit	
Hit	Miss	Miss	
Miss	Hit	Hit	
Miss	Hit	Miss	
Miss	Miss	Miss	
Miss	Miss	Hit	

Q3 [30 points] In a direct mapped cache with **16KB** of data and **4**-word blocks, assume an address is 32-bits. (Note: KB = kilobyte)

1. In an address, what's the size of `index` field?
2. In an address, what's the size of `tag` field?
3. In a cache block there are 4 words. What's the size of one cache block?

Q4 [20 points] Considering a scenario that data is transferred from memory to I/O devices. Complete the following Asynchronous Bus Handshaking Protocol.



1. I/O device requests by raising `ReadReq` & putting addr on the data lines
2.
3.
4.
5.
6.
7.