CENG3420 Computer Organization & Design
Lecture 11 Review: Multi-Issue Processor

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Data Dependencies

As known as data hazards in instruction scenario

- Read After Write (RAW): **true** data dependency

```
R2 <- R1 + R3
R4 <- R2 + R3
```

- Write After Read (WAR): **anti**-dependency

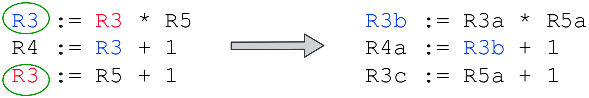
```
R4 <- R1 + R5
R5 <- R1 + R2
```

- Write After Write (WAW): **output** dependency

```
R2 <- R4 + R7
R2 <- R1 + R3
```

Resolve Data Dependencies

- True dependencies (RAW) represent the flow of data and information through a program
- Anti-dependency (WAR) & output dependency (WAW) arise because the limited number of registers, i.e., programmers reuse registers for different computations leading to storage conflicts
- Storage conflicts can be reduced (or eliminated) by increasing or duplicating the troublesome resource (i.e., register renaming)



```
R3 := R3 * R5
R4 := R3 + 1
R3 := R5 + 1
```

```
R3b := R3a * R5a
R4a := R3b + 1
R3c := R5a + 1
```

- In above example, through register renaming, WAR (red font) & WAW (green circle) can be resolved

Thanks. For any question:

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