

# CENG 3420 Homework 2 Solutions

**Due:** Mar. 14, 2016

- A1**
1. Uses the clock cycle inefficiently the clock cycle must be timed to accommodate the slowest instruction.
  2. May be wasteful of area since some functional units (e.g., adders) must be duplicated since they can not be shared during a clock cycle.

(6 points for one correct statement, 8 points for both) [8 points]

inst	PCSrc	ALUSrc	ALUOp	MemWrite	MemRead	MemToReg	RegDst	RegWrite
lw	0	1	add	0	1	1	0	1

inst	PCSrc	ALUSrc	ALUOp	MemWrite	MemRead	MemToReg	RegDst	RegWrite
lw	0	0	add	0	1	1	1	1

**A2** (1 point for one correct answer) [14 points]

**A3** The 5 stages are:

- IF : Fetch instruction from memory.
- ID : Read registers while decoding the instruction. The regular format of MIPS instructions allows reading and decoding to occur simultaneously.
- EX : Execute the operation or calculate an address.
- MEM : Access an operand in data memory.
- WB : Write the result into a register.

(2 points for one correct statement) [10 points]

**A4** Pipeline clock cycle is determined by the slowest stage.

1. 210ps, 780ps (3 points for one correct answer, 5 points for both) [5 points]
2.  $5 \times 210\text{ps} = 1050\text{ps}$ , 780ps (3 points for one correct answer, 5 points for both) [5 points]
3. MEM. 200ps. (3 points for one correct answer, 5 points for both) [5 points]

**A5** In the 5-stage MIPS pipeline: IF ID EX MEM WB. With full forwarding, we can resolve all data-hazards except load-use hazards

1. The load-use hazard between the first two instructions cannot be resolved with forwarding.

2.

```
lw    $t0, 0($a0)
addi  $a0, $a0, 4
addi  $t0, $t0, 1
sw    $t0, 0($a0)
```

(5 points for each subproblem) [10 points]

**A6** 1. 4 [5 points]

2. I, J, B[J][0] (3 points for 1 correct answer, 4 points for 2, 5 points for 3) [5 points]

3. A[J][I] [5 points]

**A7** 1.  $2^6/4 = 16$  words [4 points]

2.  $2^6 = 64$  [4 points]

3.  $1 + 20/(64*8) = 1.039$  (2 points for the process, 2 points for the answer) [4 points]

**A8** 1. Every 16 access, there's 1 miss.  $1/16 = 0.062500$ ; Not sensitive to cache size and working set; Compulsory. (3 points for the process, 2 points for the answer)[5 points]

2. Miss rates are:  $2/16$ ,  $2/64$  and  $2/128$ . Spatial. (3 points for the process, 2 points for the answer) [5 points]

3. close to zero as the next entry is always brought to cache before accessing it. (4 points for the process, 2 points for the answer) [6 points]