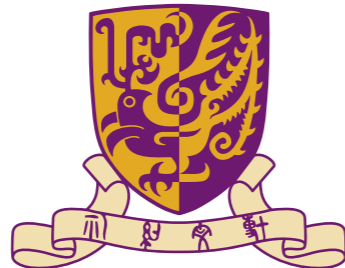# CENG 4480
Lecture 10: Clock

Bei Yu

Reference:
- Chapter 11 Clock Distribution
- **High speed digital design**
- by Johnson and Graham

香港中文大學
The Chinese University of Hong Kong

Setup Time and Time Margin

- Setup Time: The time that the input data must be stable before the clock transition of the system occurs

- Time Margin: measures the **slack**, or excess time, remaining in each clock cycle
  - ✦ Protects your circuit against signal cross-talk, miscalculation of logic delays, and later minor changes in the layout
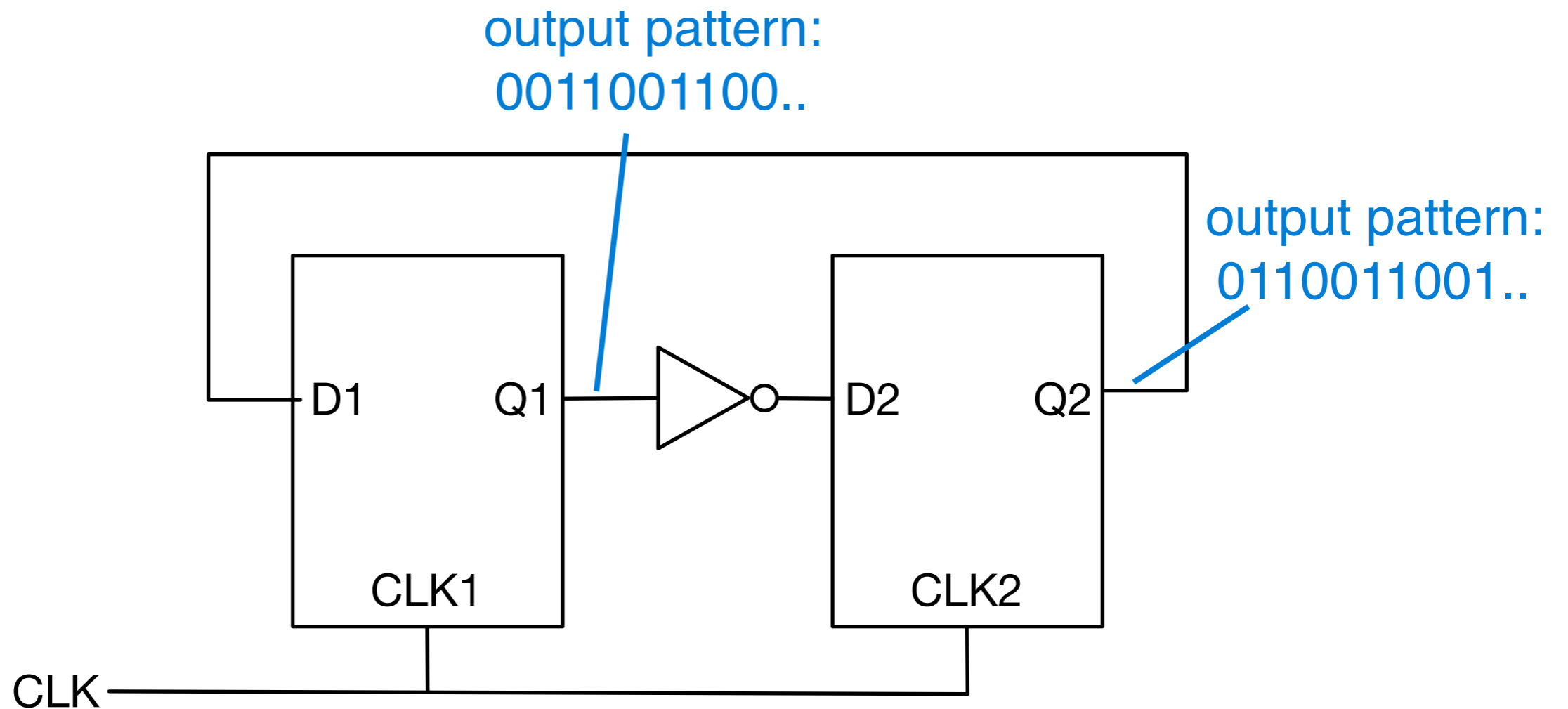 - ✦ Depends on both time delay of logic paths and clock interval

A 2-bit ring counter example

- 2-bit ring counter
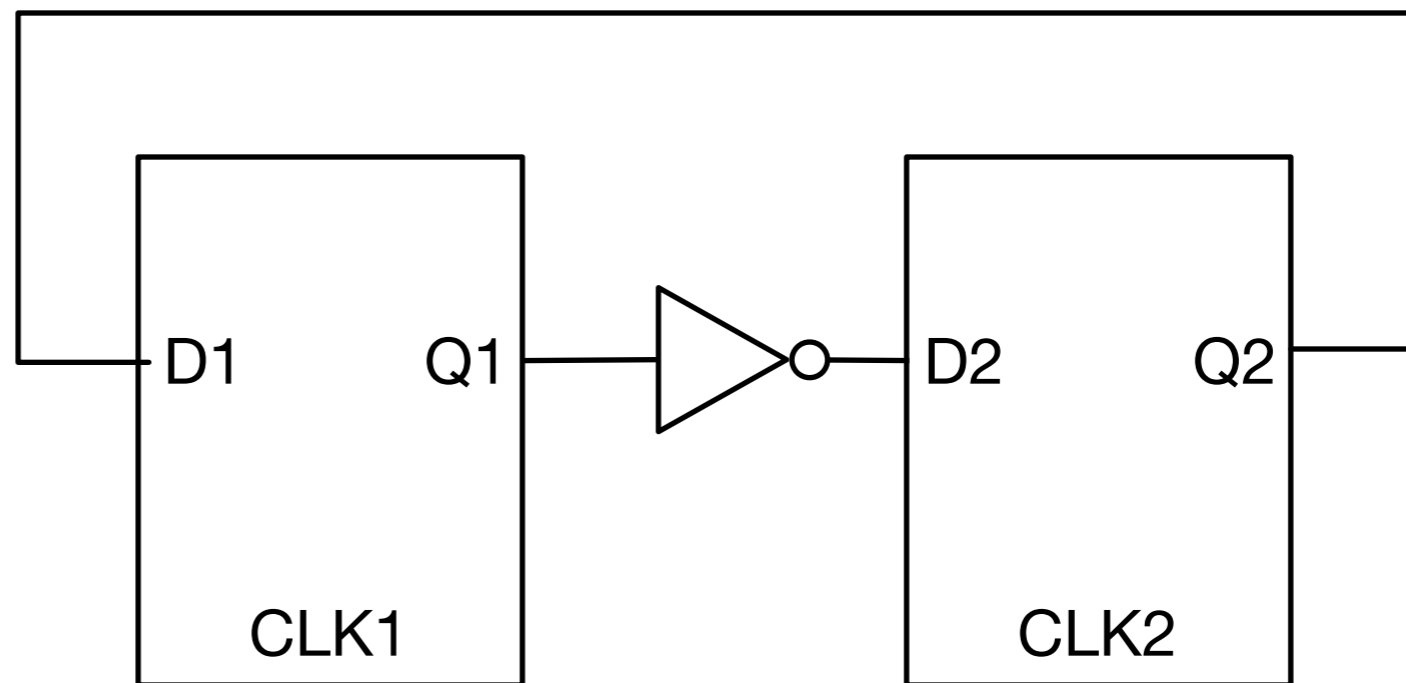
- Initially A = B = 0; A = 0011001100
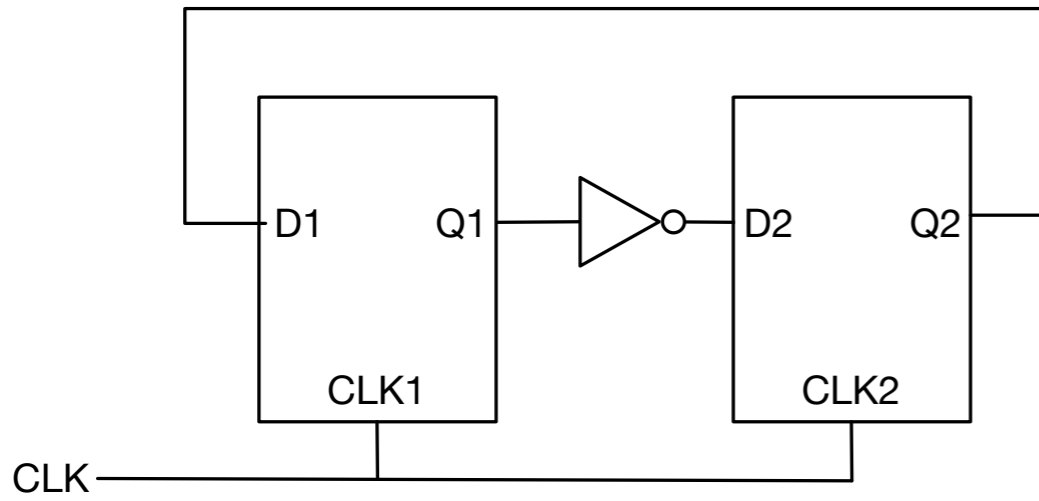
- What is B?
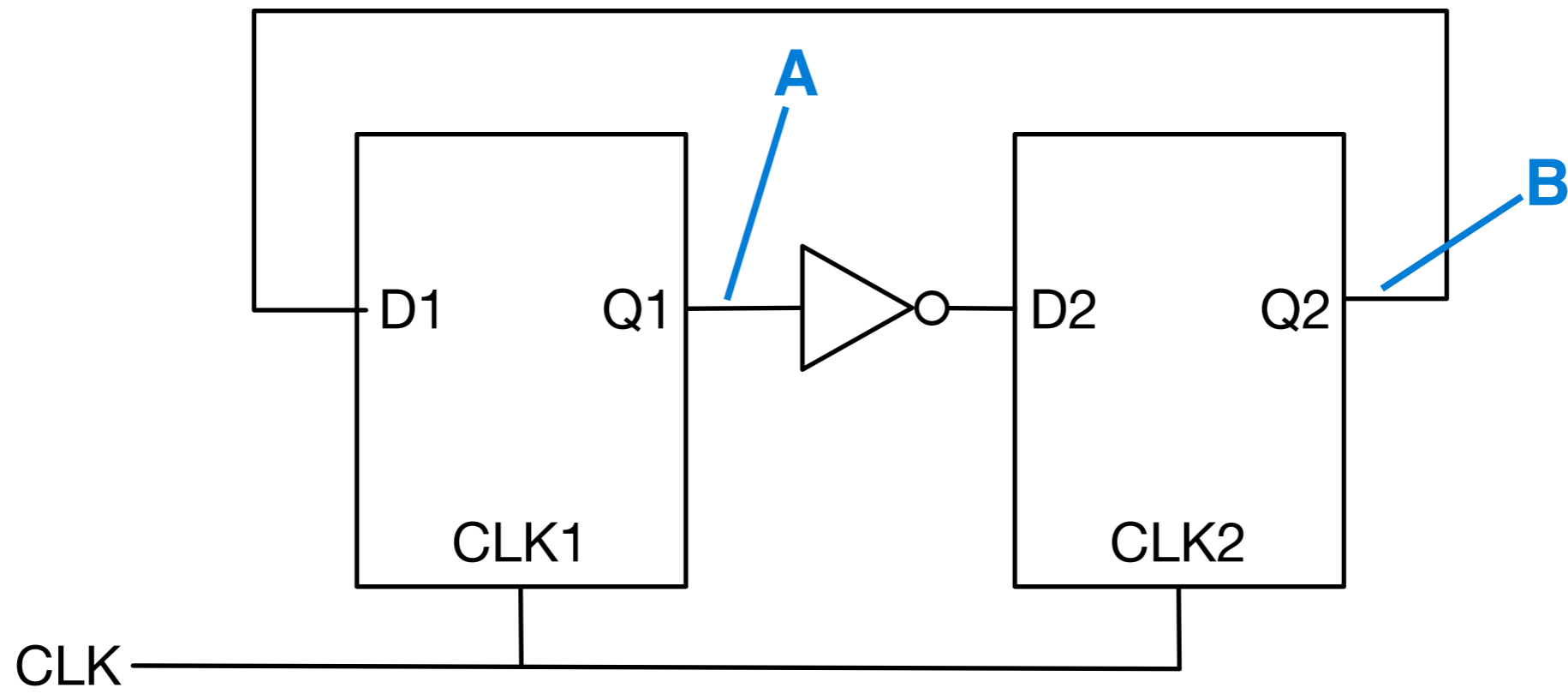
A 2-bit ring counter example

- The result is Okay when clock is slow

- But, when clock is TOO fast, get some problem

output pattern:
0011001100..

output pattern:
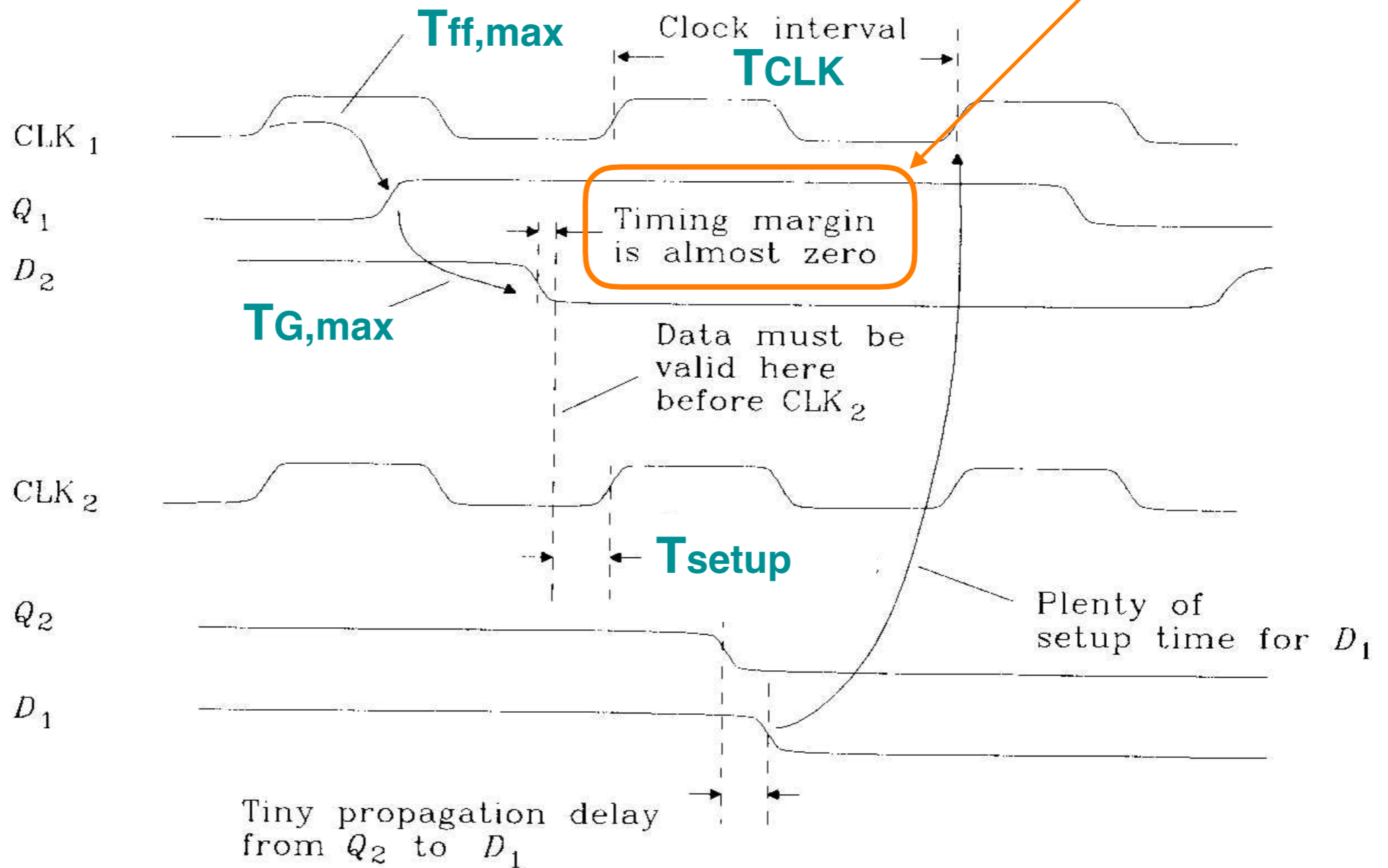0110011001..

D1   Q1   ▷○   D2   Q2

CLK1   CLK2

CLK

Notations in Clock Skew Calculation

- $T_{ff,max}$: max delay of flip-flop (FF)

- $T_{G,max}$: max delay of gate G, including track delay

- T_{setup}: worst-case setup time required by FF2, data at D2 must arrive at least T_{setup} before CLK_2

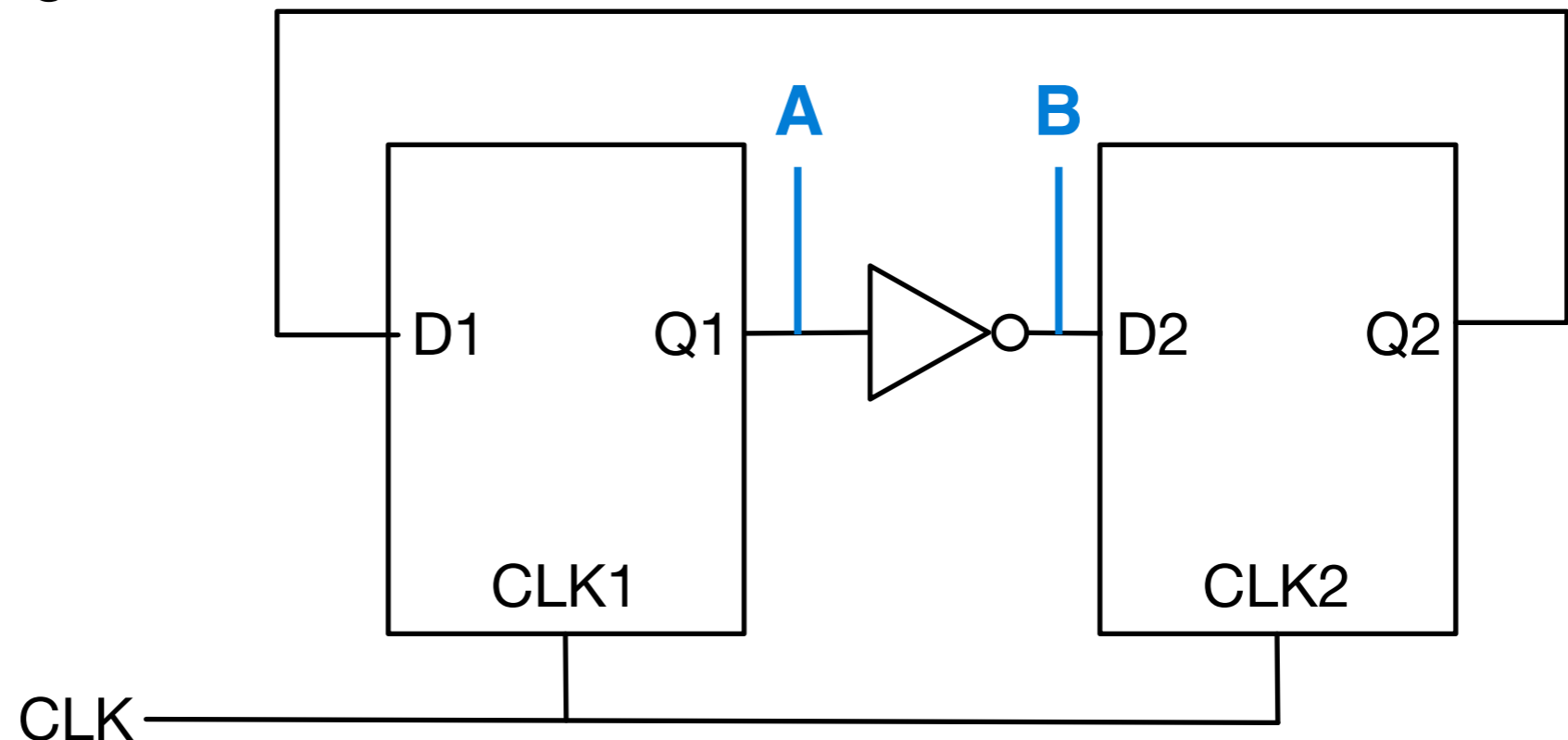- T_{CLK}: clock period; interval between clocks

May cause problem if T_{CLK} is too small

Clock interval

$T_{ff,max}$

T_{CLK}

CLK$_1$

Q_1

D_2

$T_{G,max}$

Timing margin is almost zero

Data must be valid here before CLK$_2$

CLK$_2$

T_{setup}

Q_2

Plenty of setup time for D_1
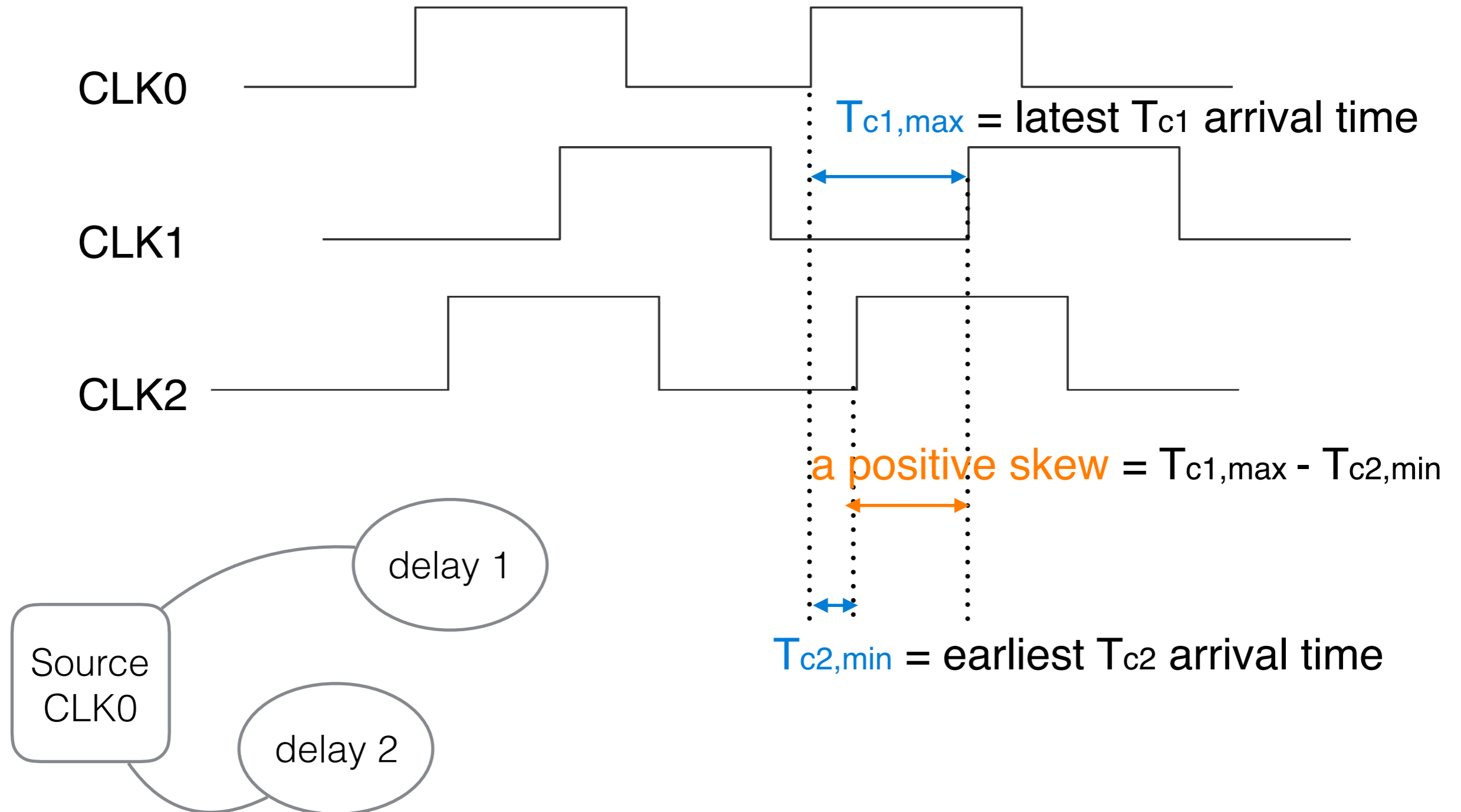
D_1

Tiny propagation delay from Q_2 to D_1

EX. B2-1

- CLK1 = CLK2 = 20MHz; $T_{ff,max}$ = 8ns; T_{setup} = 5ns; $T_{G,max}$ = 10ns.

- **Questions**:

  - Find time margin

  - How many delay G gates can you insert between A and B without creating error?

Clock Skew

- The clock does NOT reach FF1, FF2 at the same time

$T_{c1,max}$ = latest T_{c1} arrival time

a positive skew = $T_{c1,max}$ - $T_{c2,min}$

$T_{c2,min}$ = earliest T_{c2} arrival time
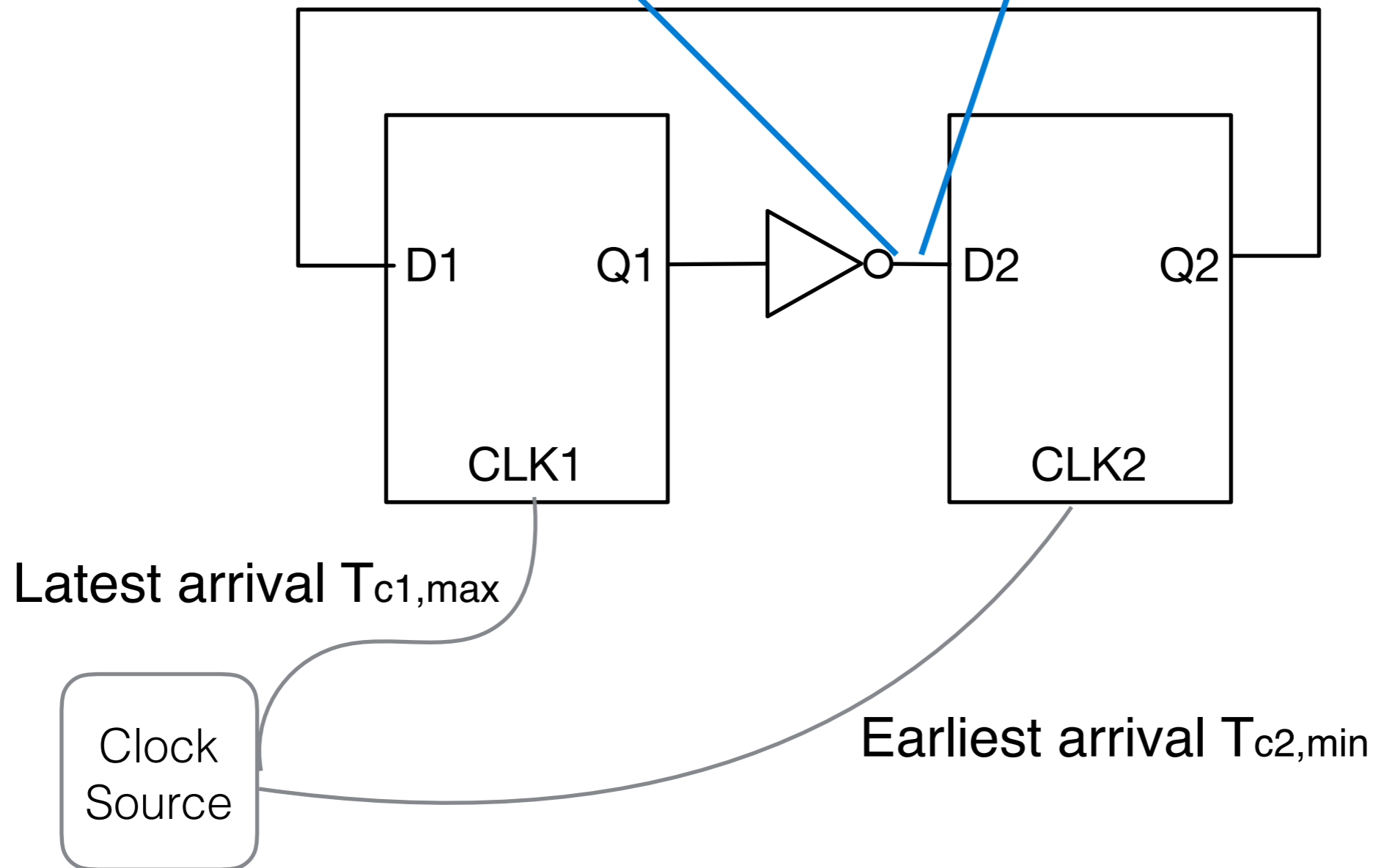
CLK0

CLK1

CLK2

delay 1

Source CLK0

delay 2

Why Care Clock Skew?

Signal arrives here no later than

$T_{c1,max} + T_{ff,max} + T_{G,max}$

Signal arrives must be valid before next clock

$T_{CLK} + T_{c2,min} - T_{setup}$

D1   Q1

CLK1

D2   Q2

CLK2

Latest arrival $T_{c1,max}$

Clock Source

Earliest arrival $T_{c2,min}$

Why Care Clock Skew?

- $T_{slow} = T_{c1,max} + T_{ff,max} + T_{G,max}$

- $T_{required} = T_{CLK} + T_{c2,min} - T_{setup}$

- Since $T_{slow} < T_{required}$ =>

$$T_{CL} > T_{ff,max} + T_{setup} + T_{G,max} + T_{c1,max} - T_{c2,min}$$

Constant
Delay

Logic
Delay
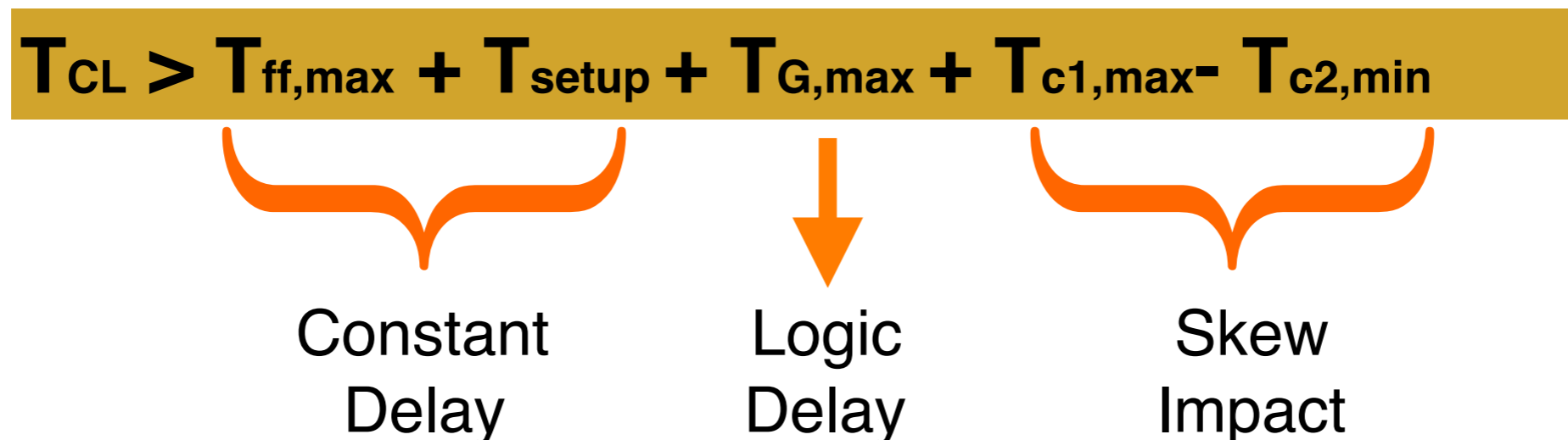
Skew
Impact

EX. B2-2

Question: Given

- $T_{ff,max}$ = 7ns;

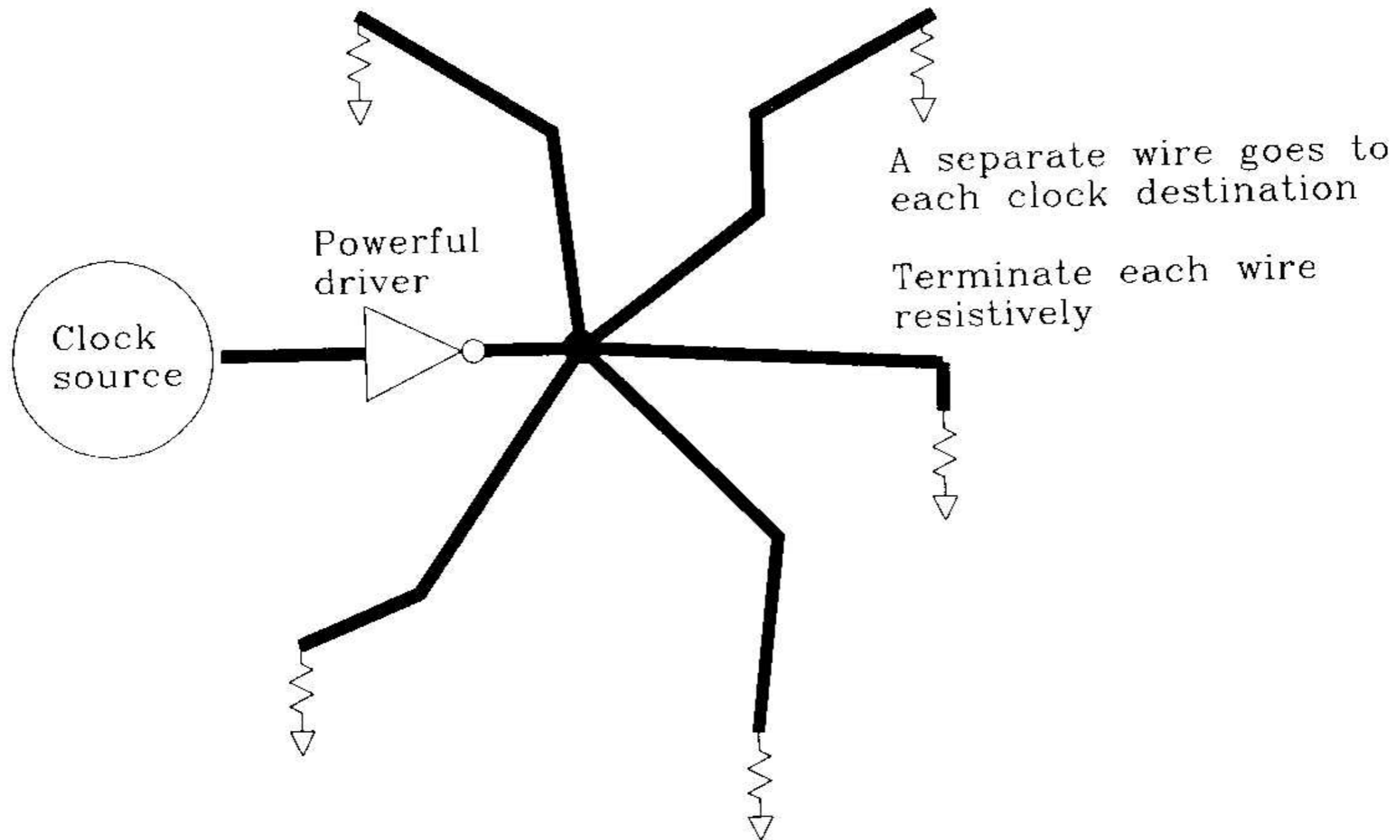- $T_{G,max}$ = 5ns;

- T_{setup} = 4ns;

- T_{CL} = 40MHZ;

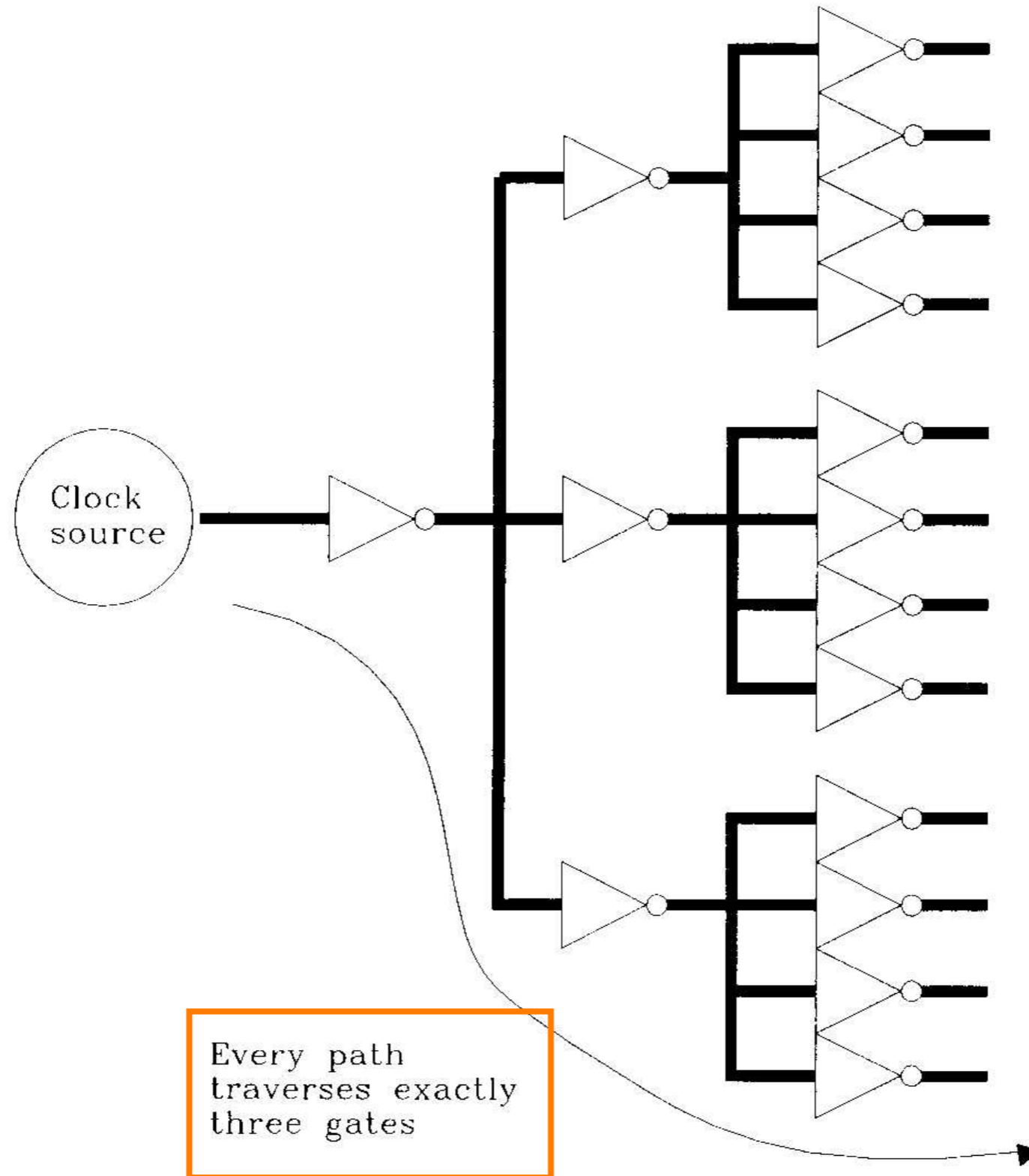What's the biggest time skew allowed?

Answer:

Strategies to reduce clock skew

- Drive them from the same source & balance the delays

- Style 1: Spider-leg distribution network
  - ✦ use a power driver to drive N outputs.
  - ✦ Use load (R) termination to reduce reflection if the traces are long (distributed circuit). Total load =R/N.
  - ✦ Two or more driver outputs in parallel may be needed.
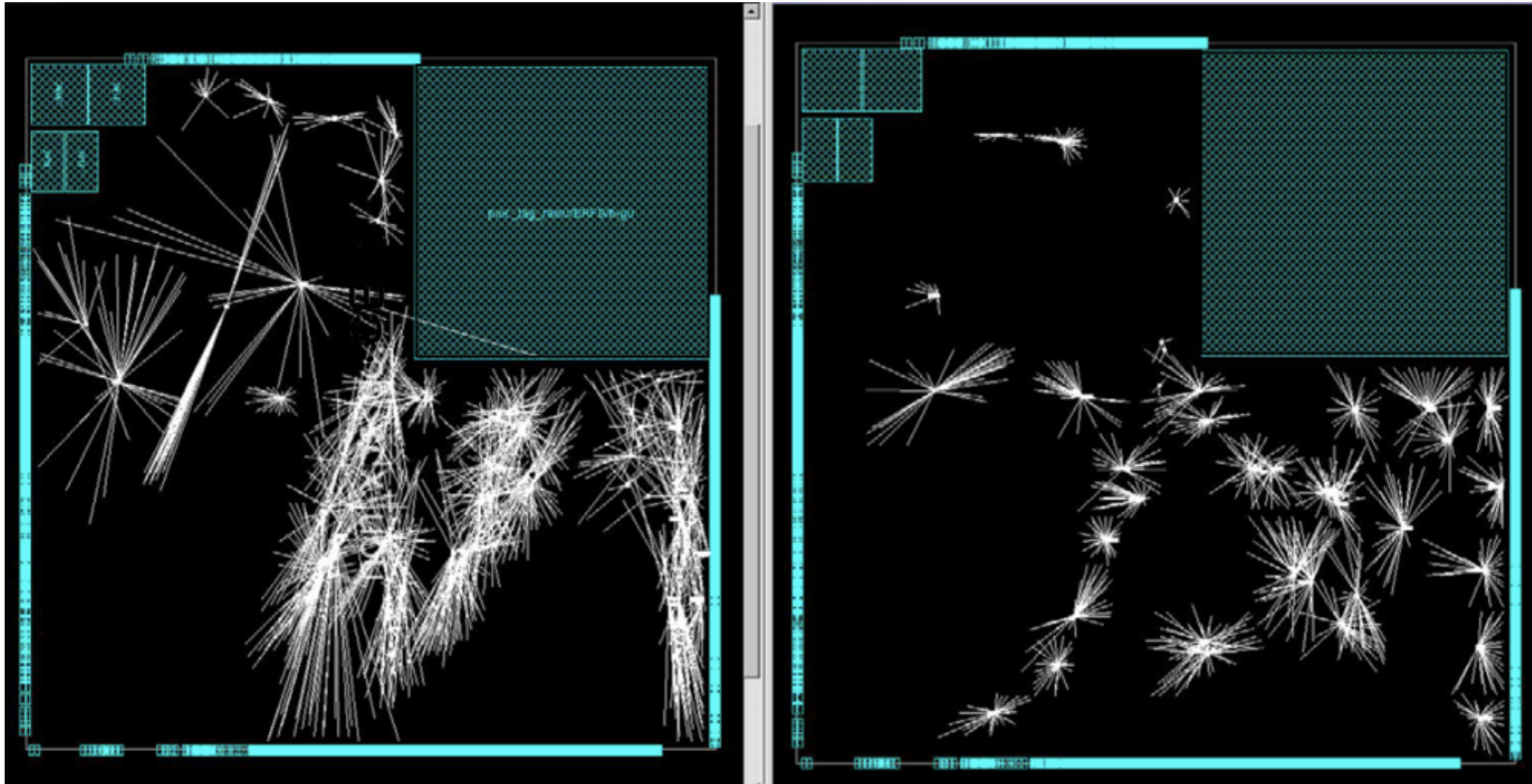
- Style 2: Clock distribution tree

Style 1: Spider-leg Clock

Clock source

Powerful driver

A separate wire goes to each clock destination

Terminate each wire resistively

Style 2: Clock Tree

Clock source

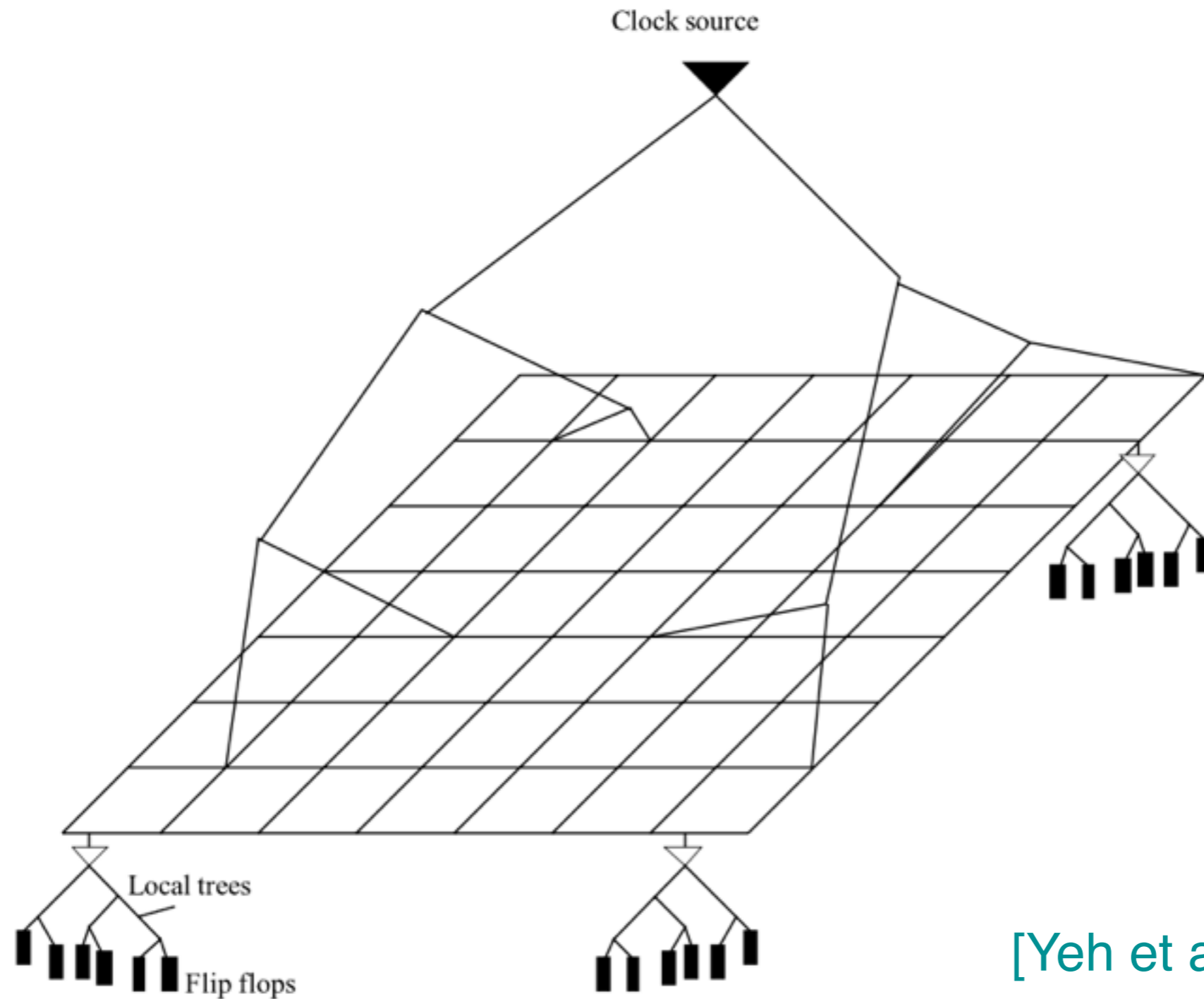Every path traverses exactly three gates

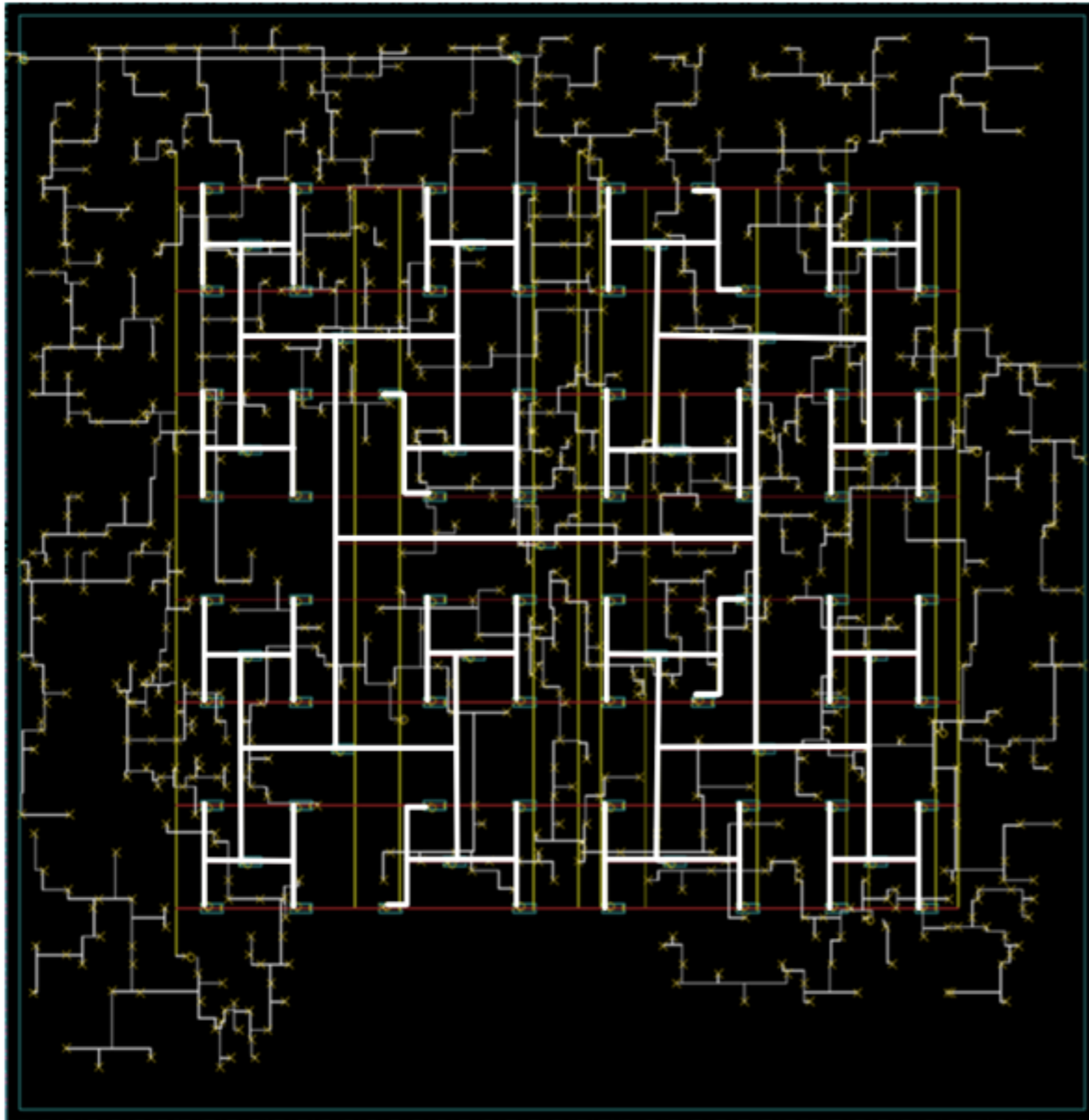# Modern Clock Design — 1

[Ho et al, ISPD'2009]

Modern Clock Design — 2

[Yeh et al, ISQED'2006]

Modern Clock Design — 3

[Seok et al, ISLPED'2010]
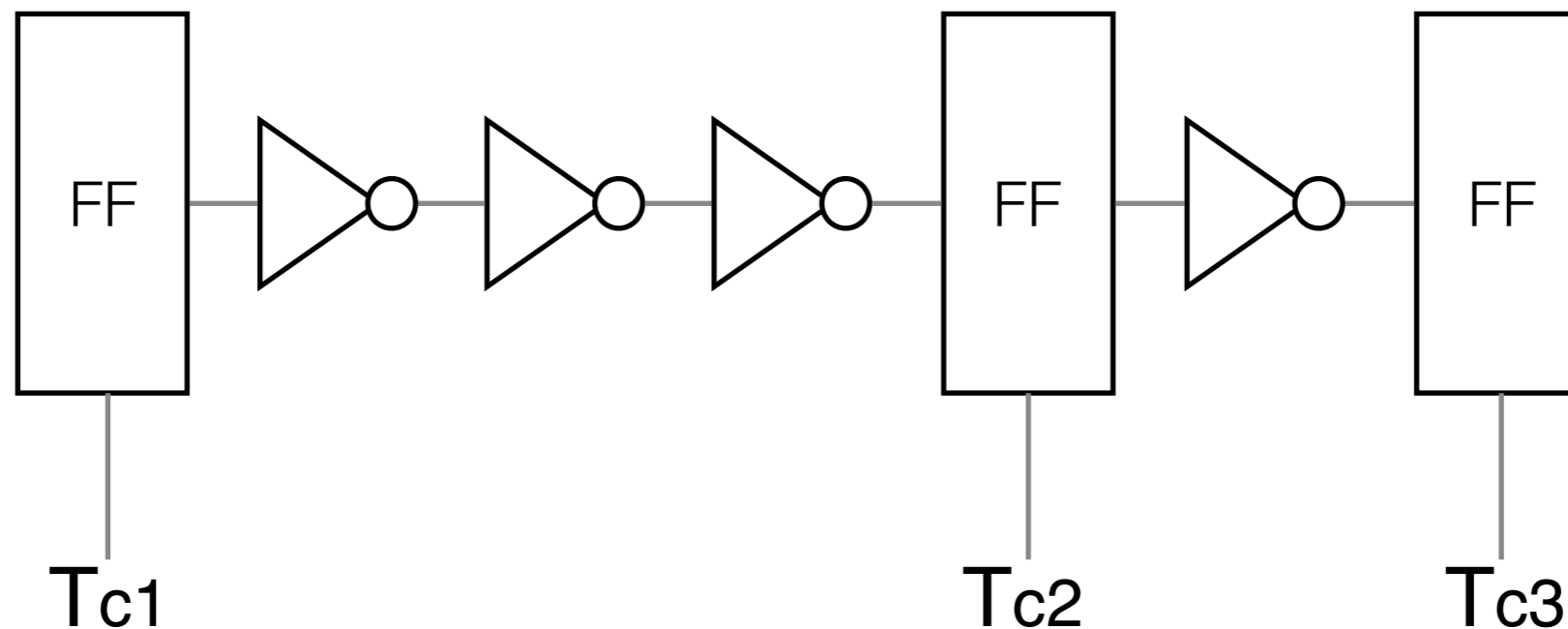
Clock Skew Distribution

325 um / unit

In X and Y Dimension
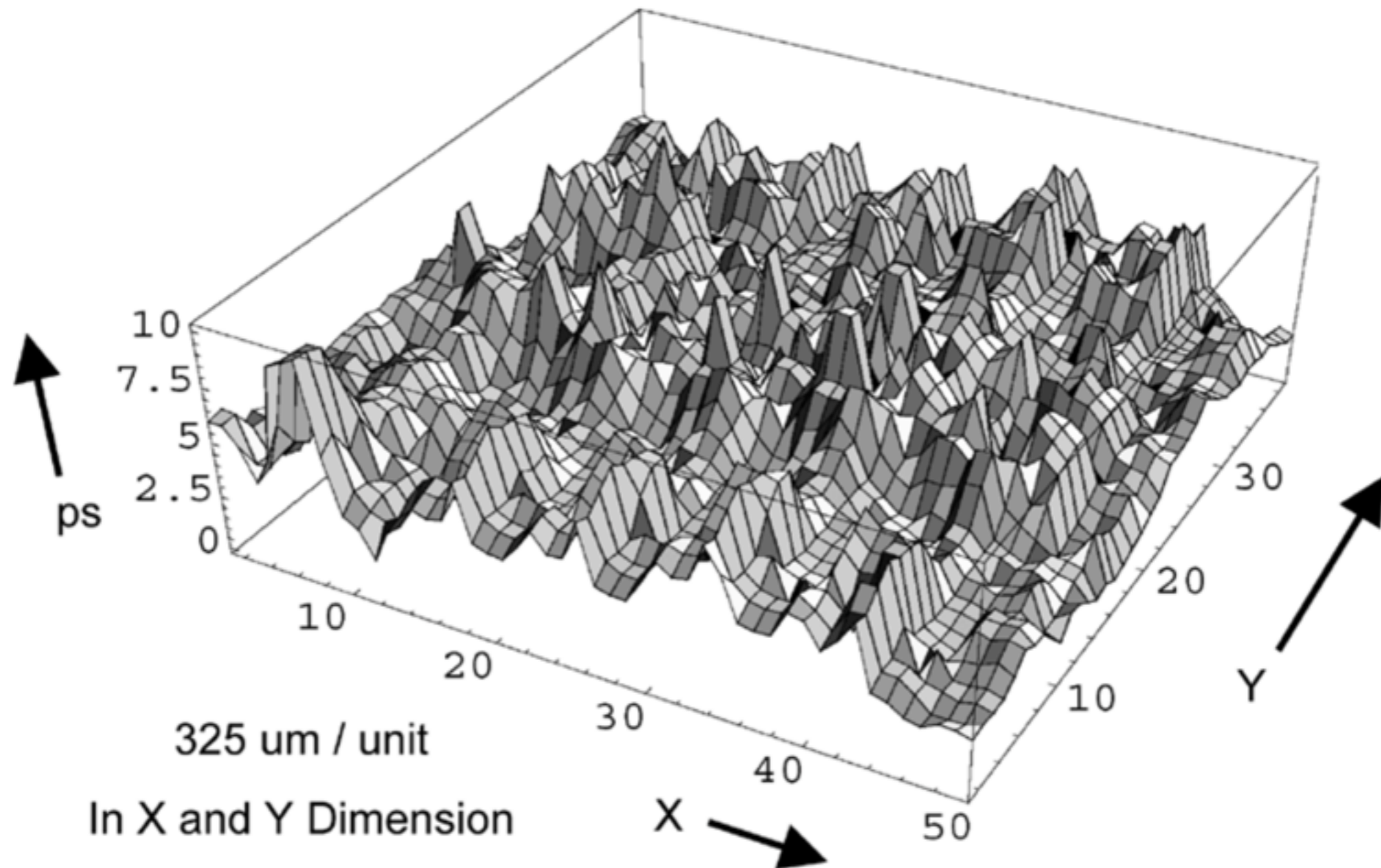
[Pham et al, JSSC'2006]

EX. Skew Optimization

- Instead of Zero-Skew, take advantage of Skew.

- Question: Given $T_{G,max}=6ns$, $T_{ff,max}=10ns$, $T_{setup}=2ns$, what's the minimal T_{CLK}? Assume $T_{c3} = 0$.

Thank You