CENG4480 Homework 3

Q1 Elaborate and examplify the differences between Combinational and Sequential Circuit.

Q2 What is the modern memory hierarchy? Analysis the properties of each hierarchy level.

Q3 For the given SR Latch Fig. 1. Draw the waveform of Q if S, R, and E(Clk) have the input shown in Fig. 2

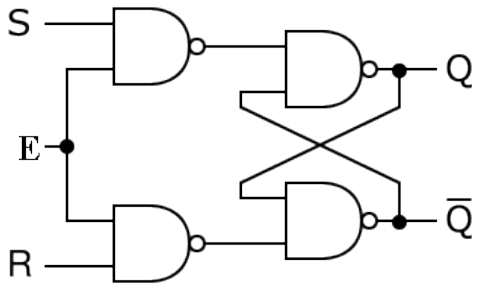

Figure 1: Gated SR Latch

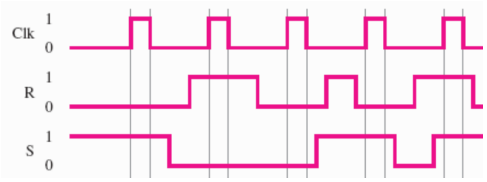

Figure 2: Gated SR Latch

Q4 Show the differences between DRAM and SRAM and which level of hierarchy of memory are they employed.

Q5 Design a finite state machine to detect the pattern of "11010" in the bit stream. How many states are required? Draw the state transition graph.

Q6 (a) What is setup time?
(b) How is clock skew generated? (c) How to alleviate clock skew?

Q7 Explain the working principle of the following register (Fig. 3) and show that the circuit is not sensitive to clock skew.

Q8 Explain cross-talk and approaches to eliminate cross-talk.

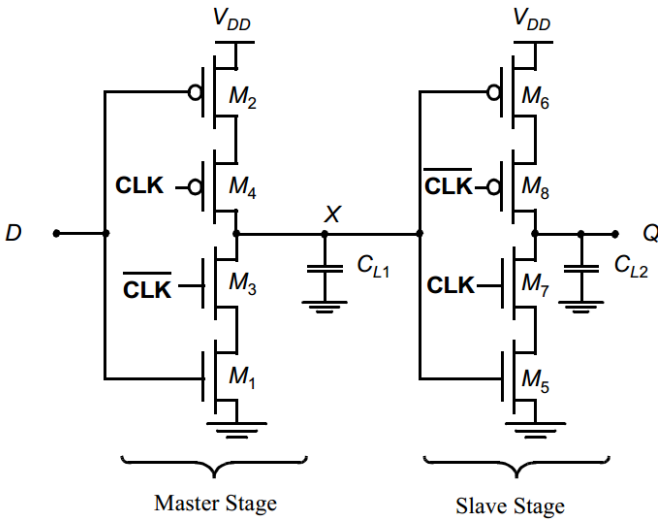

Figure 3: Sample Register.