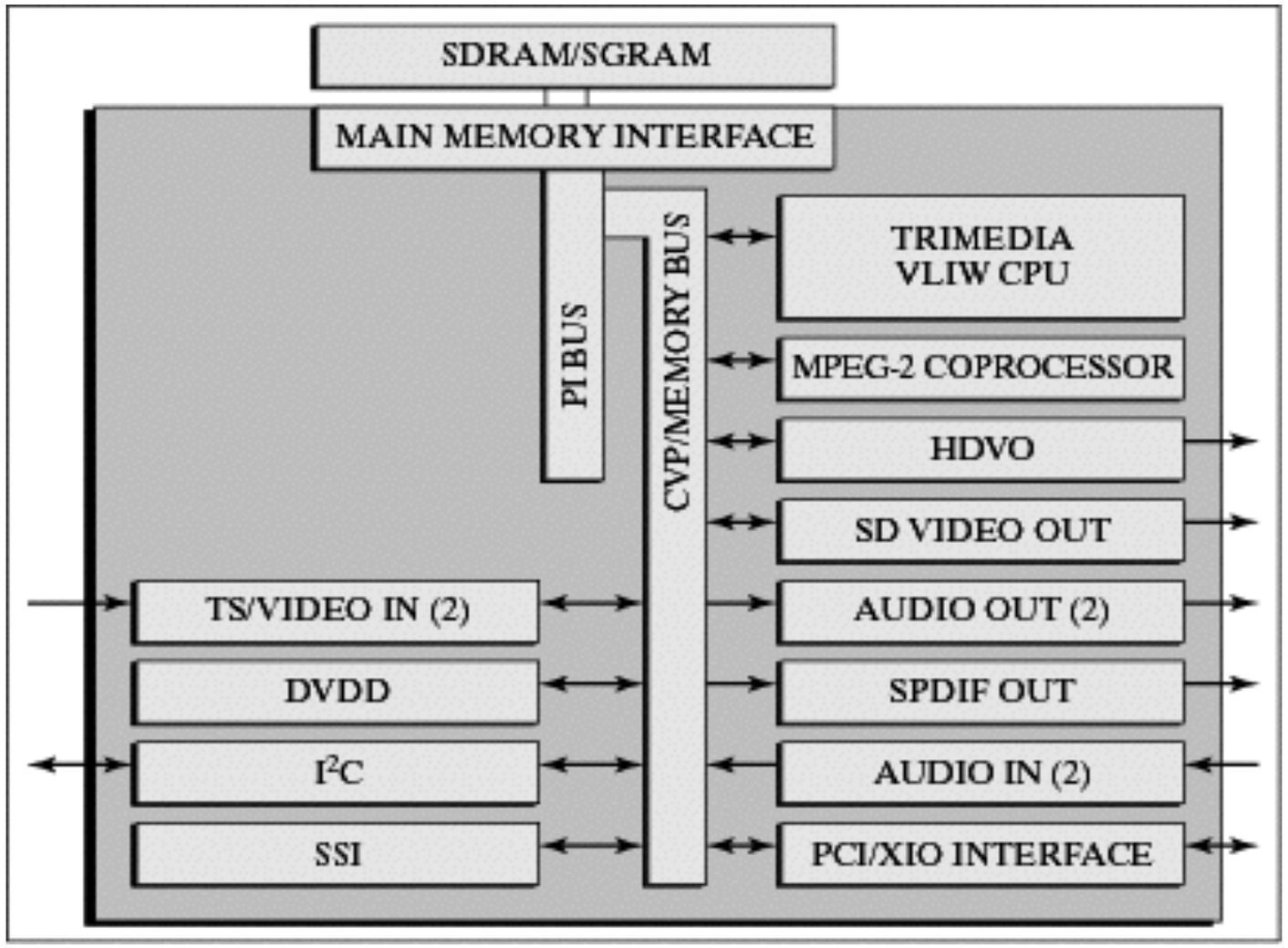
12. Design Styles

Bei Yu

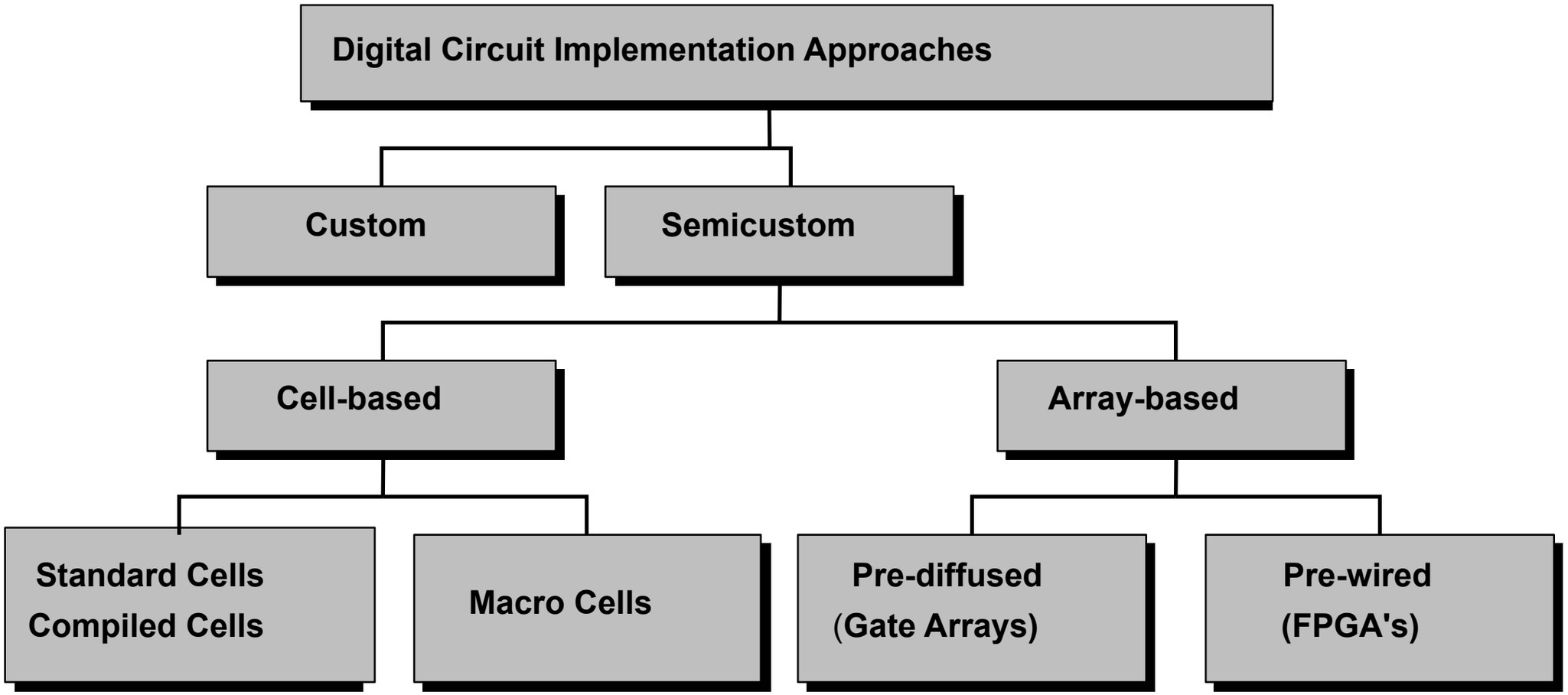
Optional

A System-on-a-Chip: Example

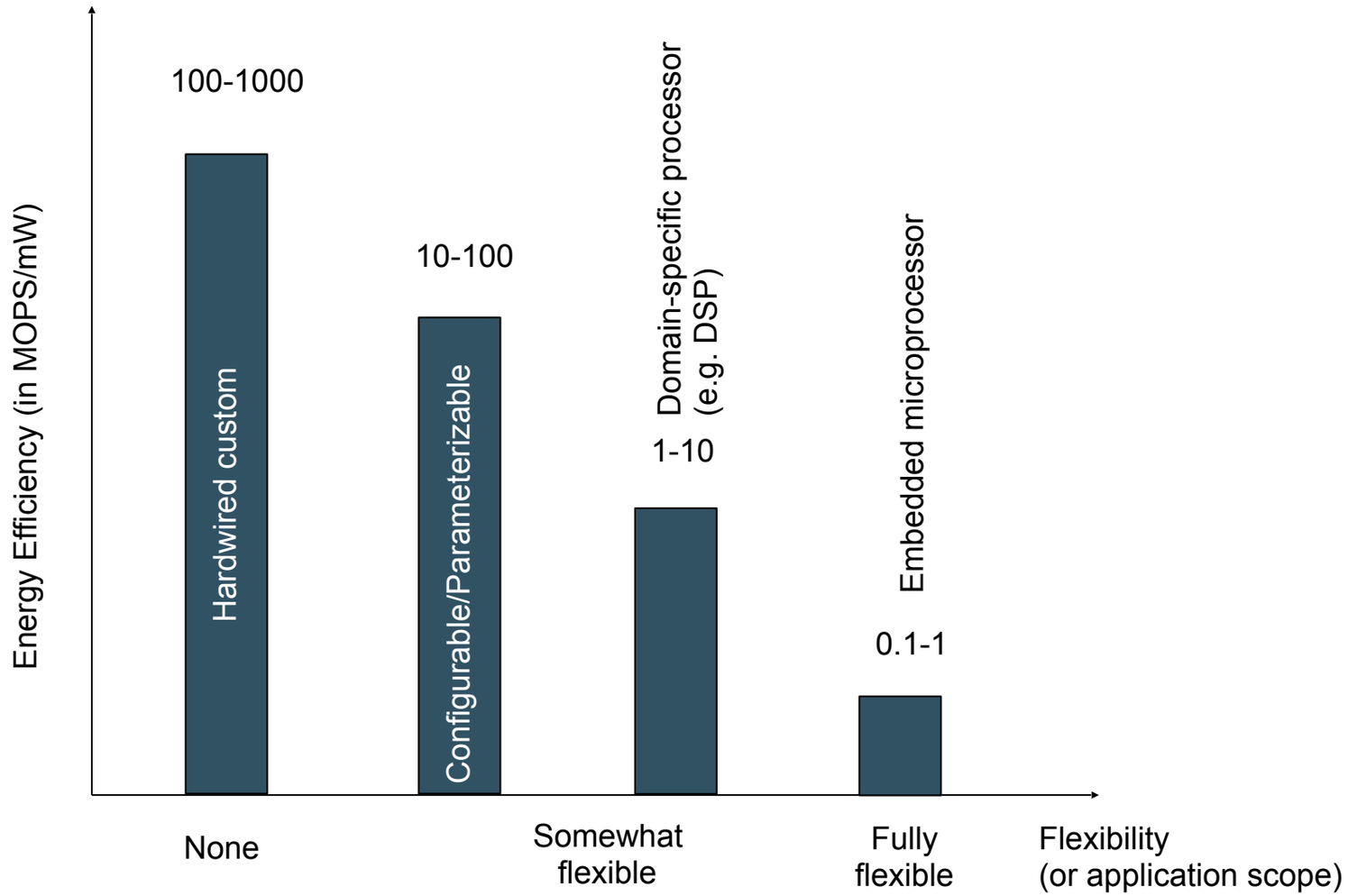


[Courtesy: Philips]

Implementation Choices

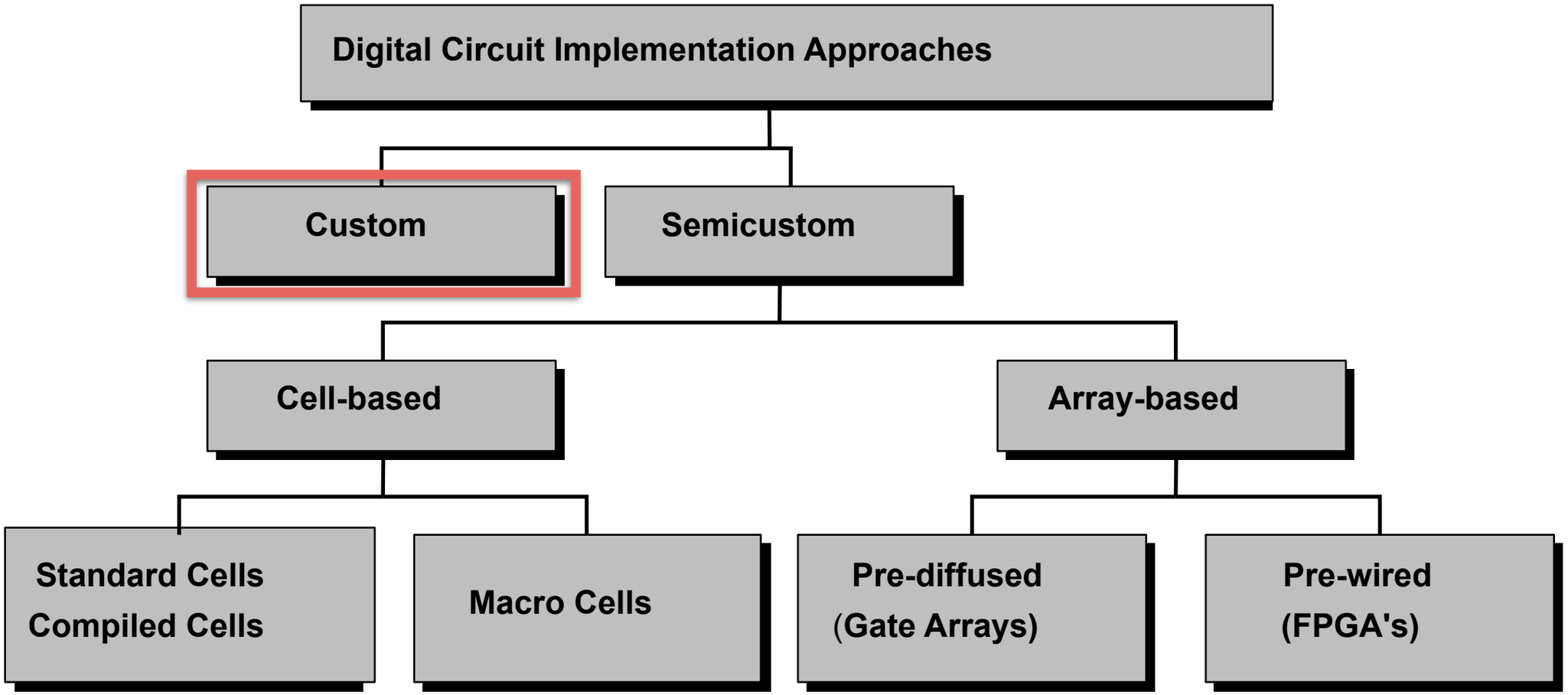


Impact of Implementation Choices



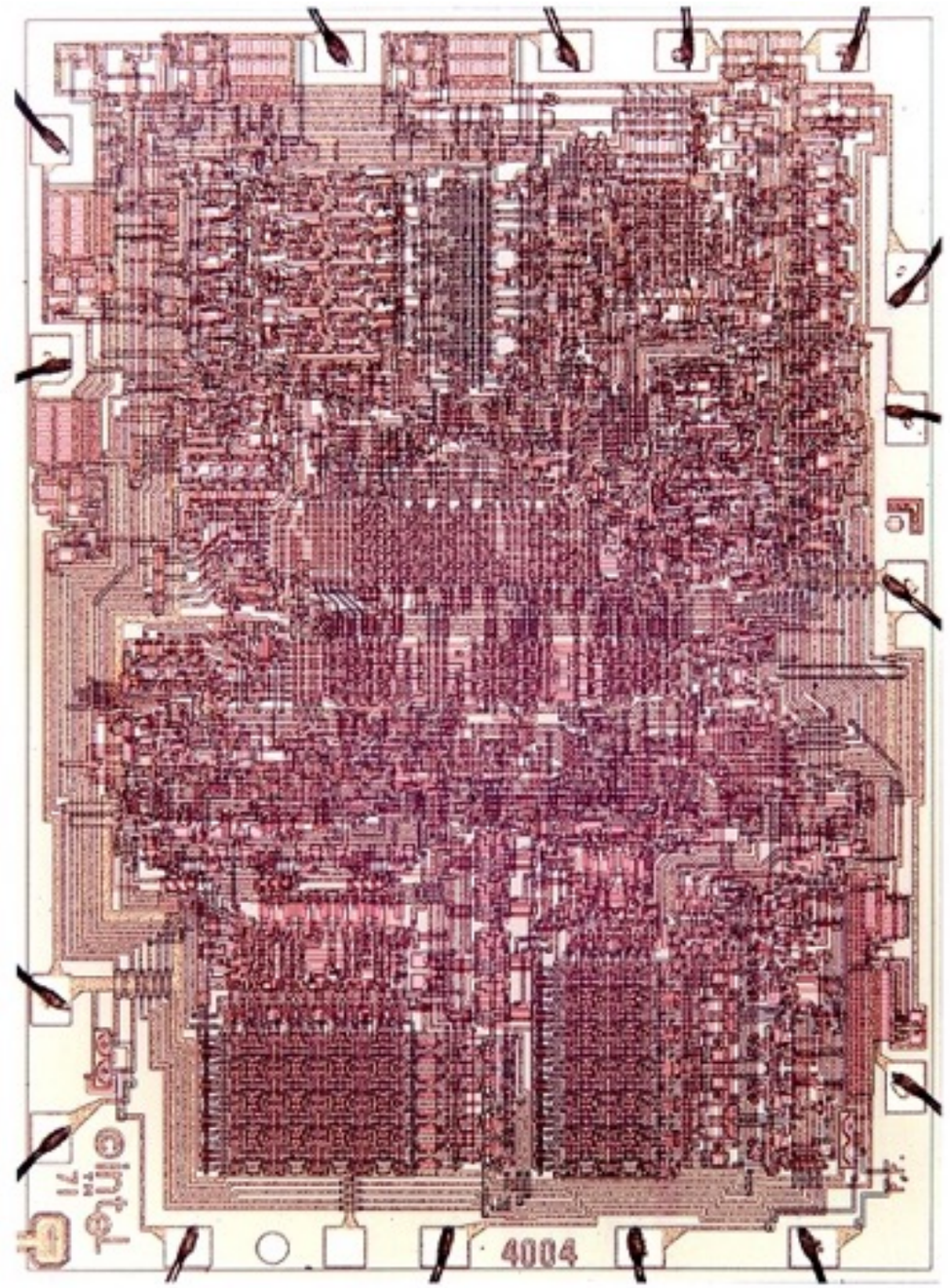
- Higher custom level, higher energy efficiency
- Higher custom level, lower design efficiency

The Custom Approach



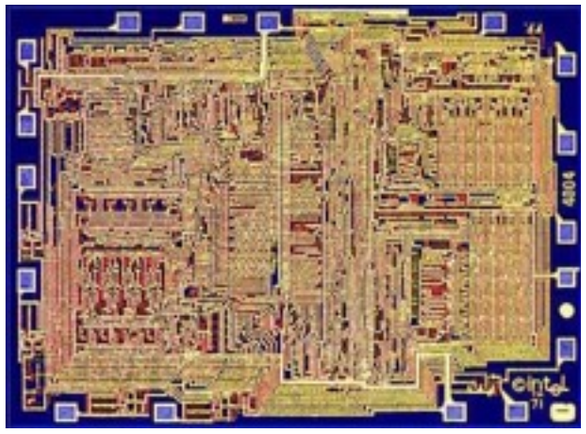
The Custom Approach

- Intel 4004

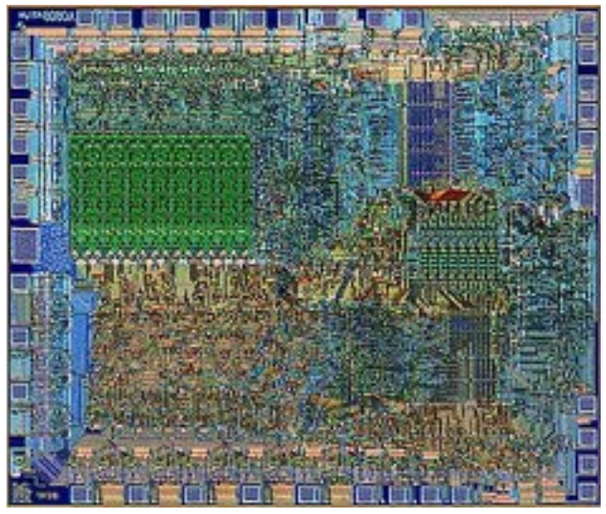


[Courtesy: Intel]

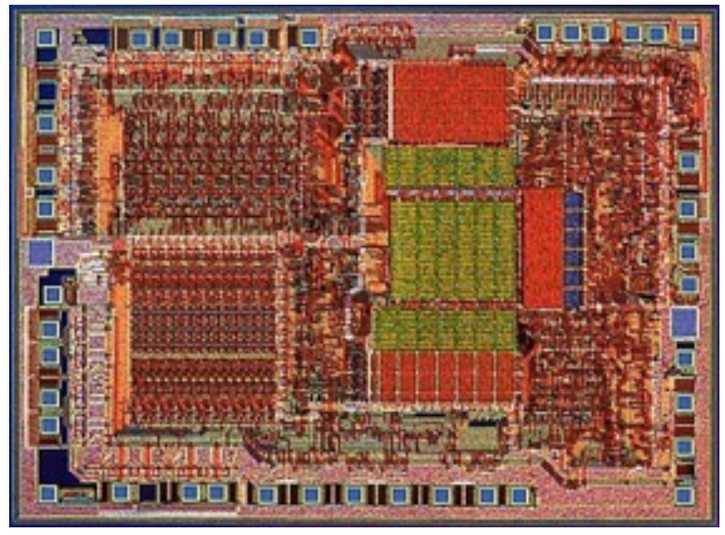
Transition to Automation and Regular Structures



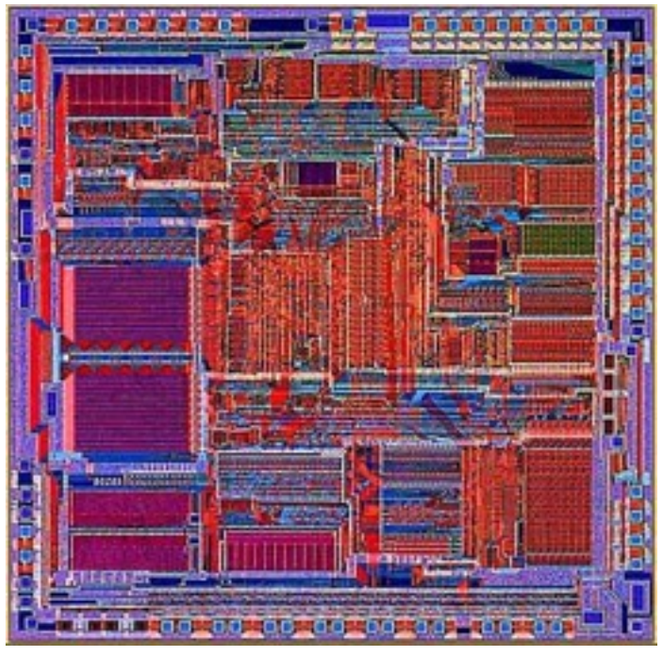
Intel 4004 (‘71)



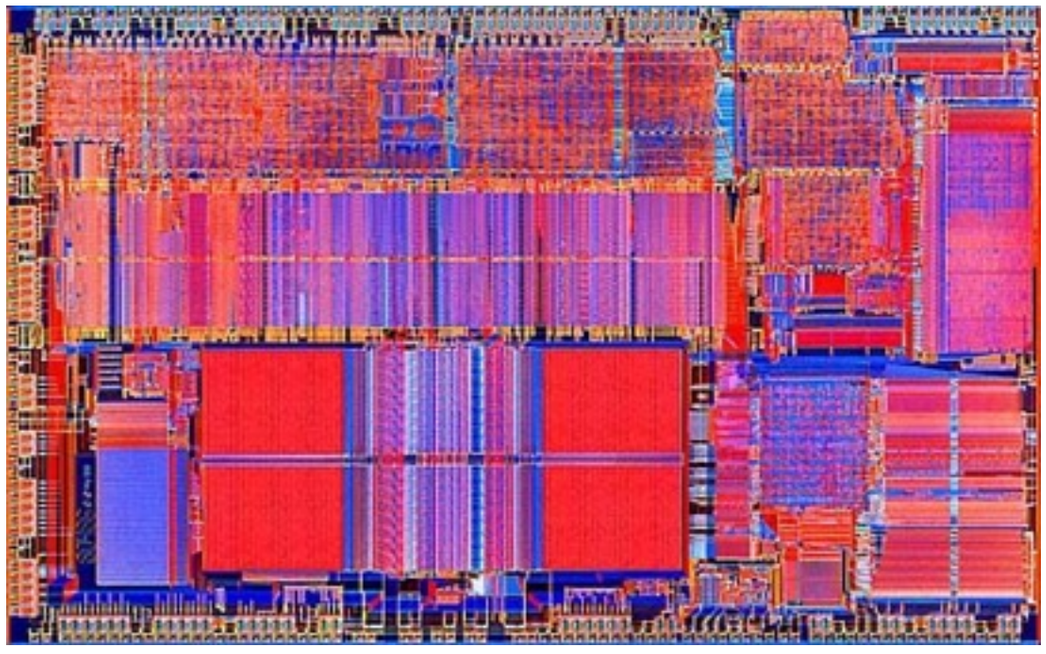
Intel 8080



Intel 8085



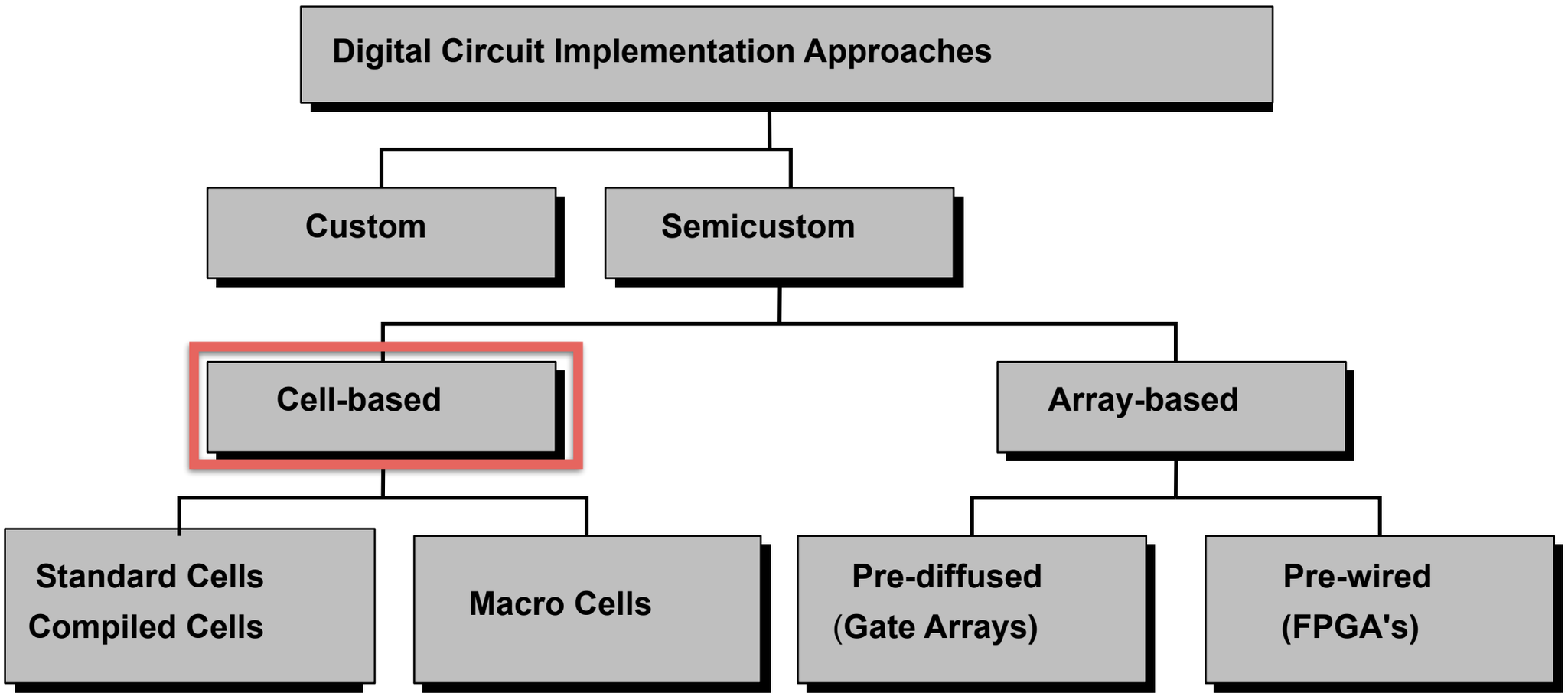
Intel 80286



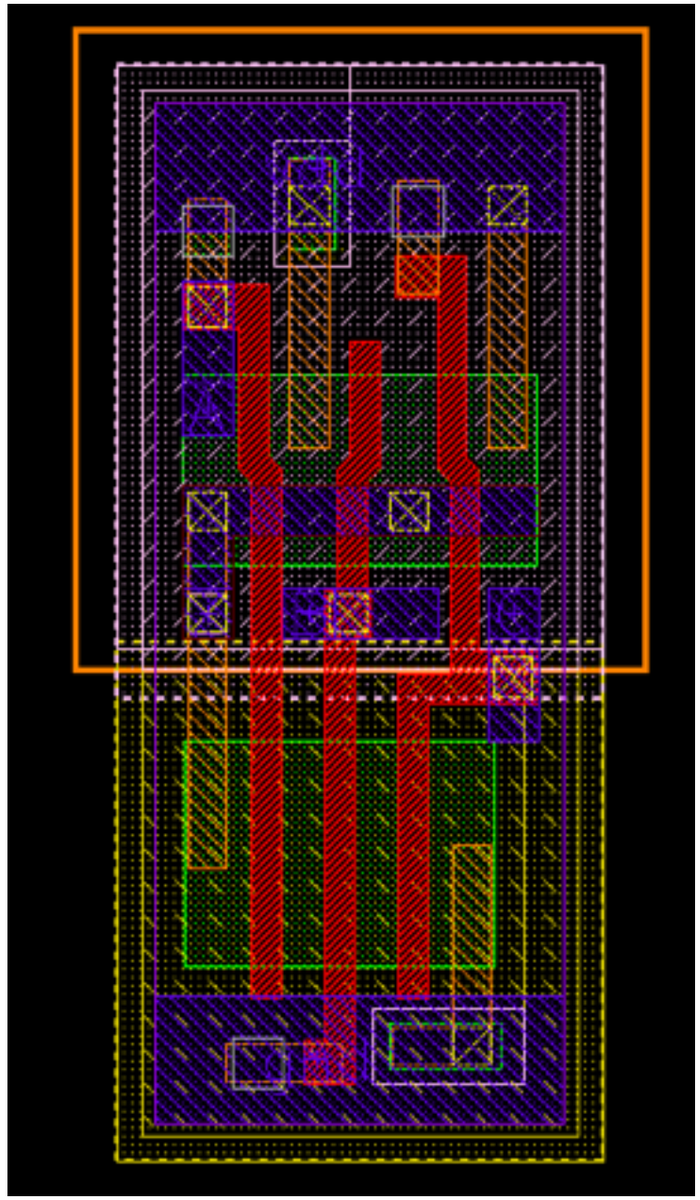
Intel 80486

[Courtesy: Intel]

Cell-based Design



Standard Cell — Example

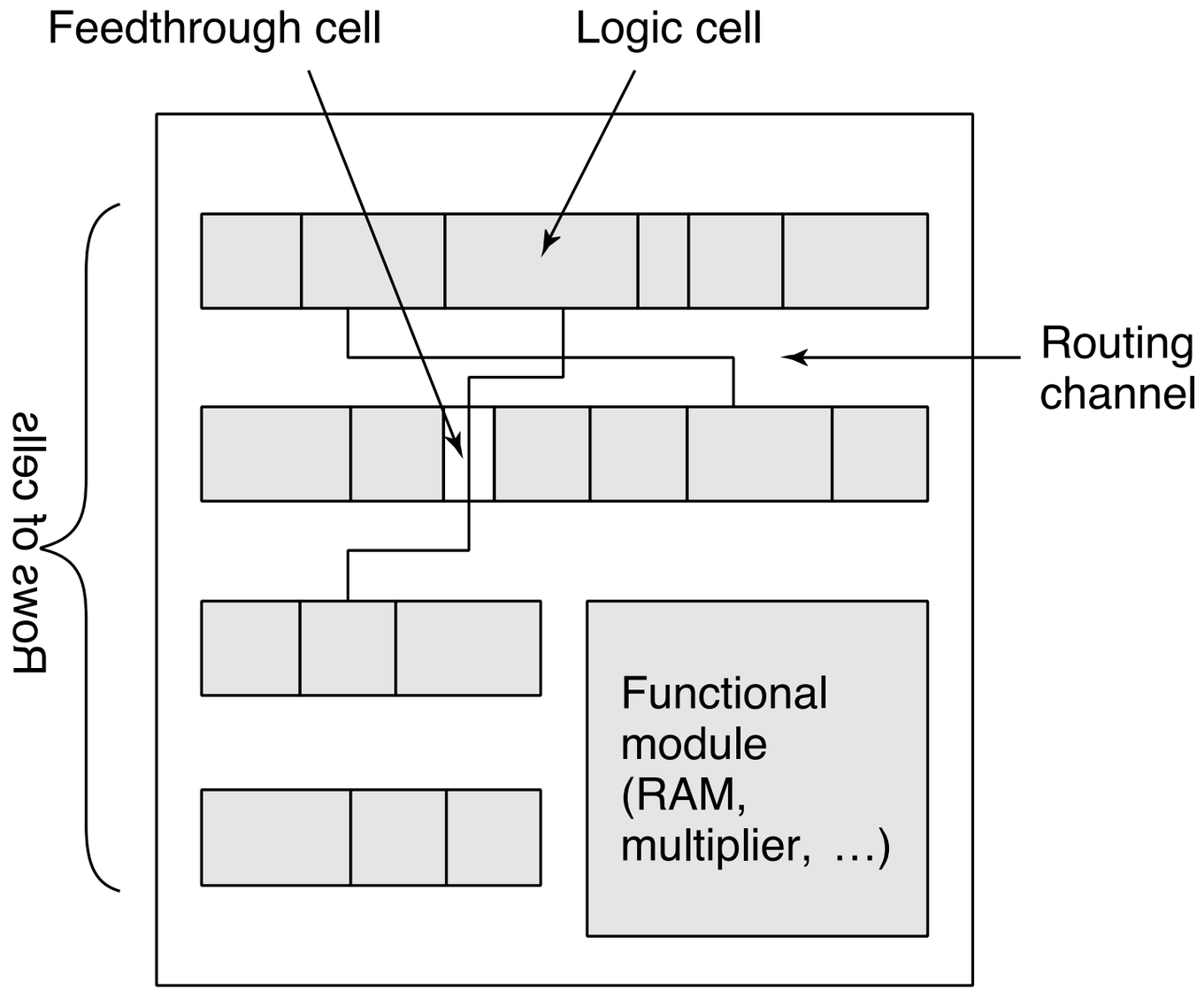


Path	1.2V - 125°C	1.6V - 40°C
$In1—t_{pLH}$	$0.073+7.98C+0.317T$	$0.020+2.73C+0.253T$
$In1—t_{pHL}$	$0.069+8.43C+0.364T$	$0.018+2.14C+0.292T$
$In2—t_{pLH}$	$0.101+7.97C+0.318T$	$0.026+2.38C+0.255T$
$In2—t_{pHL}$	$0.097+8.42C+0.325T$	$0.023+2.14C+0.269T$
$In3—t_{pLH}$	$0.120+8.00C+0.318T$	$0.031+2.37C+0.258T$
$In3—t_{pHL}$	$0.110+8.41C+0.280T$	$0.027+2.15C+0.223T$

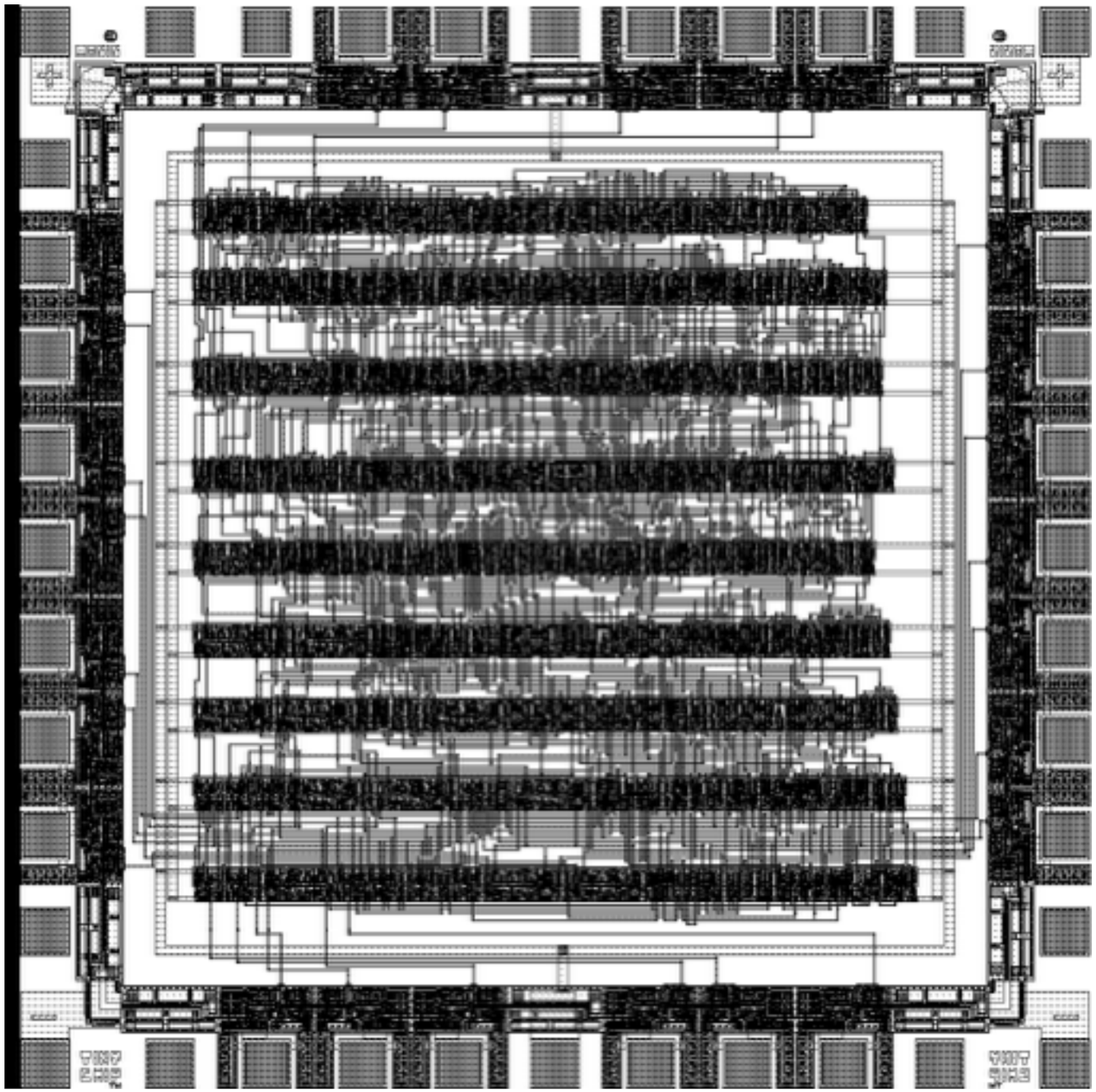
3-input NAND cell (ST Microelectronics):
C = Local Capacitance
T = input rise/fall time

Cell-based Design

- Standard cells



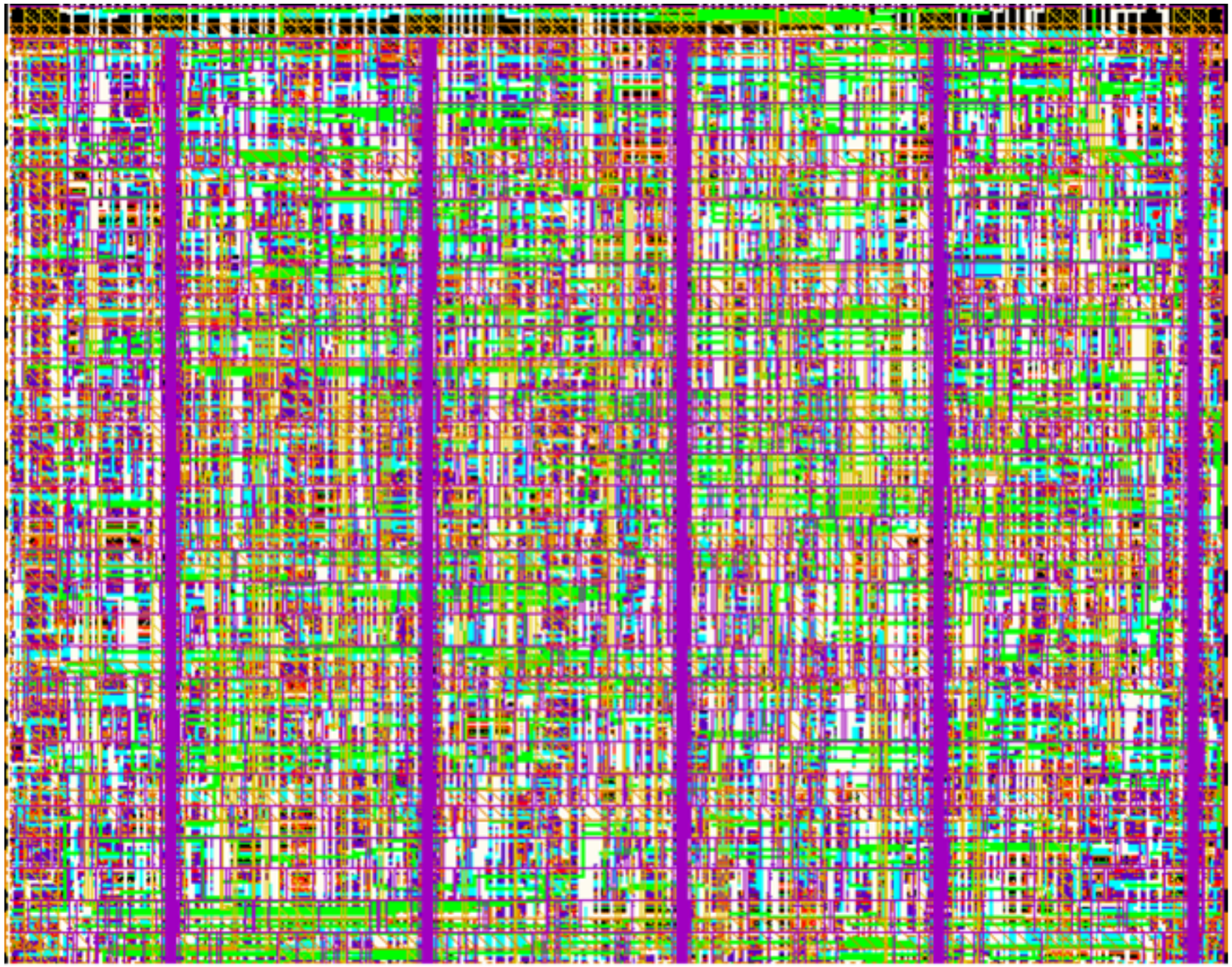
Cell-based Design — Example



Routing channel requirements are reduced by presence of more interconnect layers

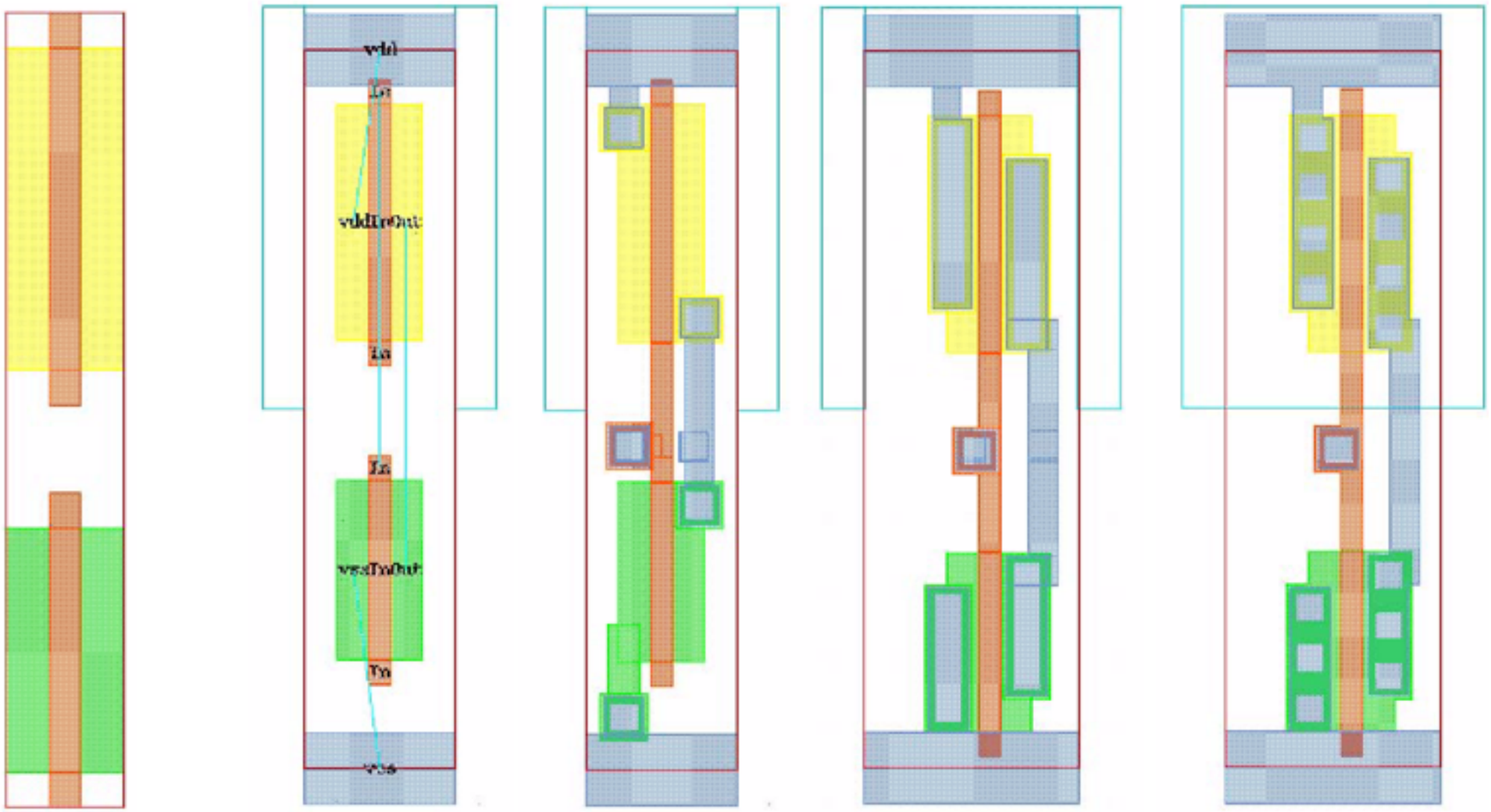
[Brodersen92]

Cell-based Design — The New Generation



Cell-structure
hidden under
interconnect layers

Automatic Cell Generation

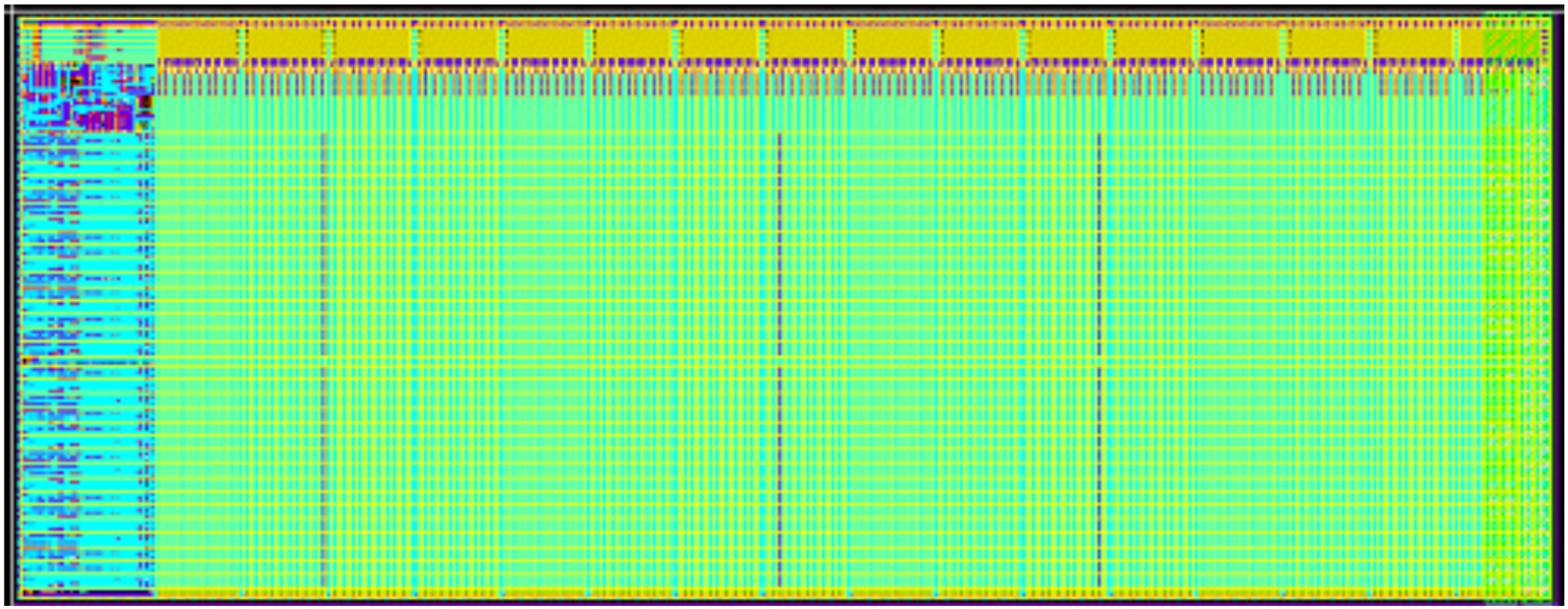


Initial transistor geometries | **Placed transistors** | **Routed cell** | **Compacted cell** | **Finished cell**

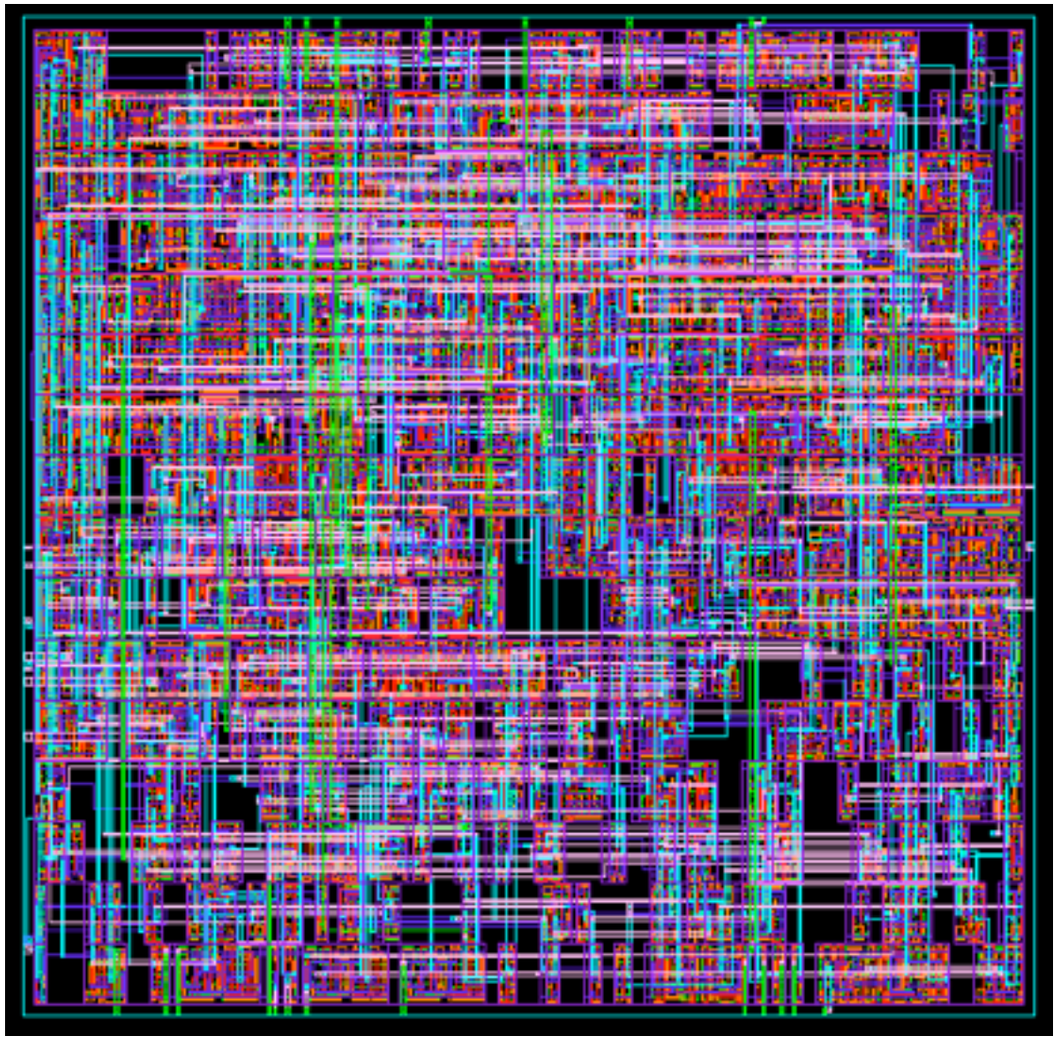
[Courtesy: Cadabra]

“Hard” Macro-Modules

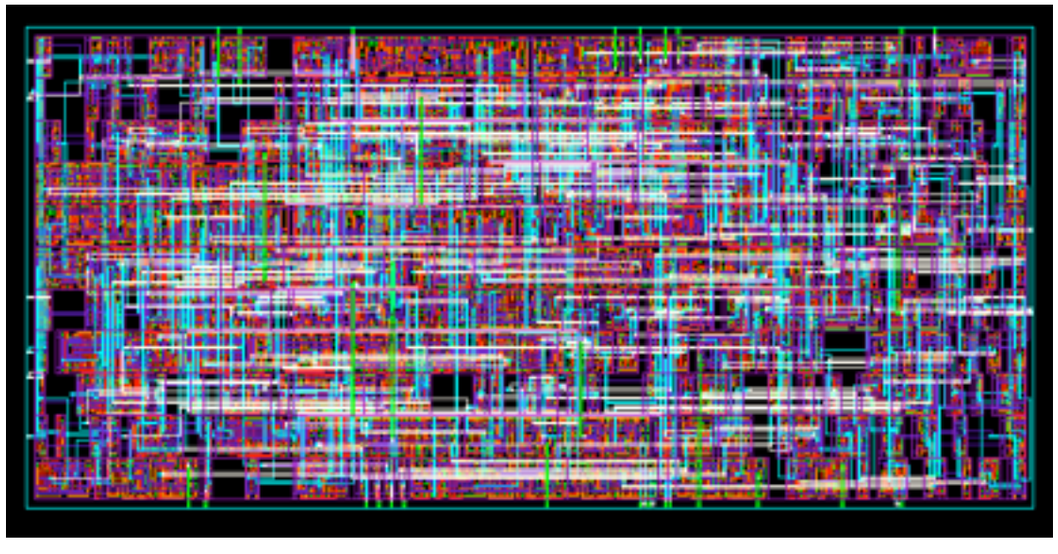
- 256×32 (or 8192 bit) SRAM
- Generated by hard-macro module generator



“Soft” Macro-Modules



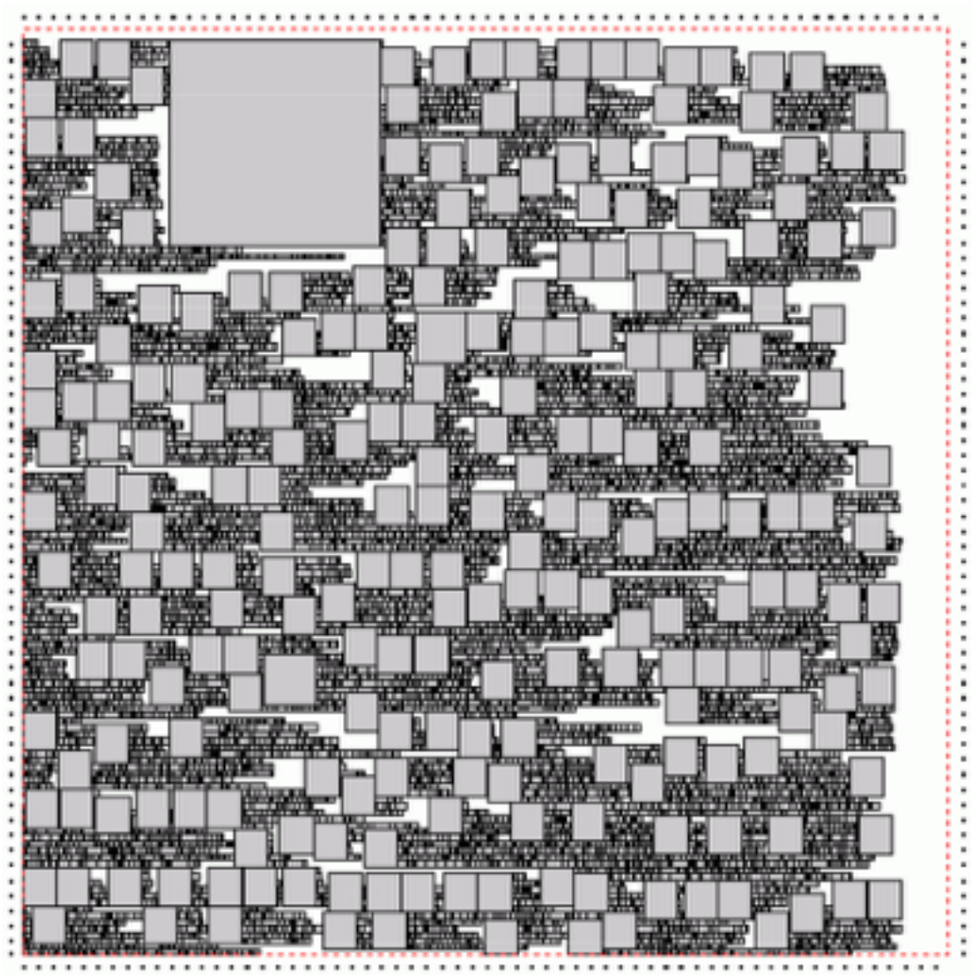
```
string mat = “booth”;
directive (multtype = mat);
output signed [16] Z = A * B;
```



Synopsys Design Compiler

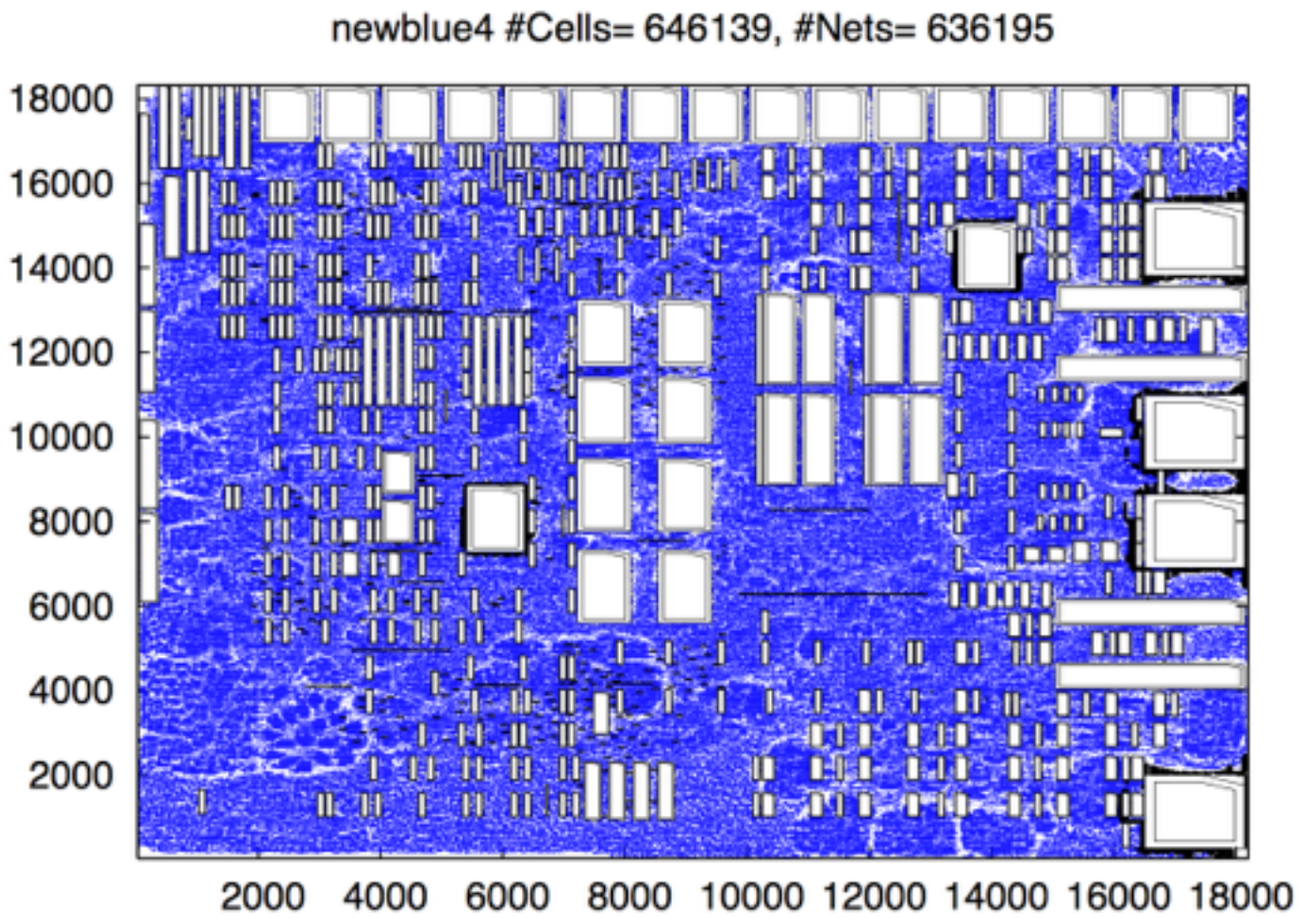
Mixed Macro & Standard Cells

ISPD98 ibm01



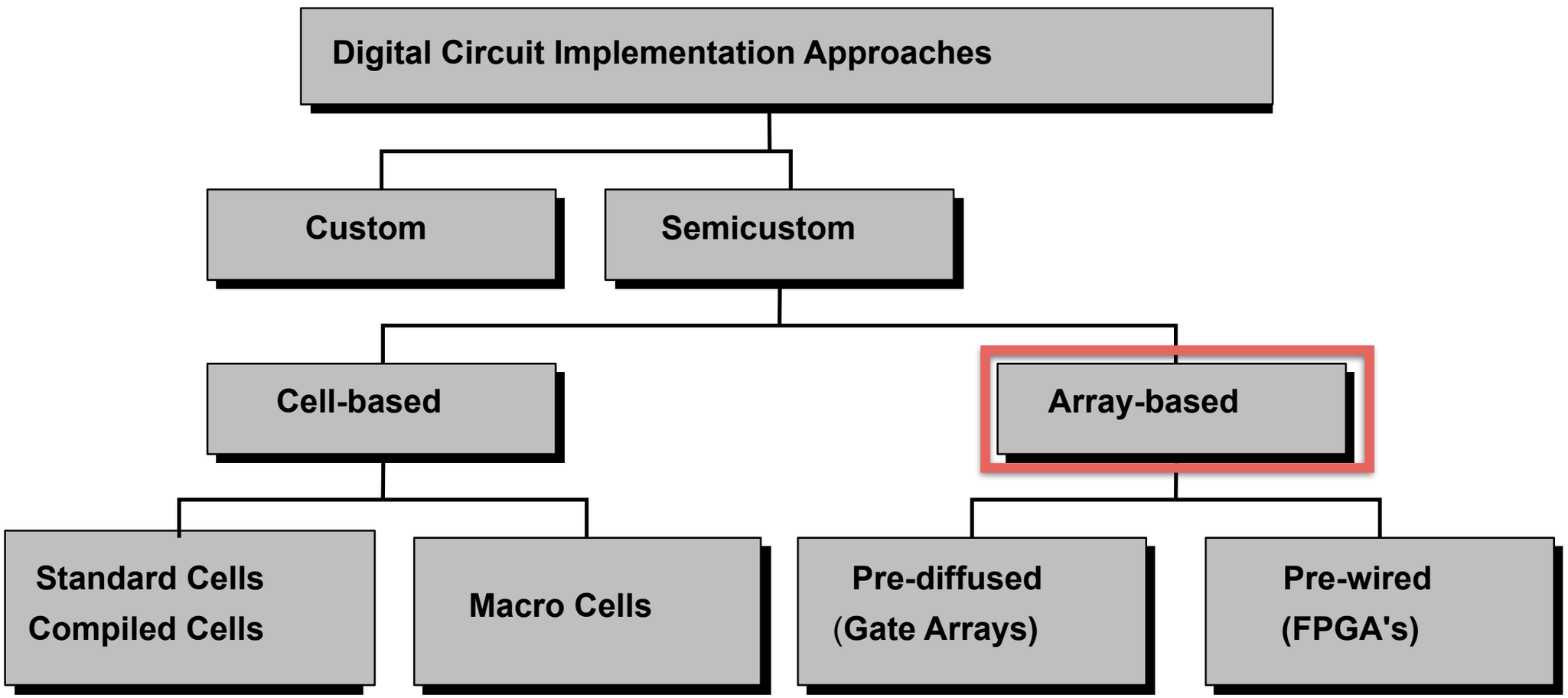
12752 cells, 247 macros

ISPD06 newblue4

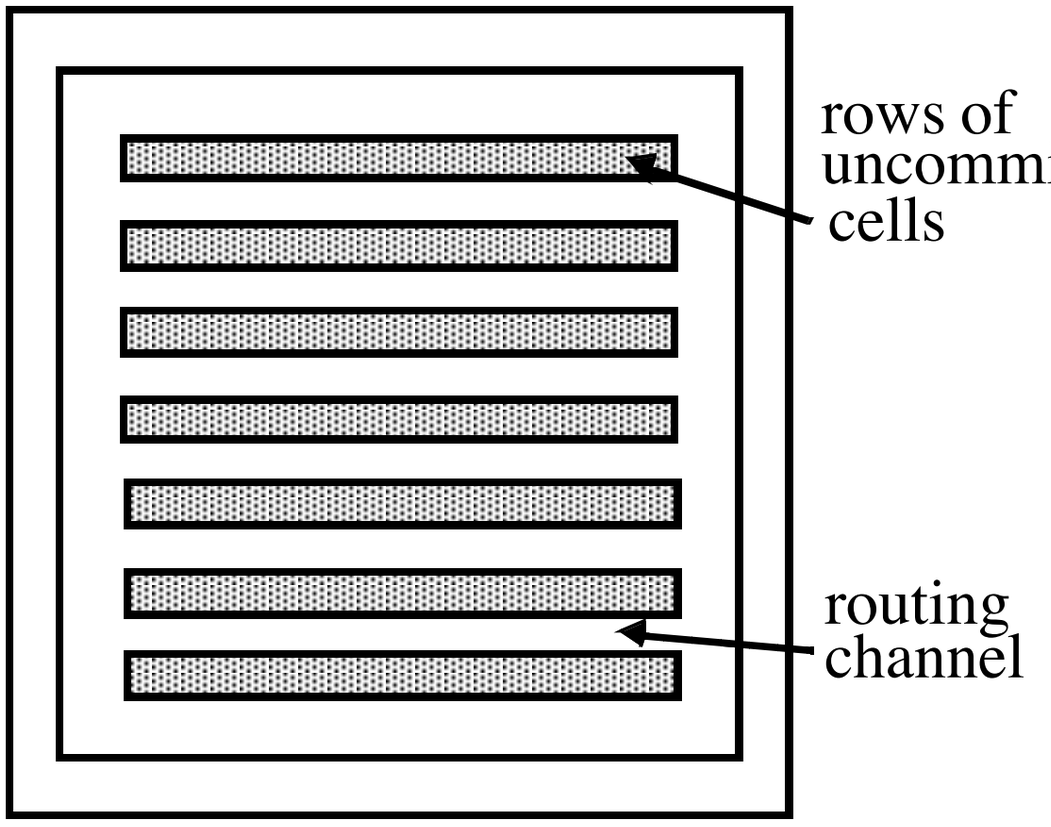


642717 cells, 3422 macros

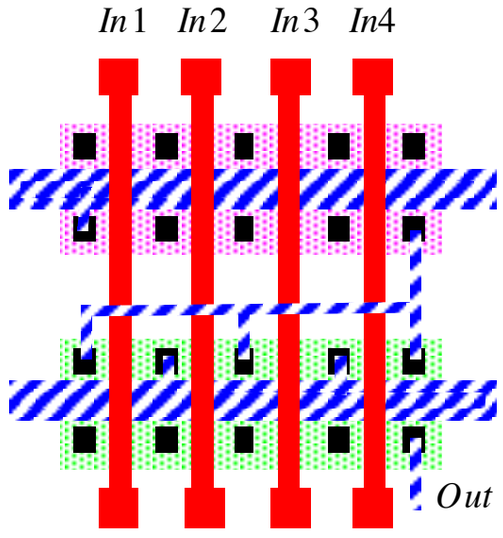
Array-based Design



Gate Array — Sea-of-gates



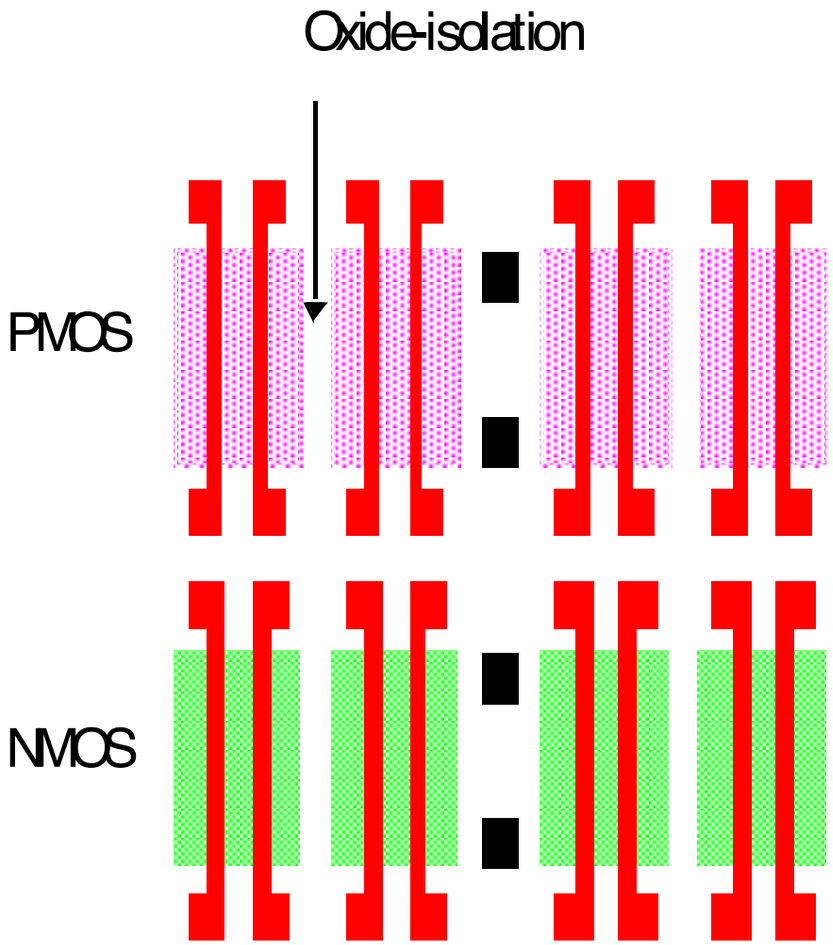
Uncommitted Cell



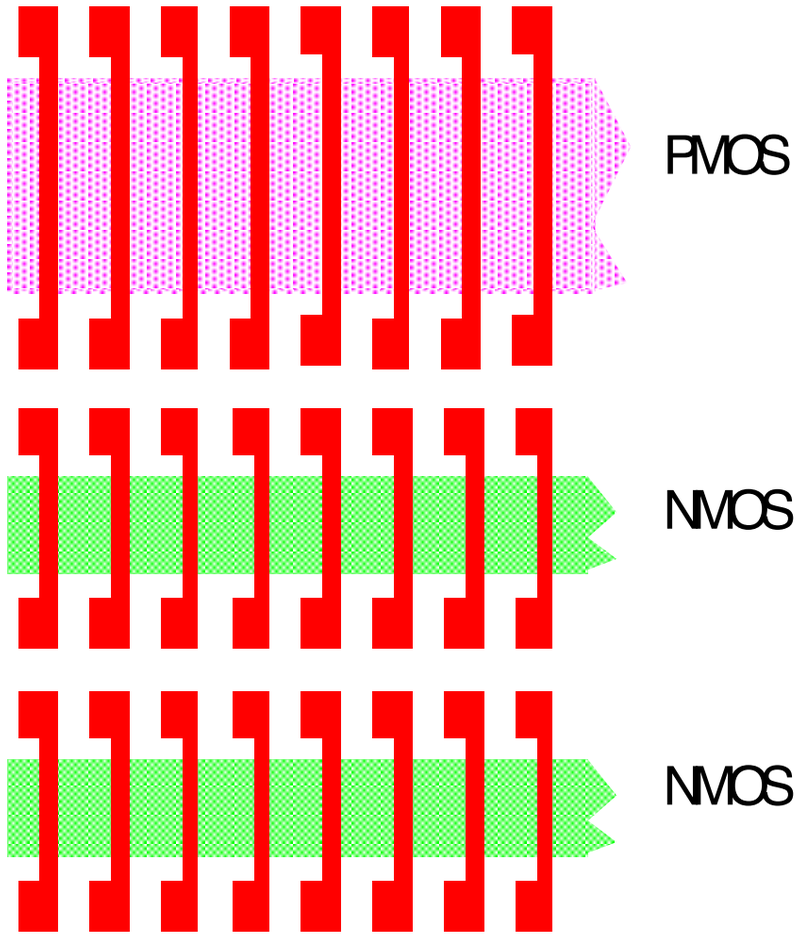
Committed Cell (4-input NOR)

- Wafers of pre-diffused transistors are pre-manufactured
- Desired interconnections added to determine the overall function of the chip

Sea-of-gate Primitive Cells

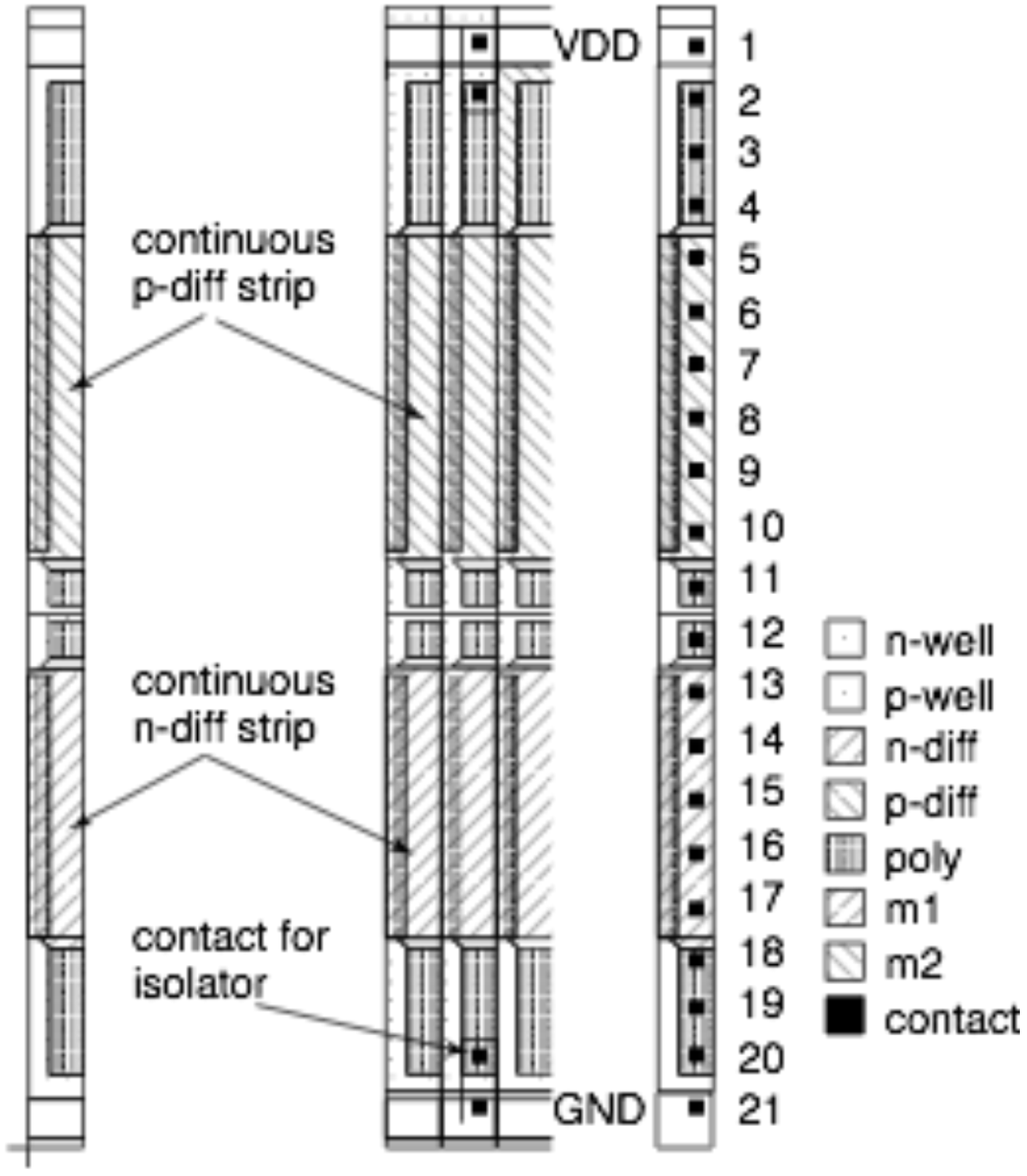


Using oxide-isolation



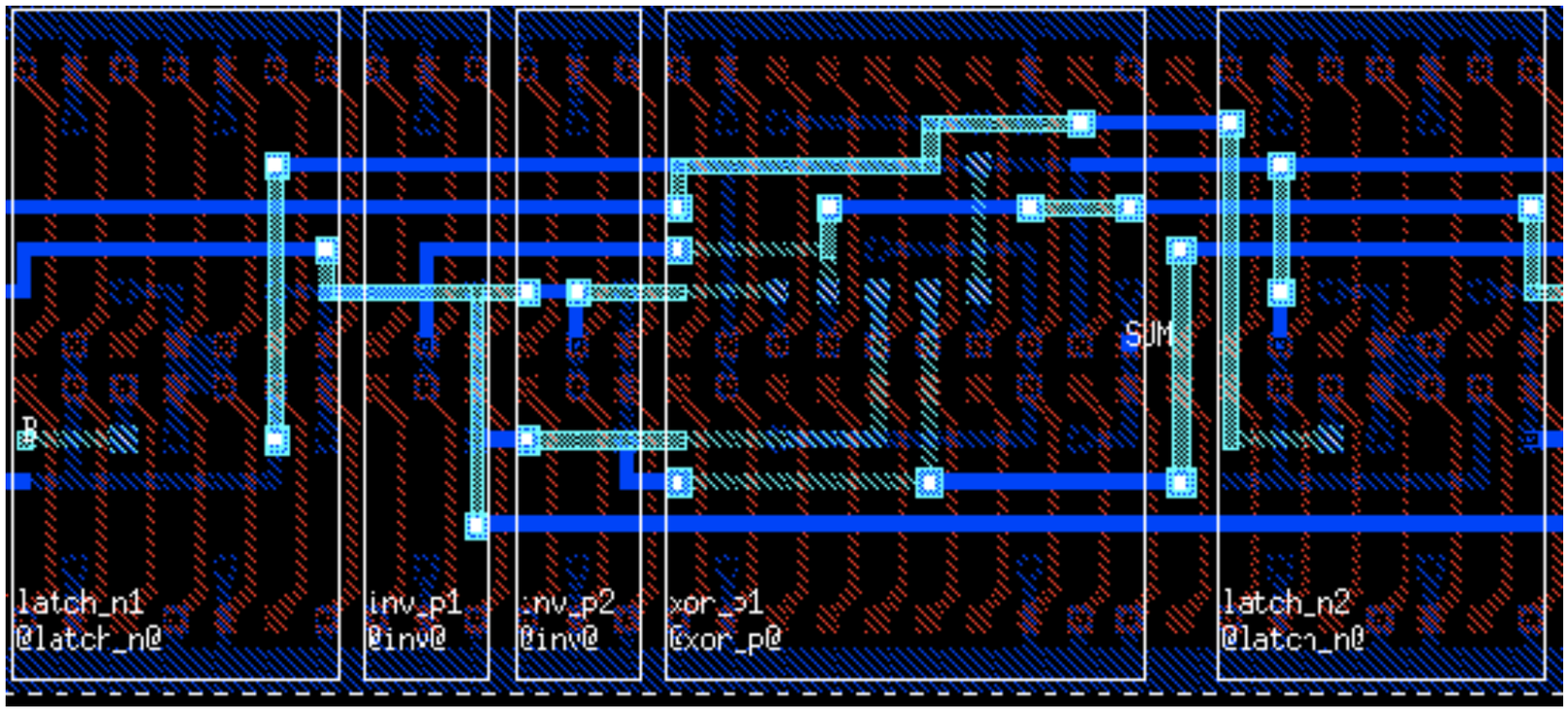
Using gate-isolation

Example: Base Cell of Gate-Isolated GA



From Smith97

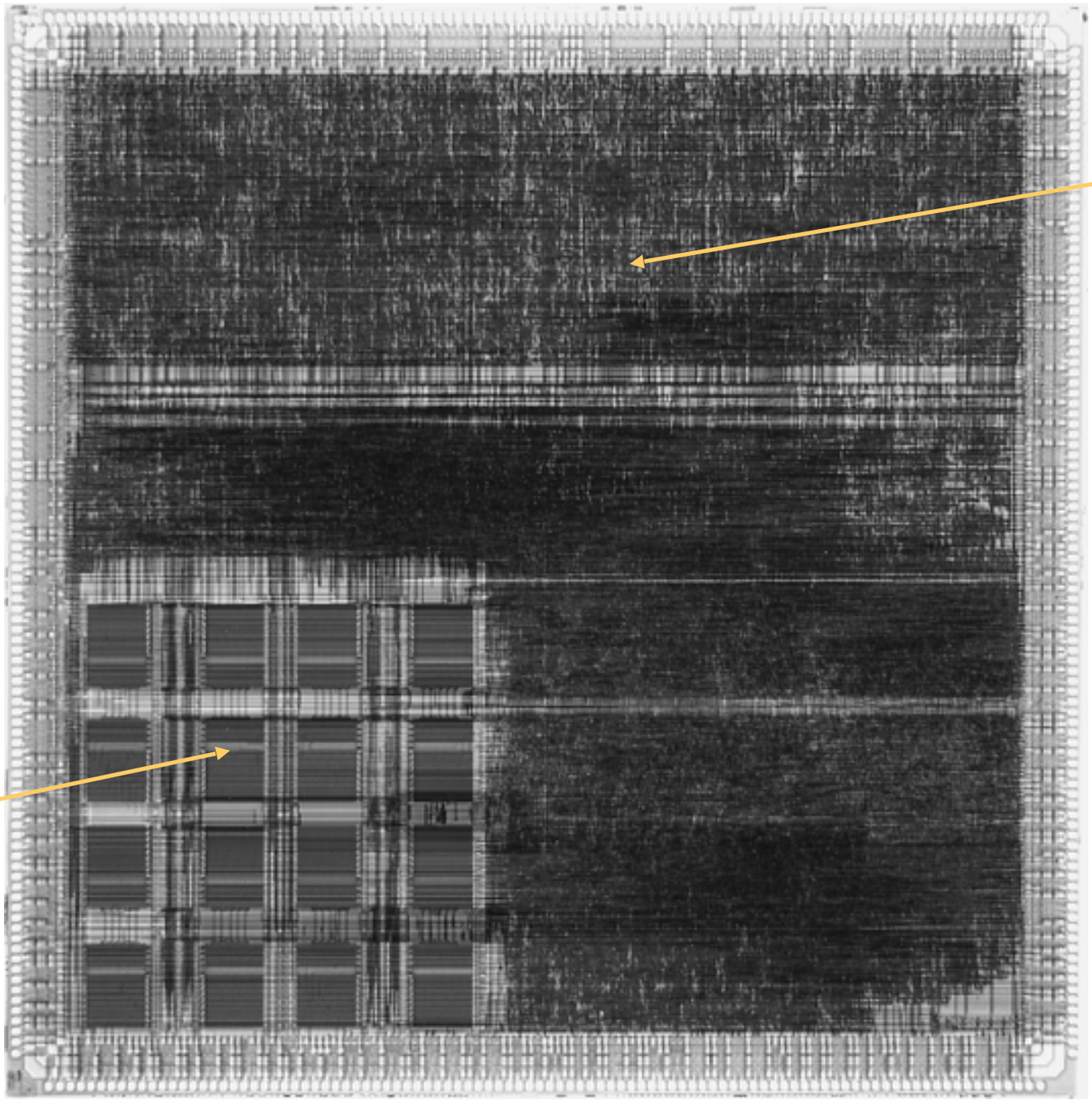
Example: Ocean System



[Courtesy: Ocean in DUT]

- Package link in DUT, the Netherlands.
- Tech report in 1993 by Patrick Groeneveld et al.

Sea-of-gates



LSI Logic LEA300K
(0.6 µm CMOS)

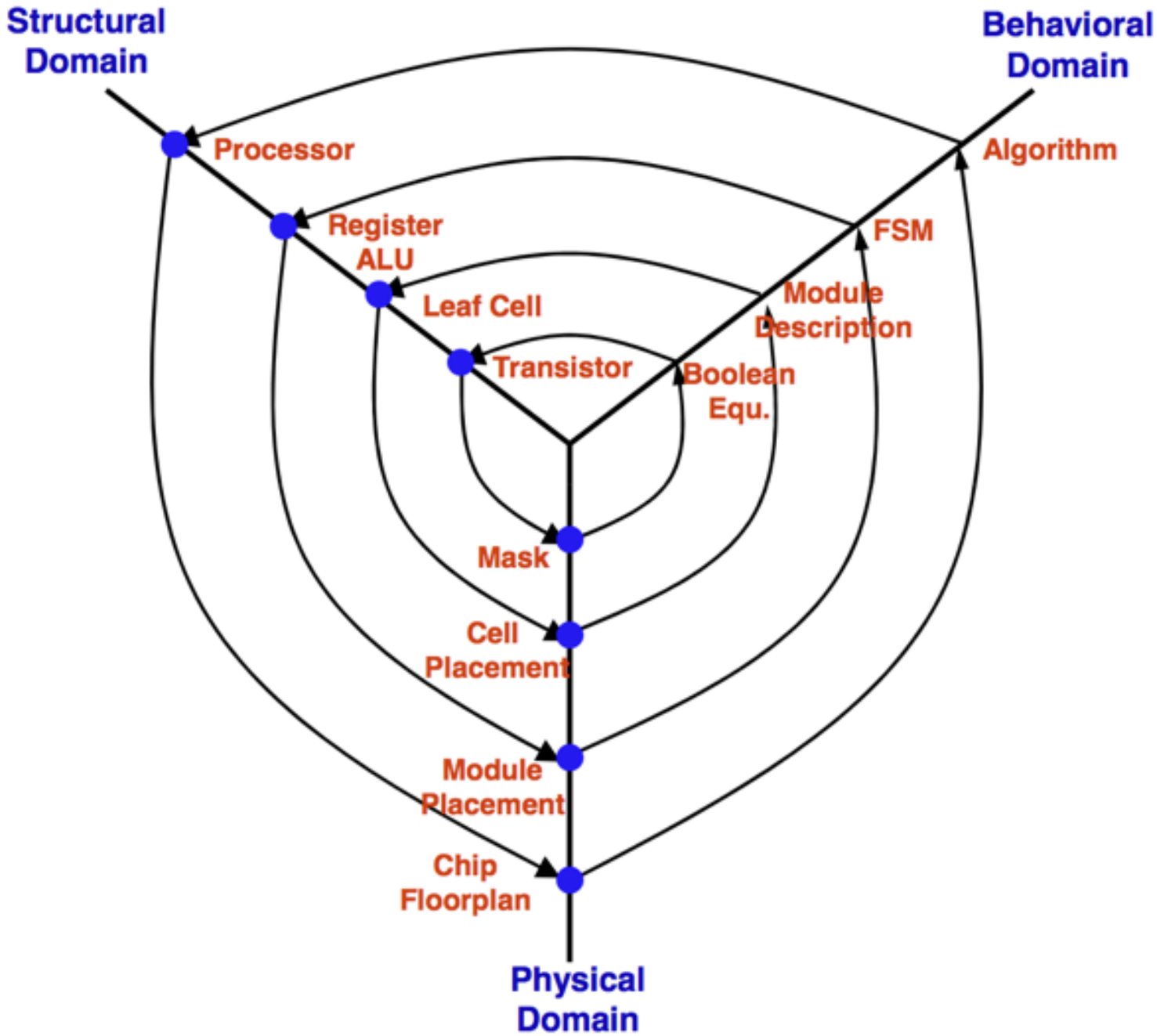
[Courtesy LSI Logic]

Pre-wired Arrays

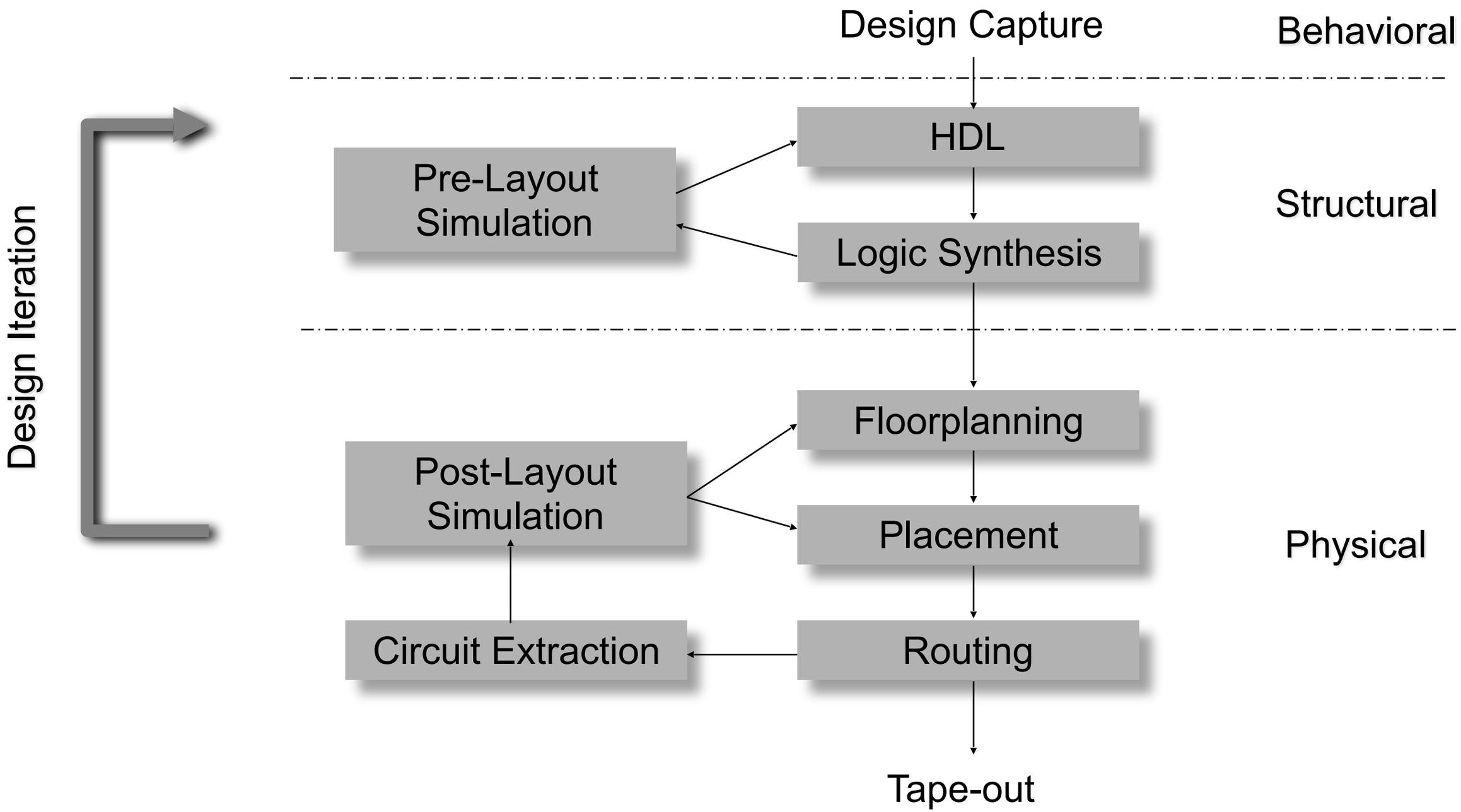
Classification of prewired arrays (or field-programmable devices):

- **Based on Programming Technique**
  - Fuse-based (program-once)
  - Non-volatile EPROM based
  - RAM based
- **Programmable Logic Style**
  - Array-Based
  - Look-up Table
- **Programmable Interconnect Style**
  - Channel-routing
  - Mesh networks

Design Methodology



“Design Closure” Problem

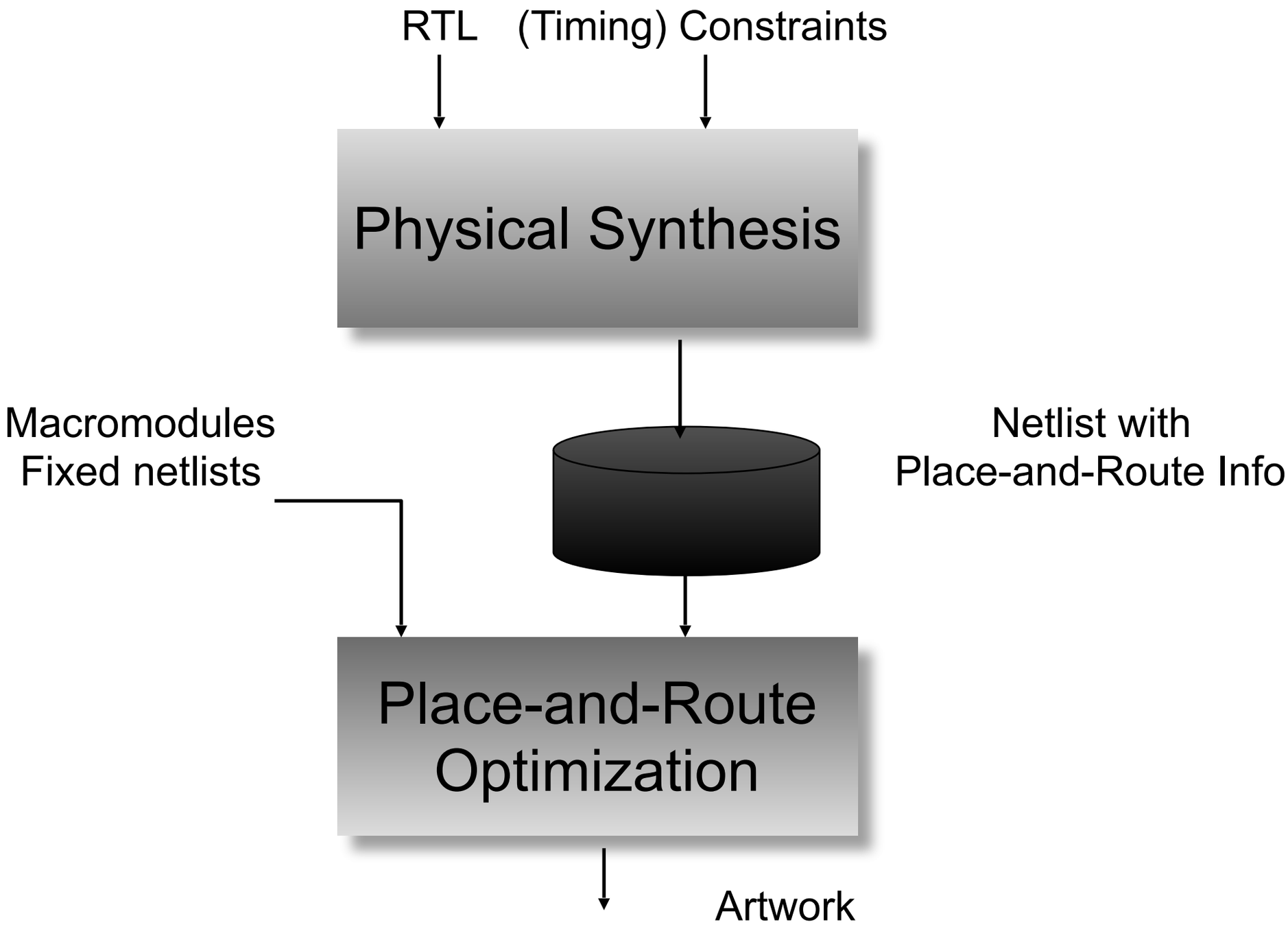


“Design Closure” Problem

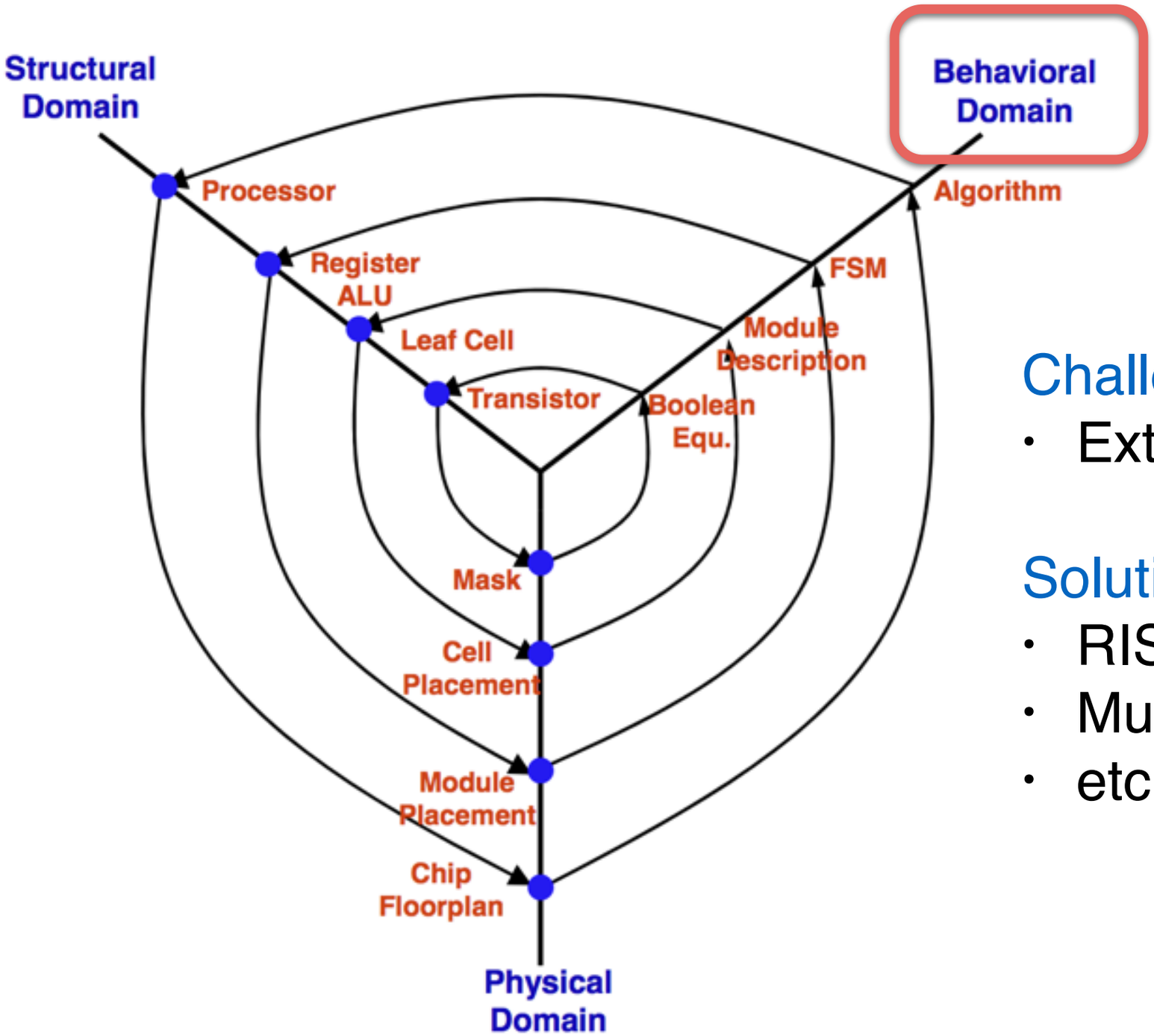
Iterative Removal of Timing Violations (white lines)

Courtesy Synopsys

Integrating Synthesis with Physical Design



Design Challenges — Behavioral Domain



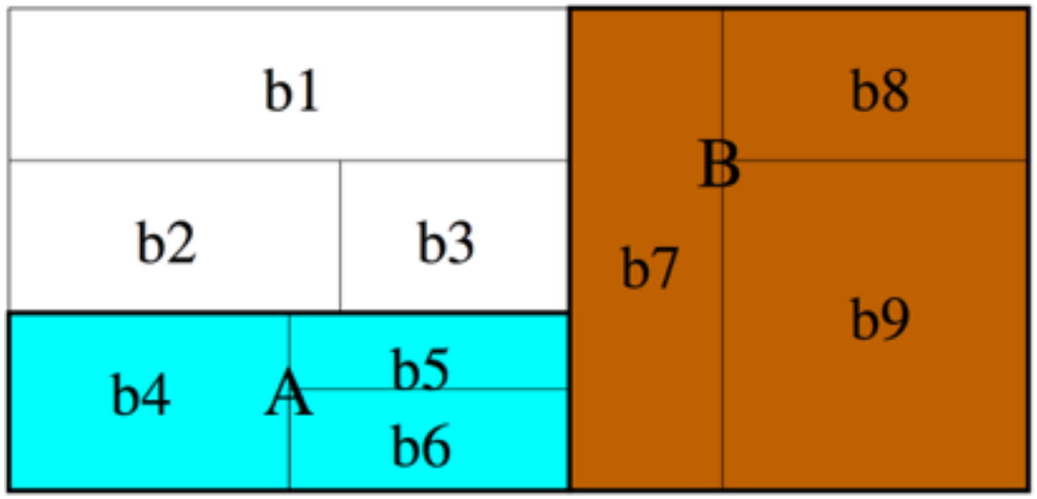
Challenge:

- Extreme Low Power Design

Solutions:

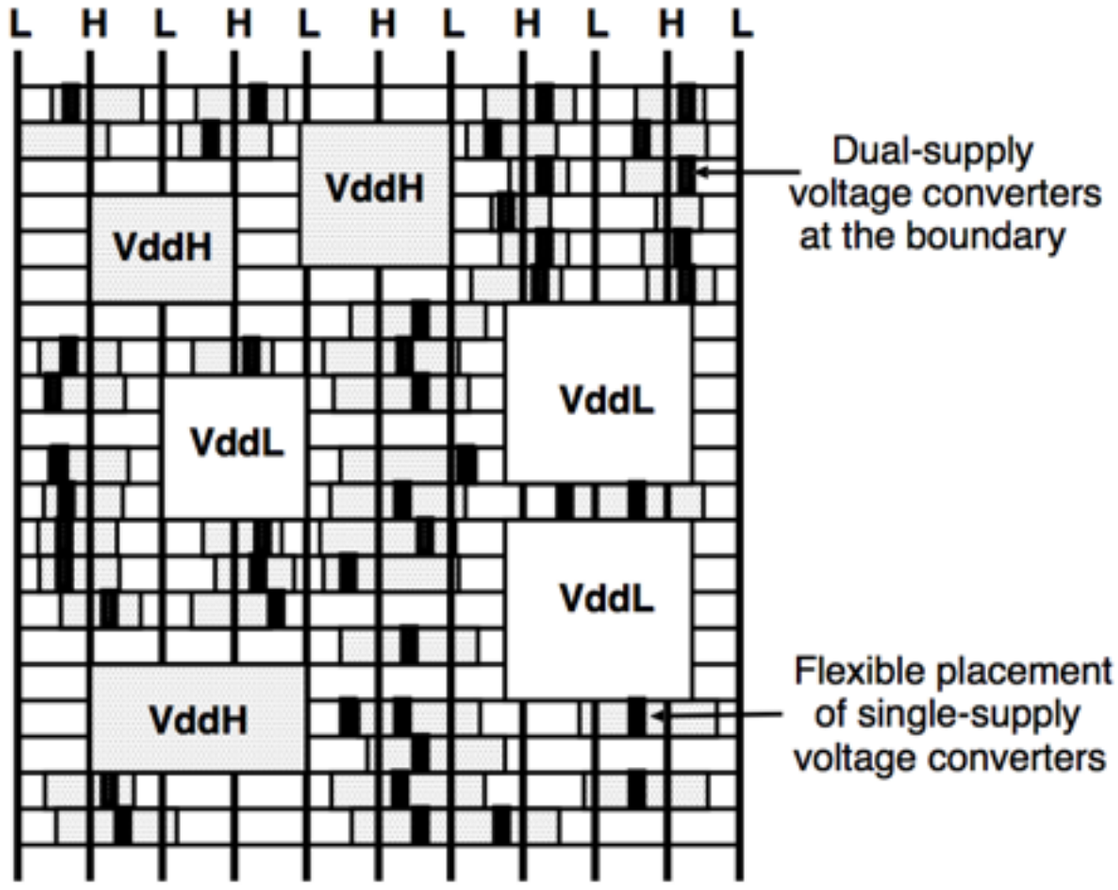
- RISC
- Multi-Supply Voltage
- etc

Multi-Supply Voltage toward Low Power



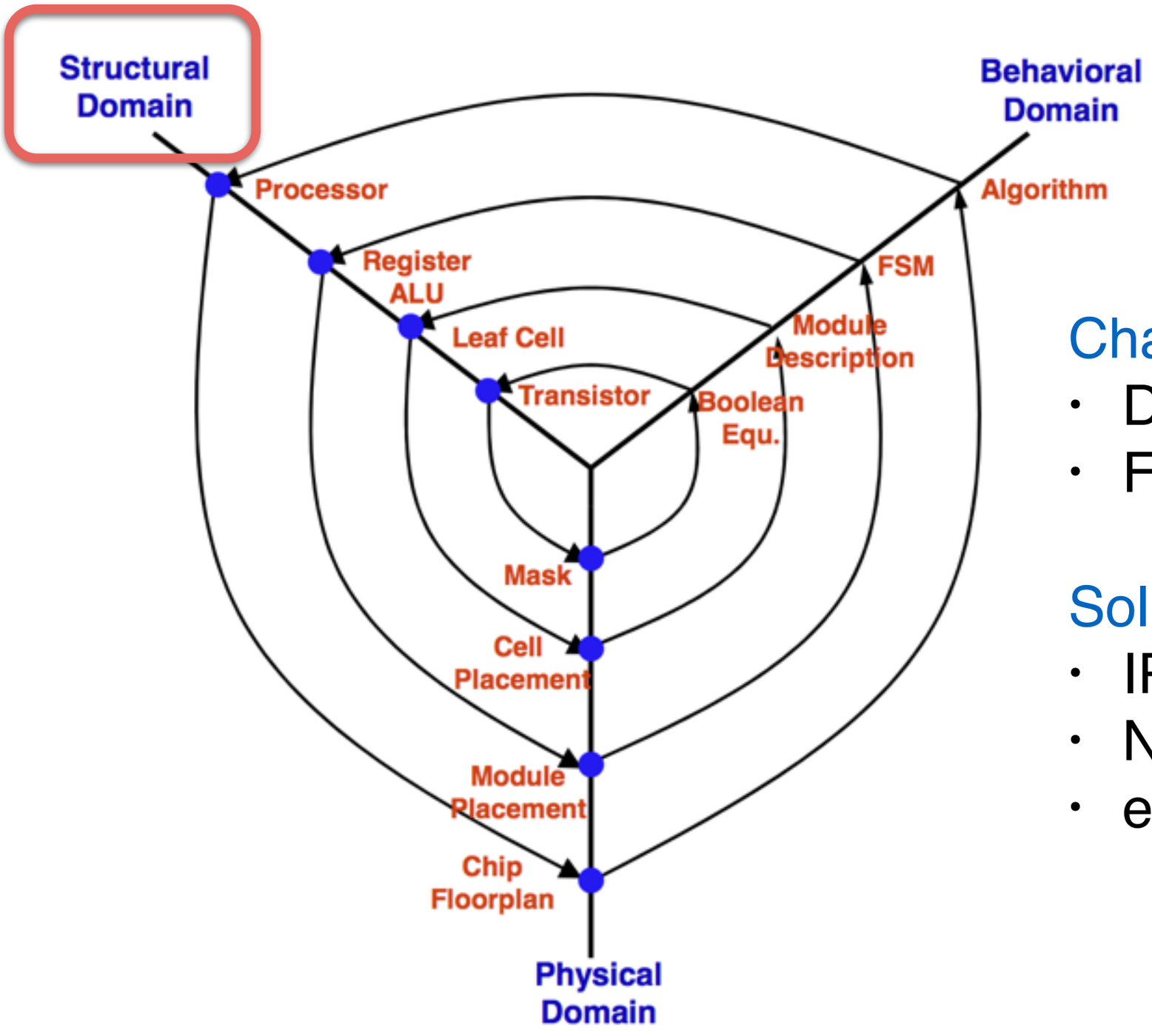
chip level 1.4 volt: b1,b2,b3
voltage island A (1.3 volt): b4,b5,b6
voltage island B (1.2 volt): b7,b8,b9

Higher level design
[Hung+,ICCD'05]



Lower level design
[Puri+,ICCAD'05]

Design Challenges — Structural Domain



Challenge:

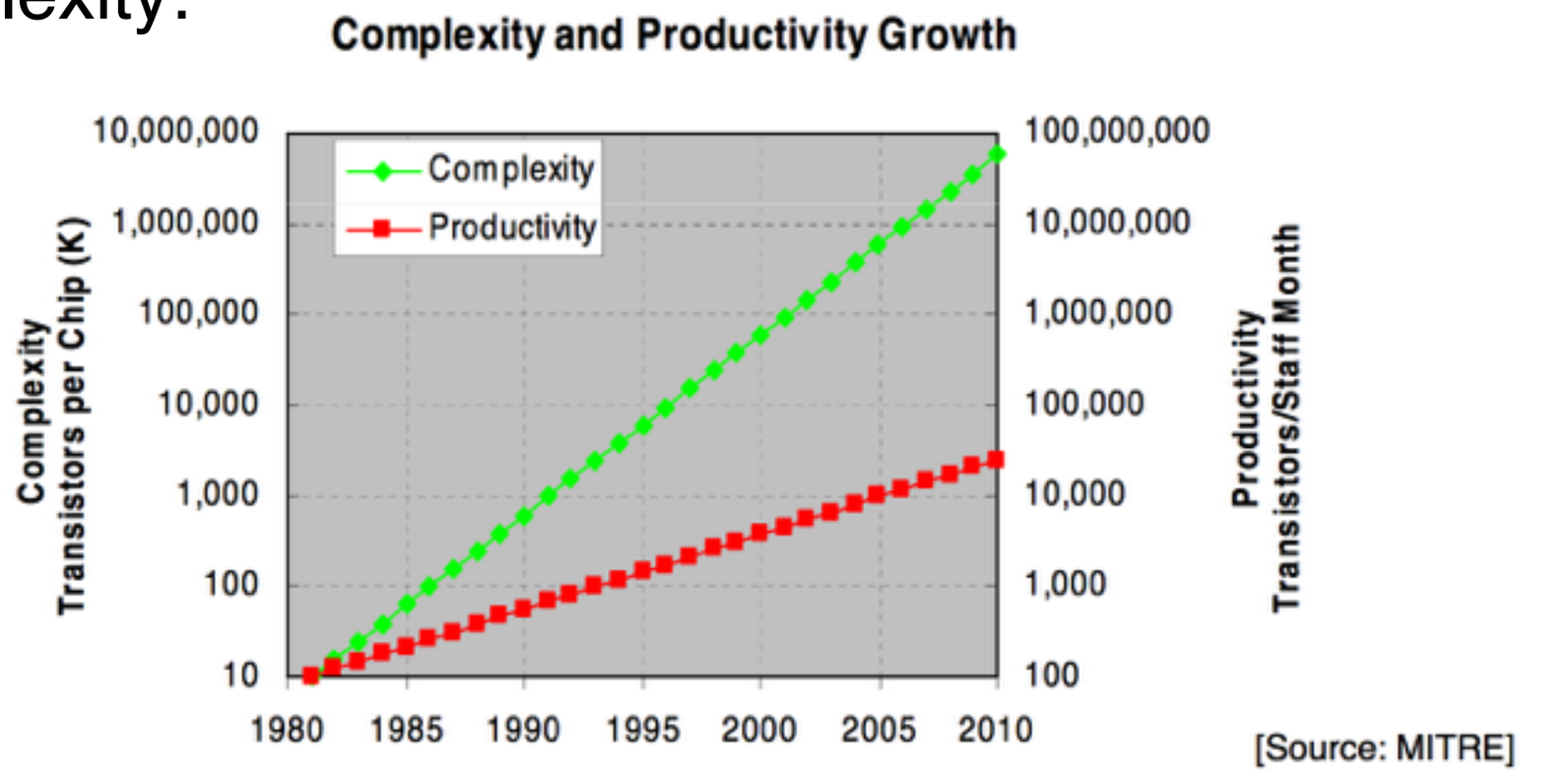
- Distributed design
- Faster design converge

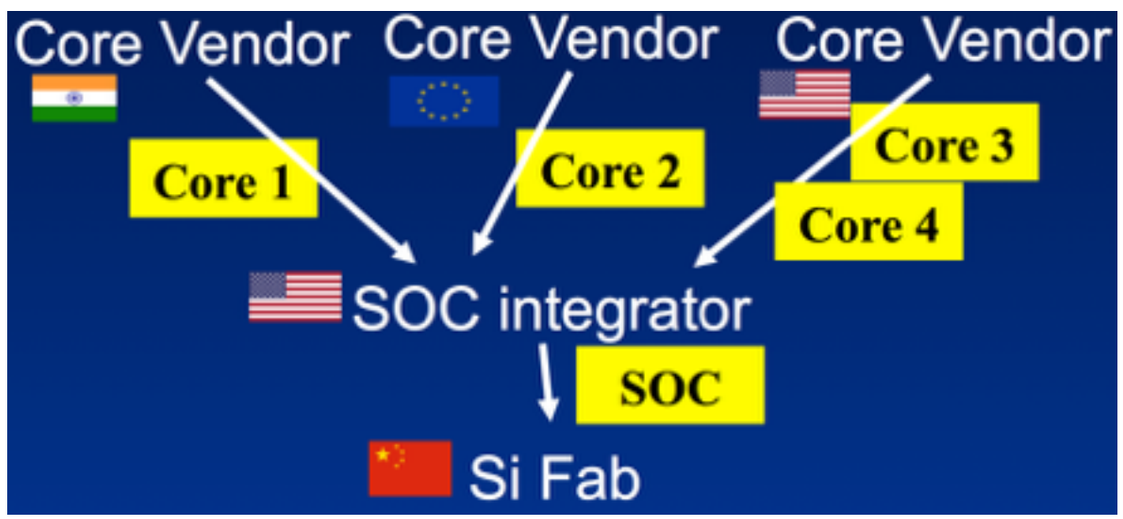
Solutions:

- IP re-use
- Network-on-Chips (NoCs)
- etc

Distributed SoC Design Flow

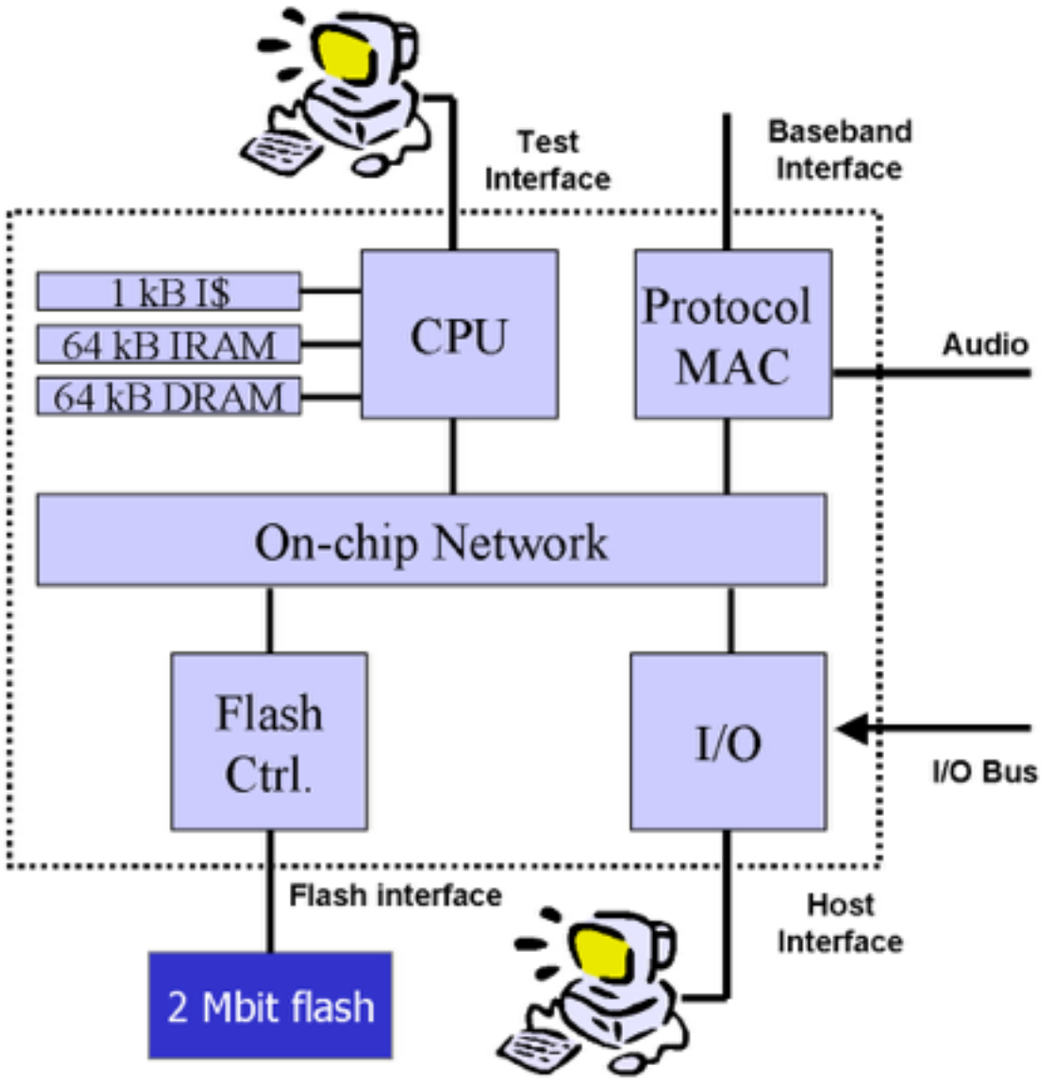
To overcome design complexity:



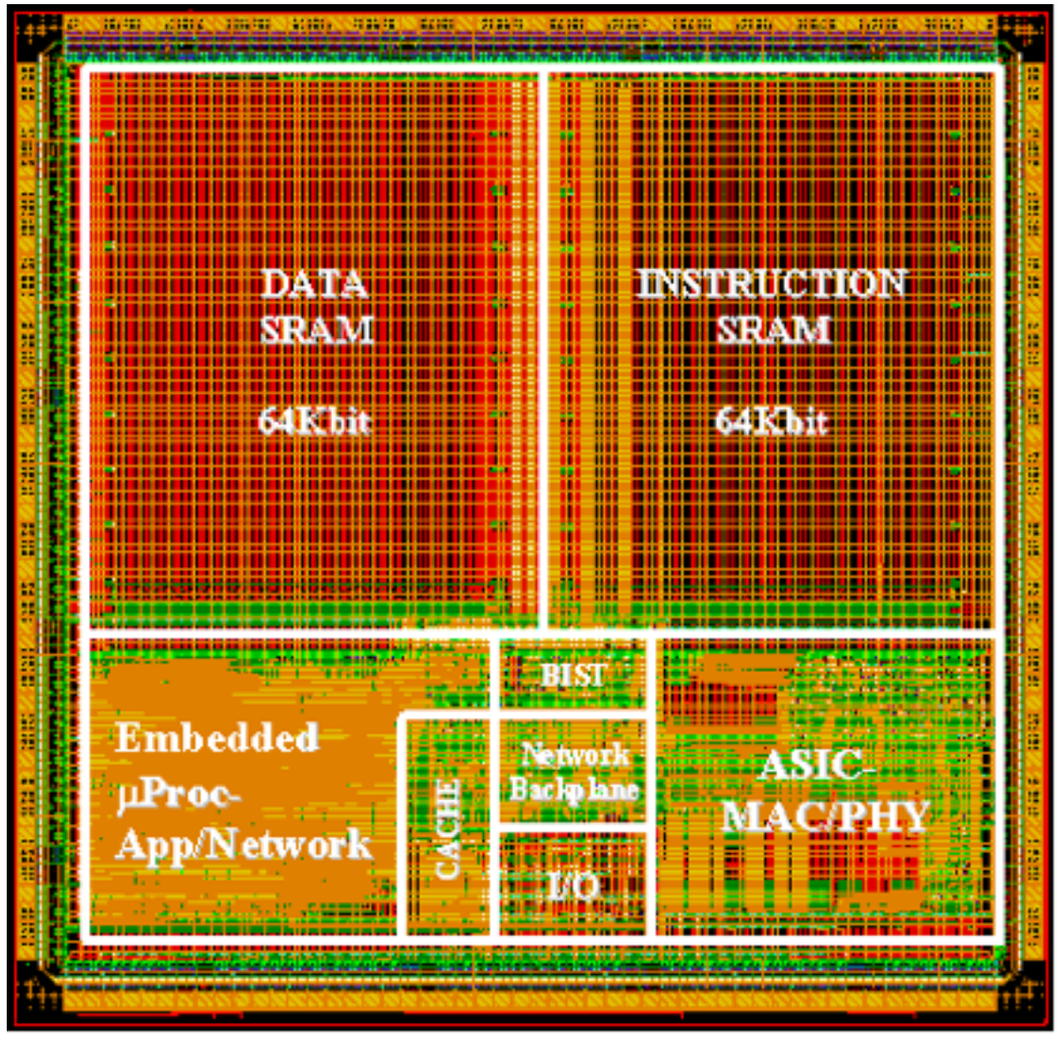


[Leef, ISPD'14]

“Intellectual Property” (IP) Cores

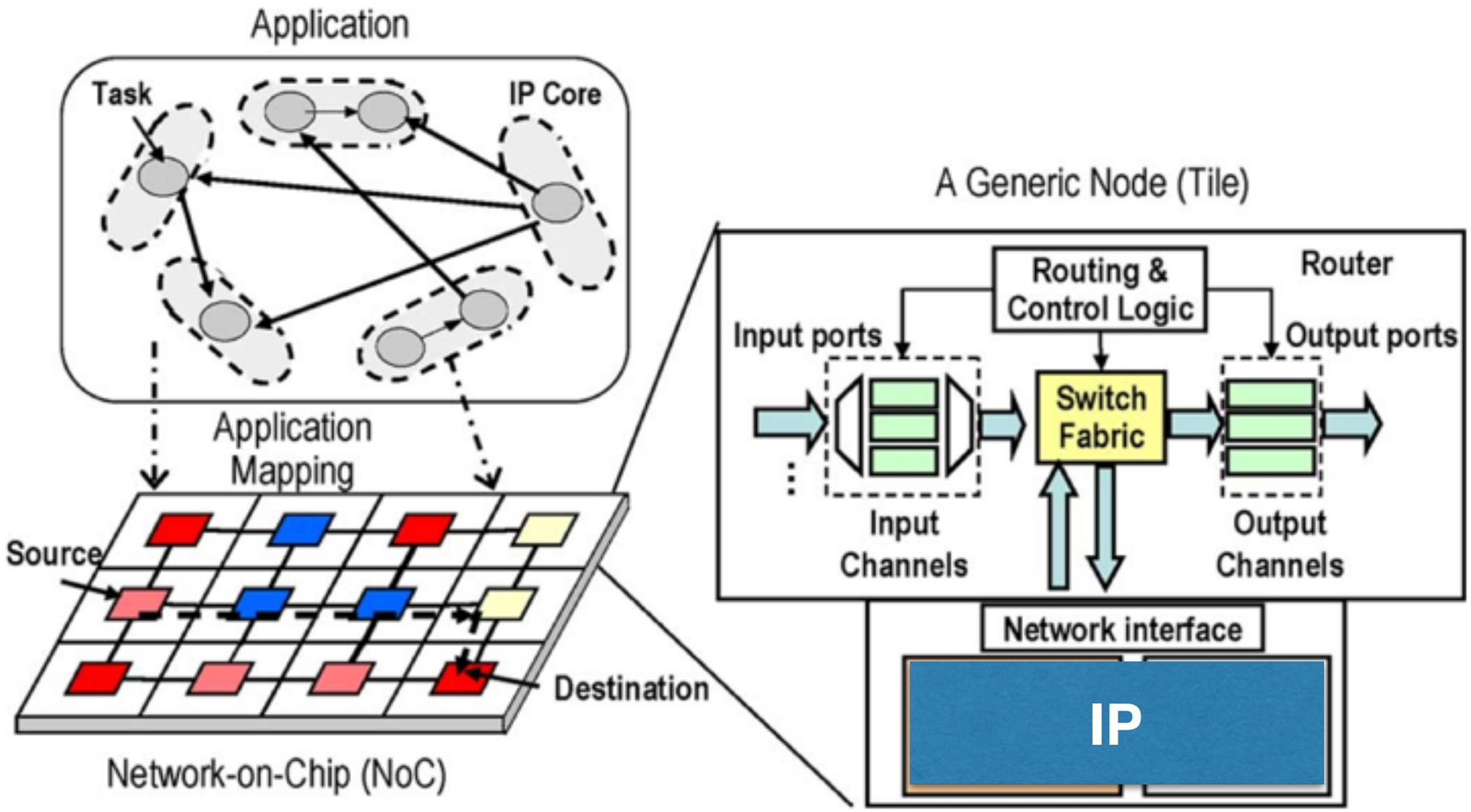


3422



A Protocol Processor for Wireless

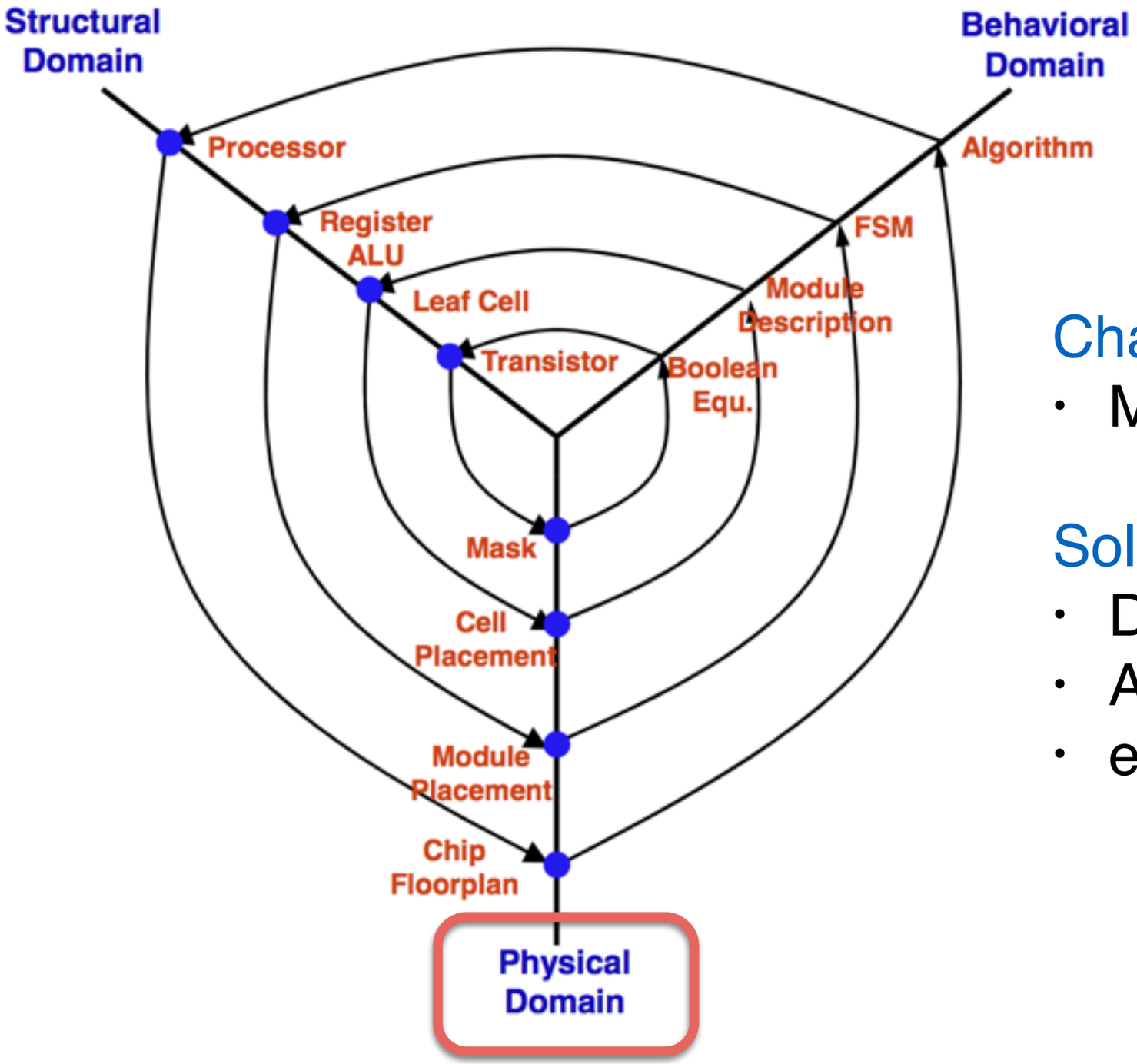
Network-on-Chips (NoCs)



[Marculescu+,TCAD'09]

- NoCs: heterogeneous IPs
- Communication through network interface (NI)

Design Challenges — Physical Domain



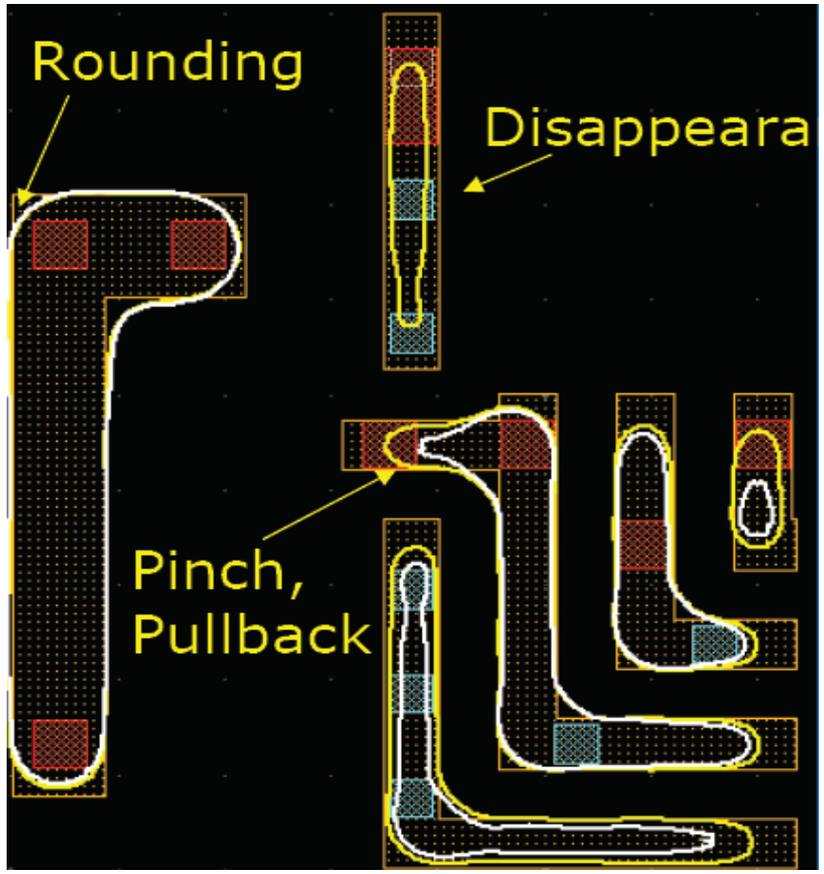
Challenge:

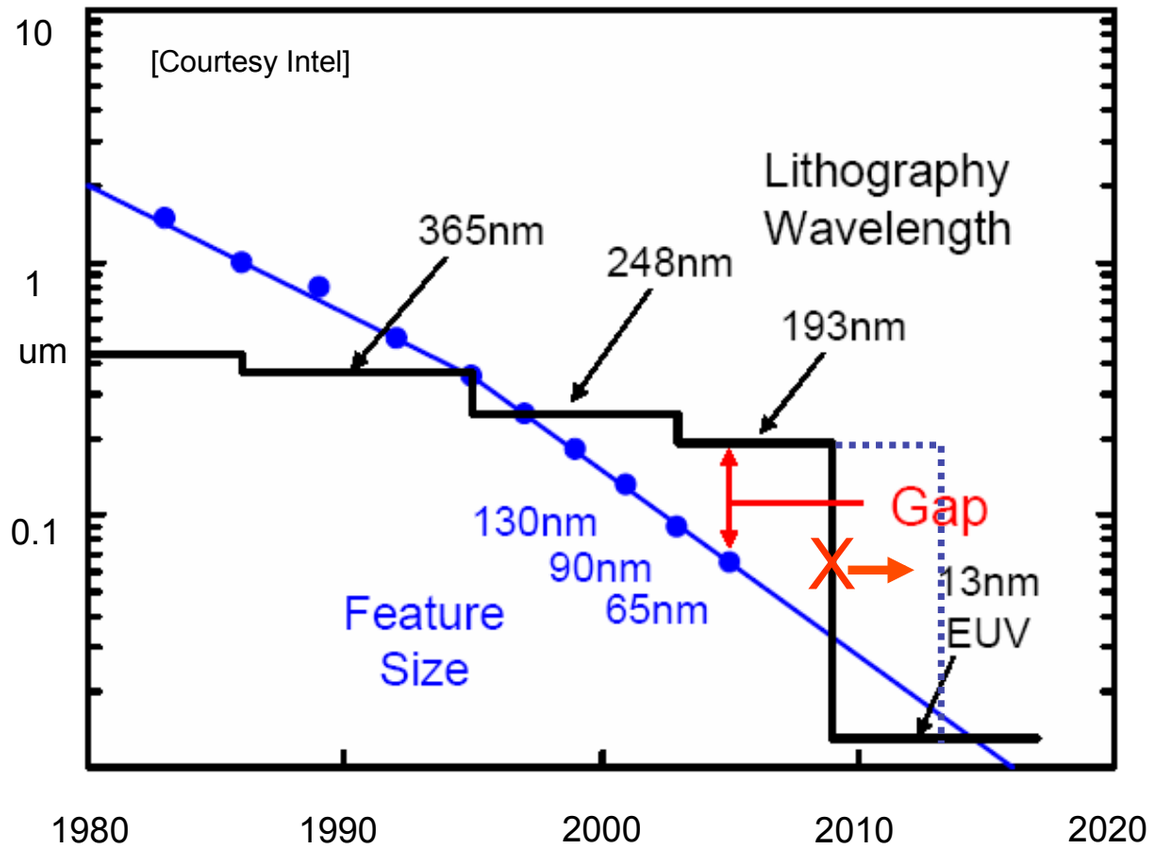
- Manufacturing

Solutions:

- Design for Manufacturing
- Advanced lithography
- etc

Manufacturing Challenges

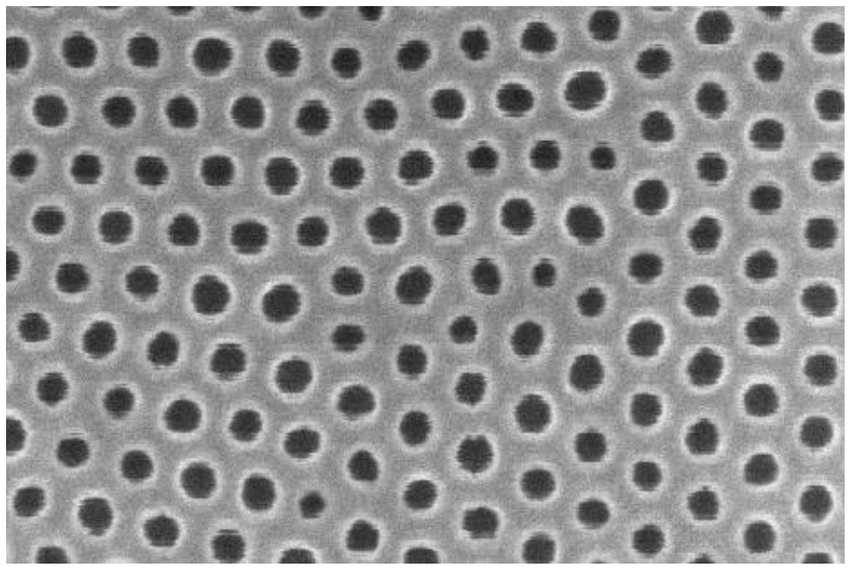




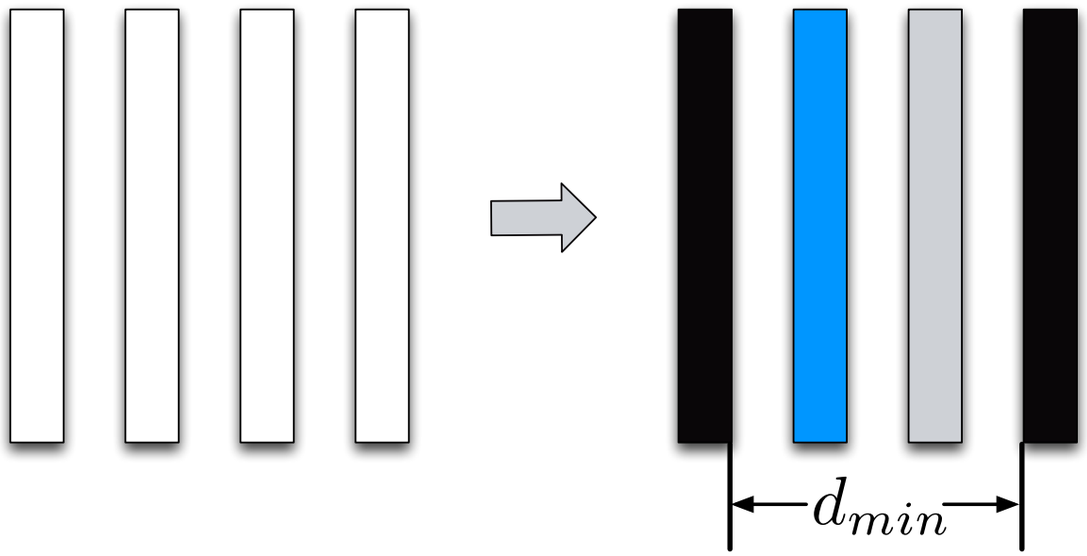
- Near future: multiple patterning lithography for 22nm/14nm ...
- Long term future: other advanced lithography

Courtesy ASML

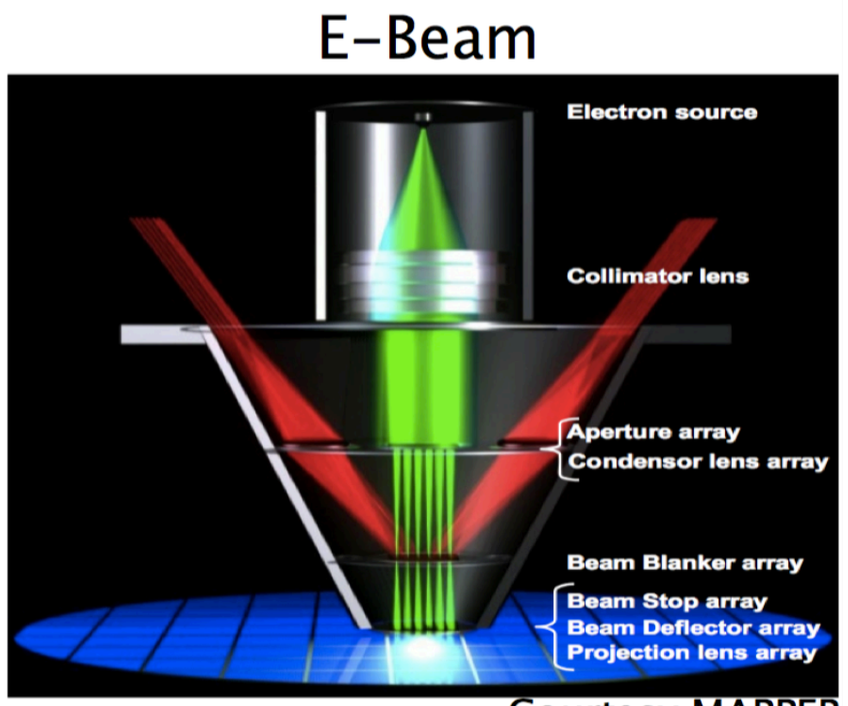
Extremely Ultra-Violet (EUV)



Directly Self-Assembly (DSA)



Triple Patterning Lithography (TPL)



Courtesy MAPPER

Electron Beam Lithography (EBL)