B3. Memory—1 Summary

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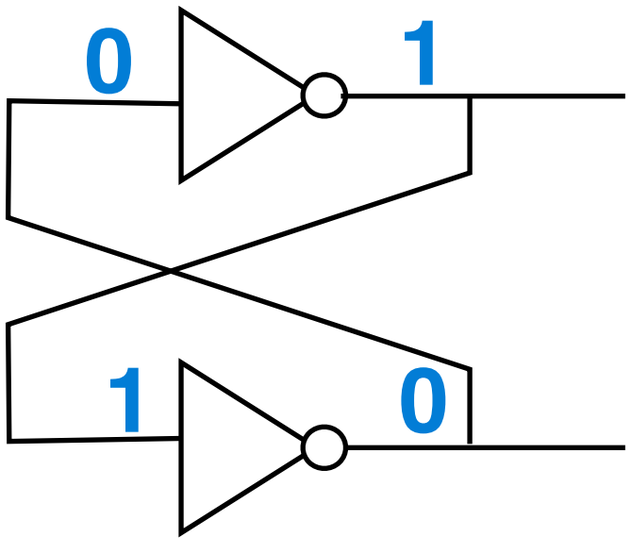
Reference:

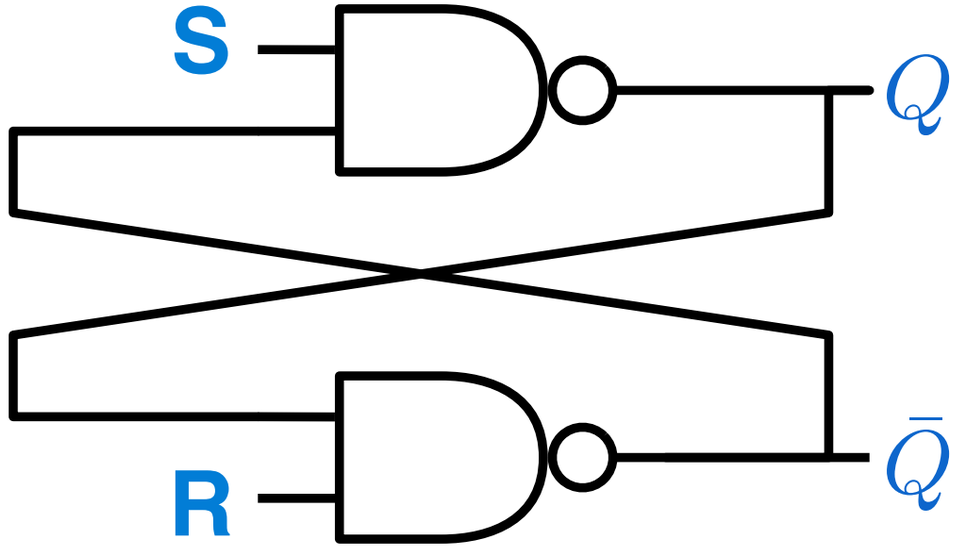
- Chapter 11 Memories
- **CMOS VLSI Design—A Circuits and Systems Perspective**
- by H.E.Weste and D.M.Harris

How to change the value stored?

- Replace inverter with NAND gate
- RS Latch
- If S or R=1, NAND gate works as inverter

A	B	A nand B
0	0	1
0	1	1
1	0	1
1	1	0

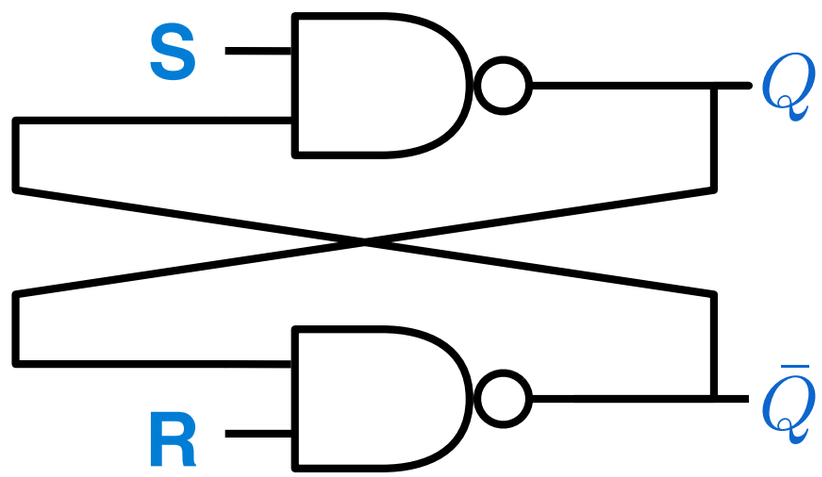




EX. RS Latch Summary

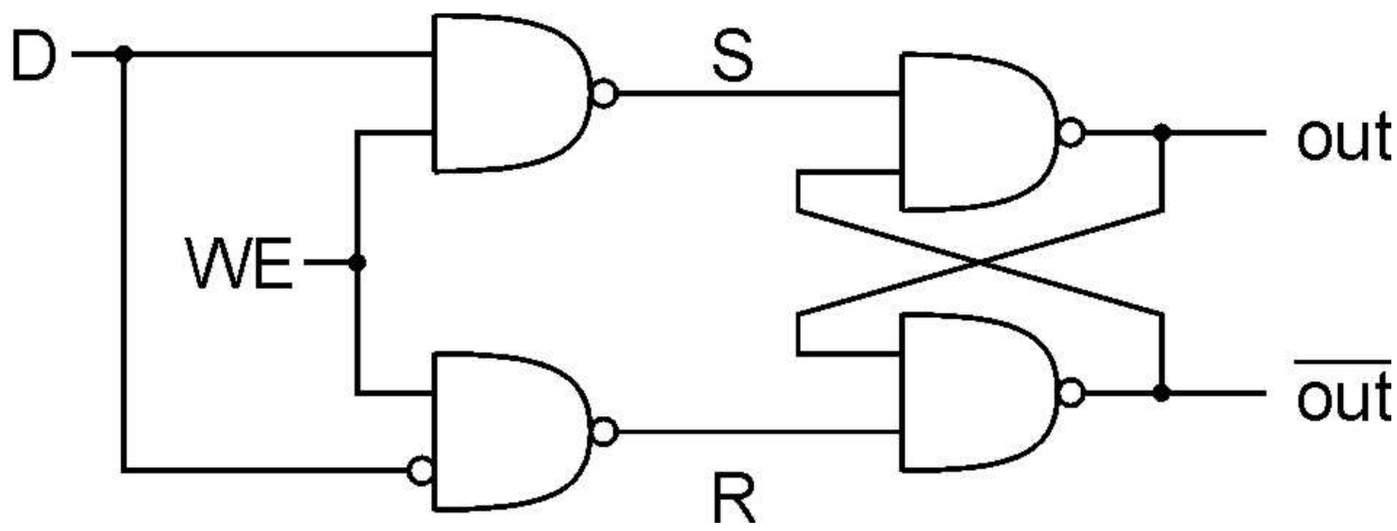
- **Question**: What's the Q value based on different R, S input.
  - R=S=1: latch holds current value
  - S=0, R=1: set value to 1
  - S=1, R=0: set value to 0
  - R=S=0: not determined, not allowed

A	B	A nand B
0	0	1
0	1	1
1	0	1
1	1	0

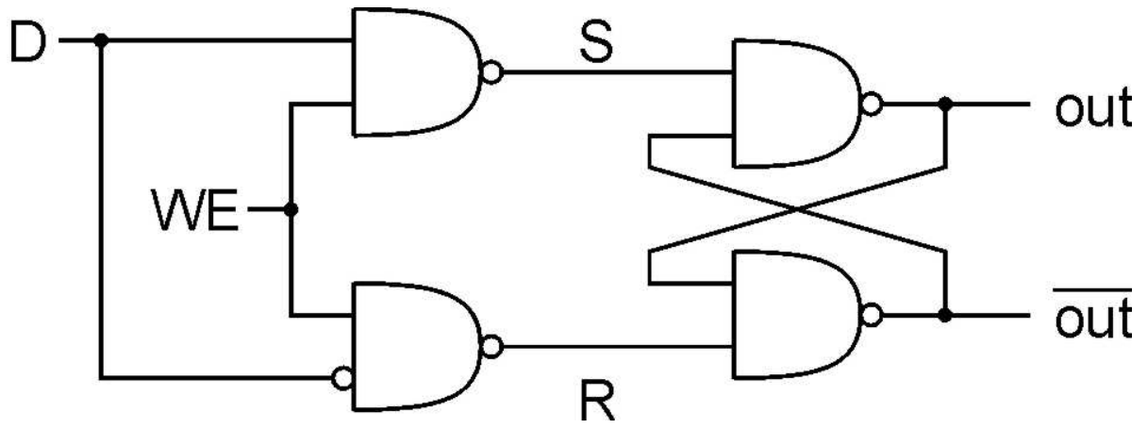


Gated D-Latch

- Two inputs: **D** (data) & **WE** (write enable)
- When WE=1, S=NOT(D), R=D;
- When WE=0, S=R=1



EX. Gated D-Latch



- **Question 1**: will S & R be zero at the same time?

No. D and NOT(D) make sure S and R are never zero at the same time

- **Question 2**: out values when
  - WE=1: S=NOT(D), R=D. out=D
  - WE=0: S=R=1, out holds current value

EX: 6T SRAM Read

- **Question 1**: A = 0, A_b = 1, discuss the behavior:
  1. bit & bit_b are pre-charged to high, then float
  2. word is set to high

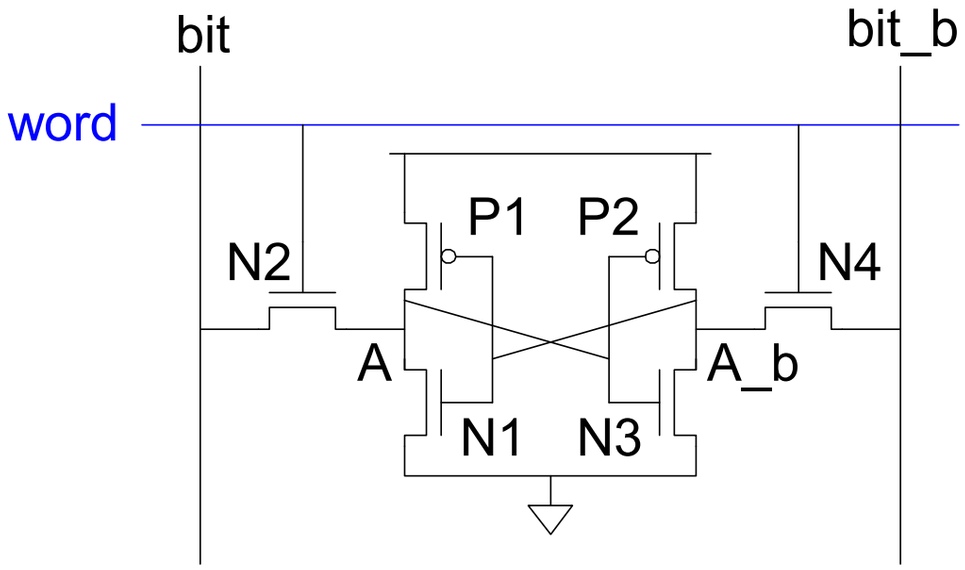
  3.1 bit_b=A_b=1, thus right side remains the same

  3.2 bit line is pulled down through N2 and N1

- **Question 2**: At least how many bit lines to finish read?

  One line.

  For example, only bit is enough for reading.



EX: 6T SRAM Write

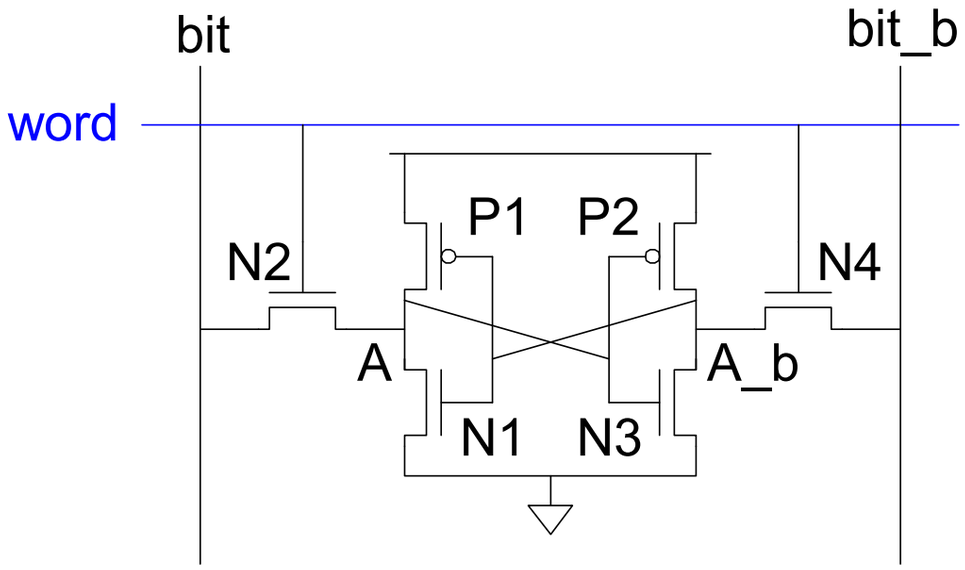
- **Question 1**: A = 0, A_b = 1, discuss the behavior:

  1. bit = 1 & bit_b= 0;
  2. word is set to high
  3 A=0 => P2 is open => P2<<N4

     => A_b would be pulled down by bit_b (0)

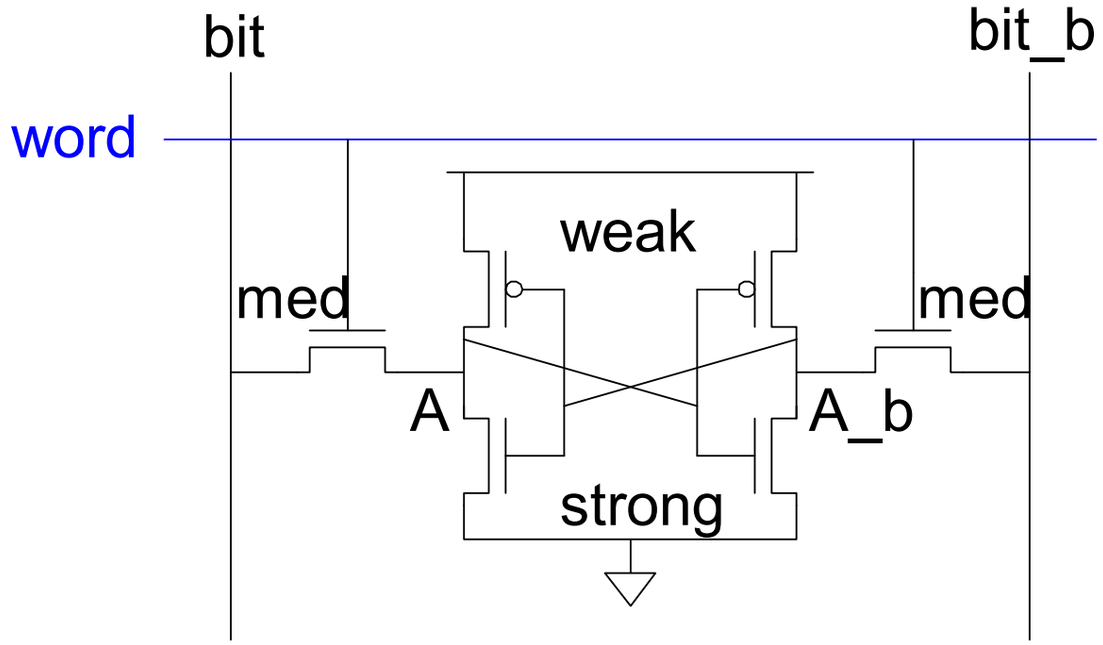
- **Question 2**: At least how many bit lines to finish write?

  We need two.

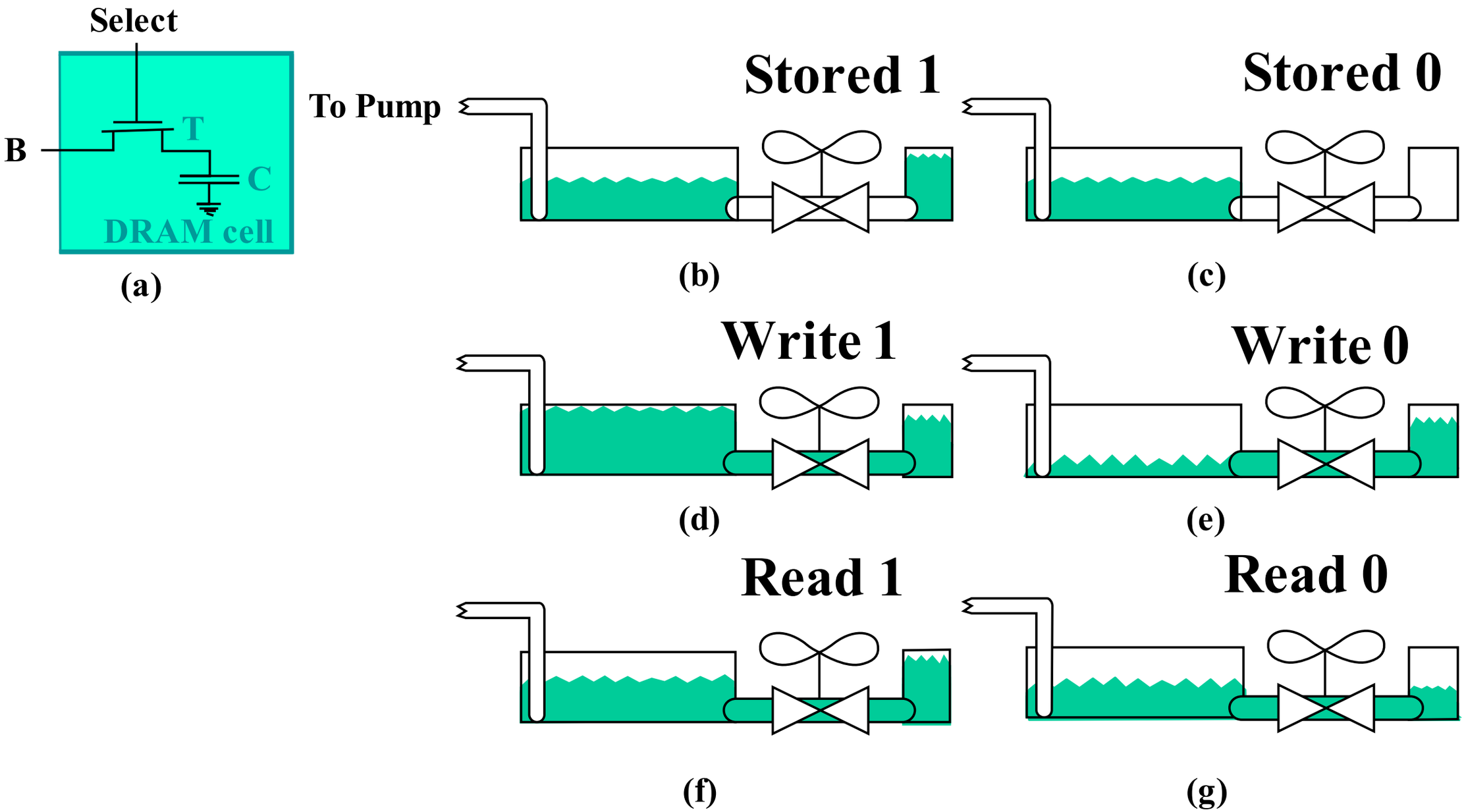


6T SRAM Sizing

- High bitlines must not overpower inverters during reads
- But low bitlines must write new value into cell



1T DRAM Cell



- Need sense amp helping reading

EX. 1T DRAM Cell

- **Question**: V_{DD}=4V, C_S=100pF, C_{BL}=1000pF. What's the voltage swing value?
- Note: $\Delta V = \frac{V_{DD}}{2} \cdot \frac{C_S}{C_S + C_{BL}}$

△V = 2 * 100 / (1000+100) = 0.045V = 45mV

SRAM v.s. DRAM

Static (SRAM)

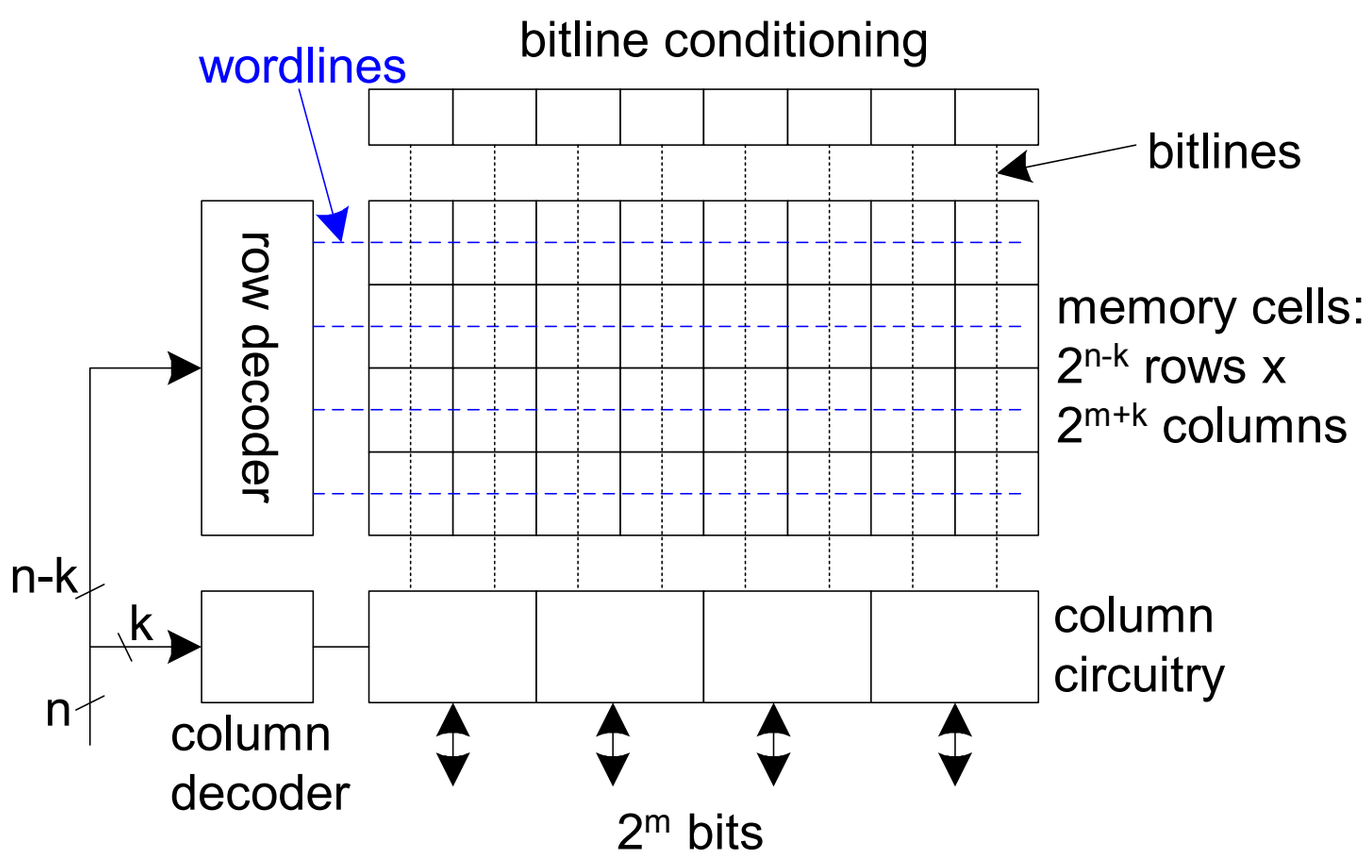
- Data stored as long as supply is applied
- Large (6 transistors/cell)
- Fast
- Compatible with current CMOS manufacturing

Dynamic (DRAM)

- Periodic refresh required
- Small (1-3 transistors/cell)
- Slower
- Require additional process for trench capacitance

Array Architecture

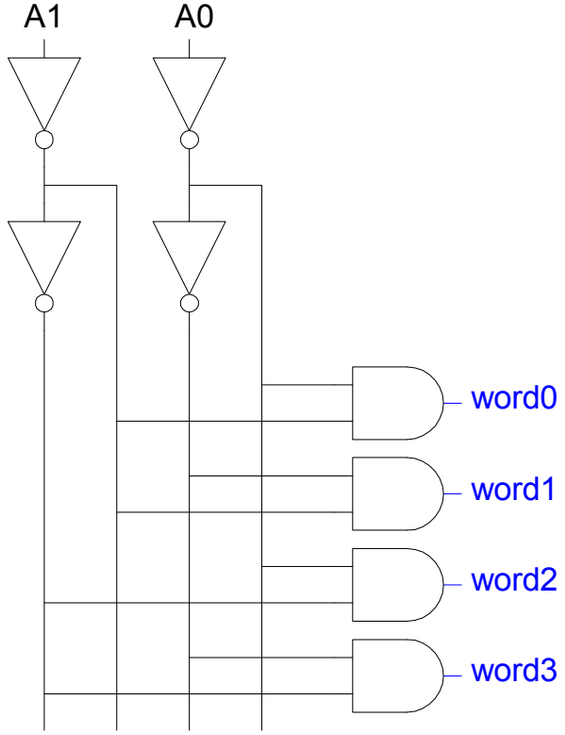
- 2^n words of 2^m bits each
- How to design if n >> m?
- fold by 2k into fewer rows of more columns



Decoders

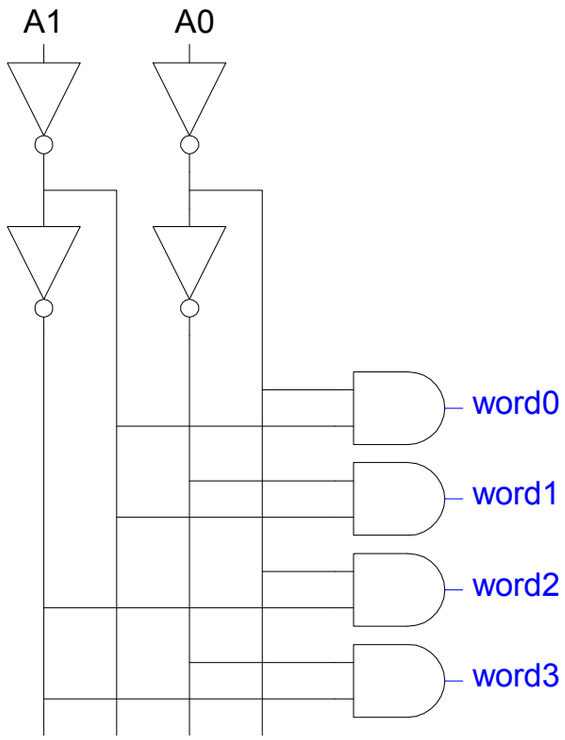
- n:2^n decoder consists of 2^n n-input AND gates
  - One needed for each row of memory
  - Build AND from NAND or NOR gates

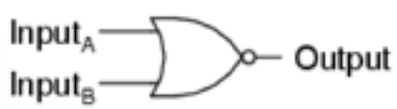
Static CMOS



EX. Decoder using NOR gates

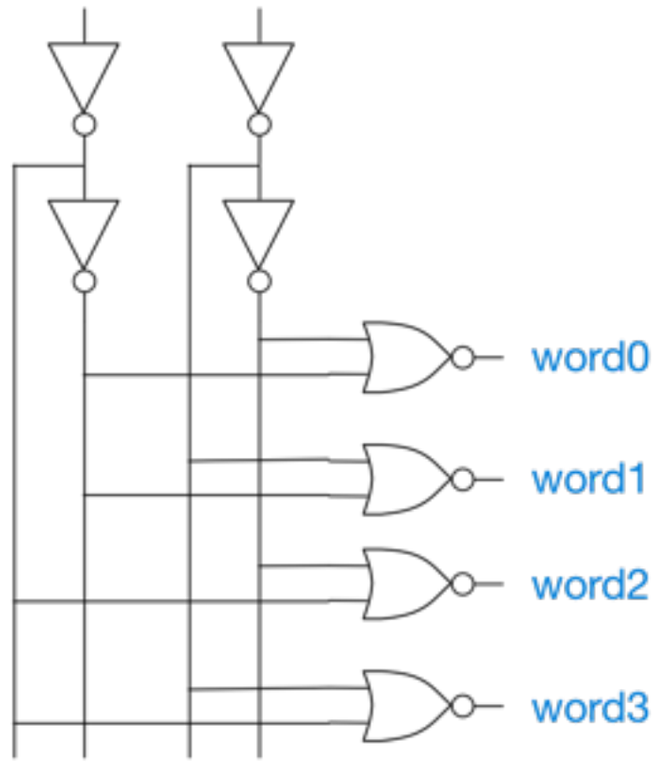
- **Question**: AND gates => NOR gate structure





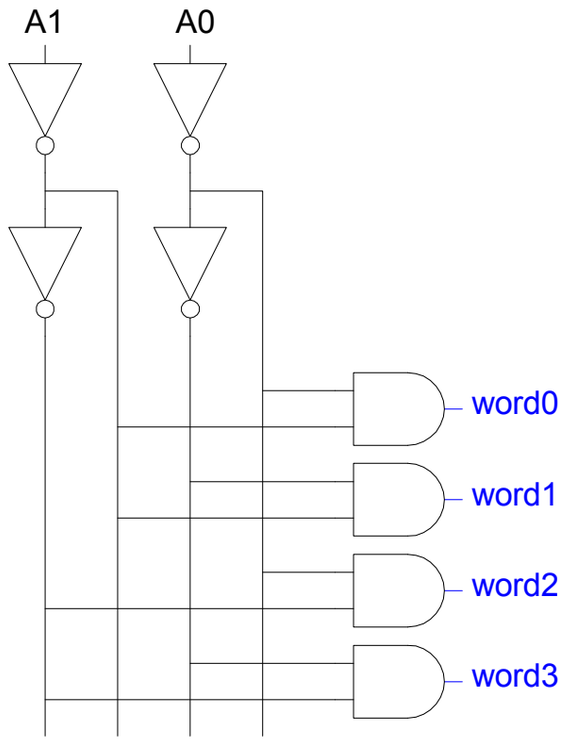
A	B	Output
0	0	1
0	1	0
1	0	0
1	1	0

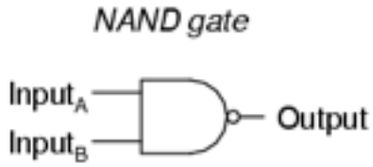
- **Answer**:



EX. Decoder using NAND gate

- **Question**: AND gates => NAND gate structure





A	B	Output
0	0	1
0	1	1
1	0	1
1	1	0

- **Answer**: [replace AND gates with NAND gates, followed by inverters]

Thank You :-)