

B2. Clock Summary

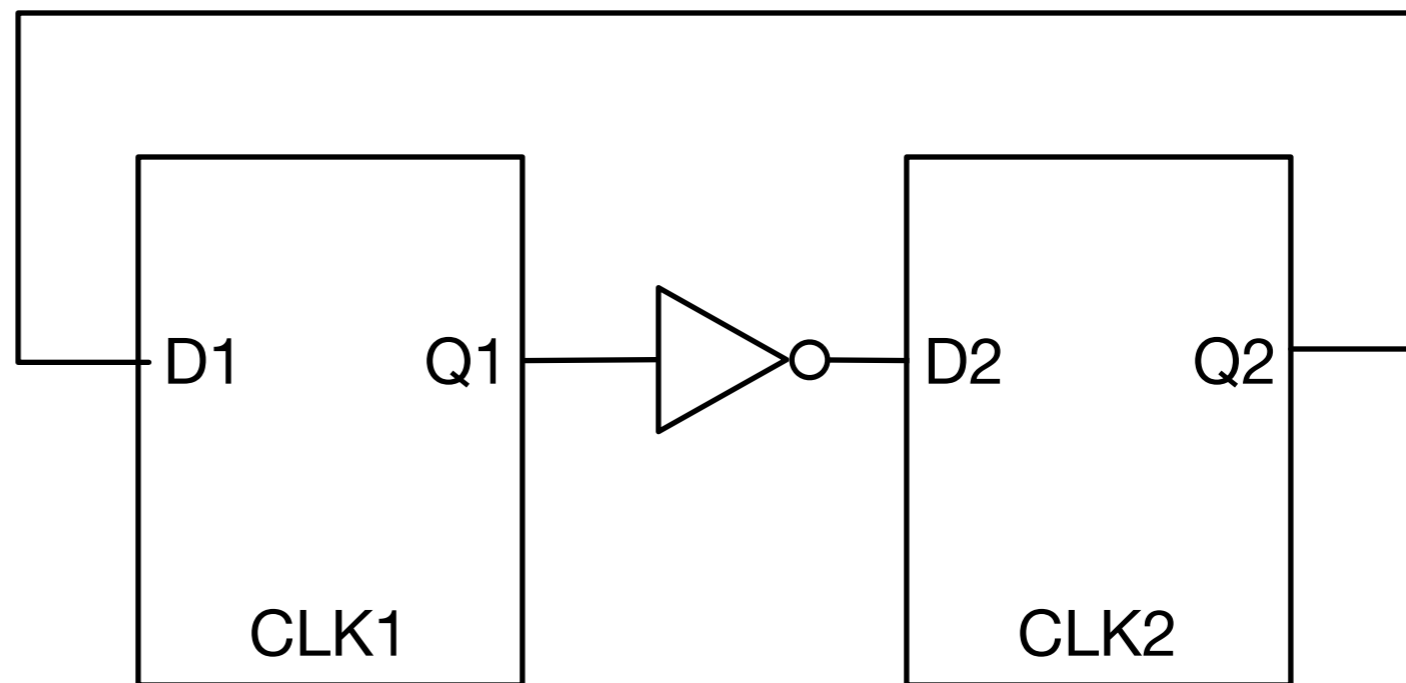
Bei Yu

Reference:

- **Chapter 11 Clock Distribution**
- **High speed digital design**
- **by Johnson and Graham**

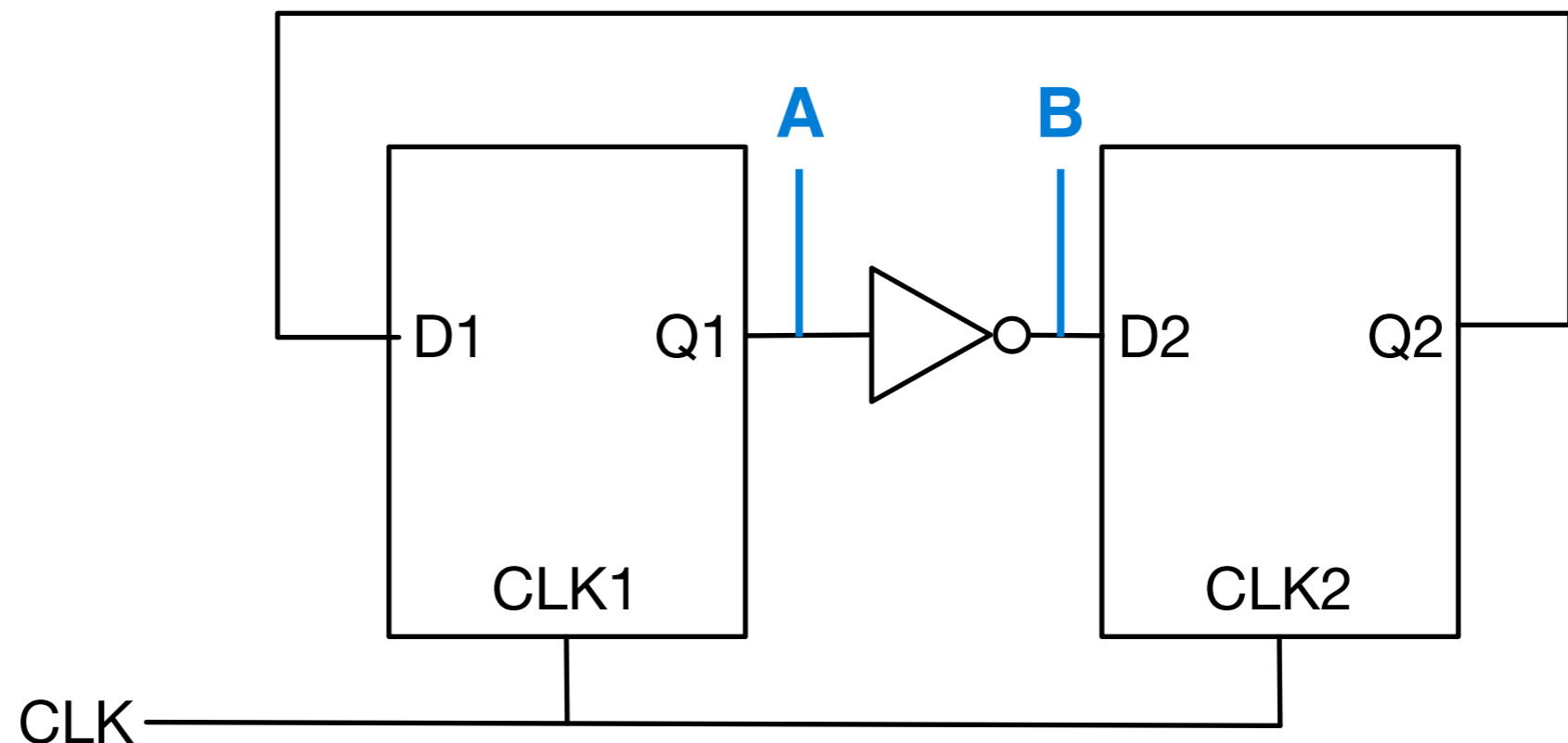
Notations in Clock Skew Calculation

- **$T_{ff,max}$** : max delay of flip-flop (FF)
- **$T_{G,max}$** : max delay of gate G, including track delay
- **T_{setup}** : worst-case setup time required by FF2, data at D2 must arrive at least T_{setup} before CLK_2
- **T_{CLK}** : clock period; interval between clocks



EX. B2-1

- CLK1 = CLK2 = 20MHz; flip flop max delay $T_{ff,max} = 8ns$; flip-flop setup time $T_{setup} = 5ns$; For each gate $T_{G,max} = 10ns$.
- **Questions:**
 - ♦ Find time margin
 - ♦ How many delay G gates can you insert between A and B without creating error?



EX. B2-1

- $T_{CLK} = 1 / 20\text{MHz} = 50\text{ns}$;
- **A1**: Time margin
 - ♦ $= T_{CLK} - T_{ff,max} - T_{setup} - T_{G,max}$
 - ♦ $= 50\text{ns} - 8\text{ns} - 5\text{ns} - 10\text{ns} = 27\text{ns}$
- **A2**: since each delay is 10ns, **2** more gates can be inserted between A and B

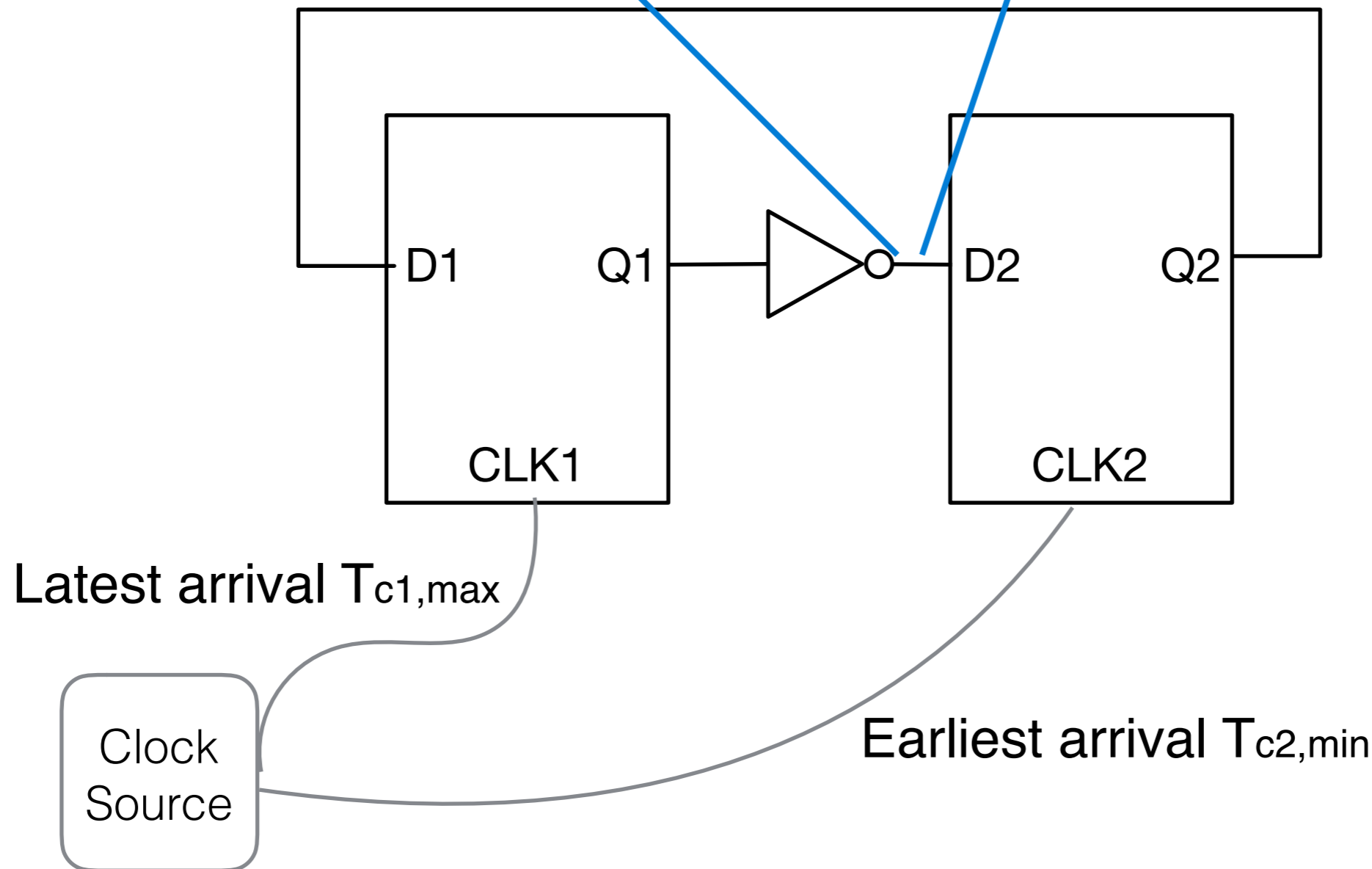
Why Care Clock Skew?

Signal arrives here no later than

$$T_{c1,max} + T_{ff,max} + T_{G,max}$$

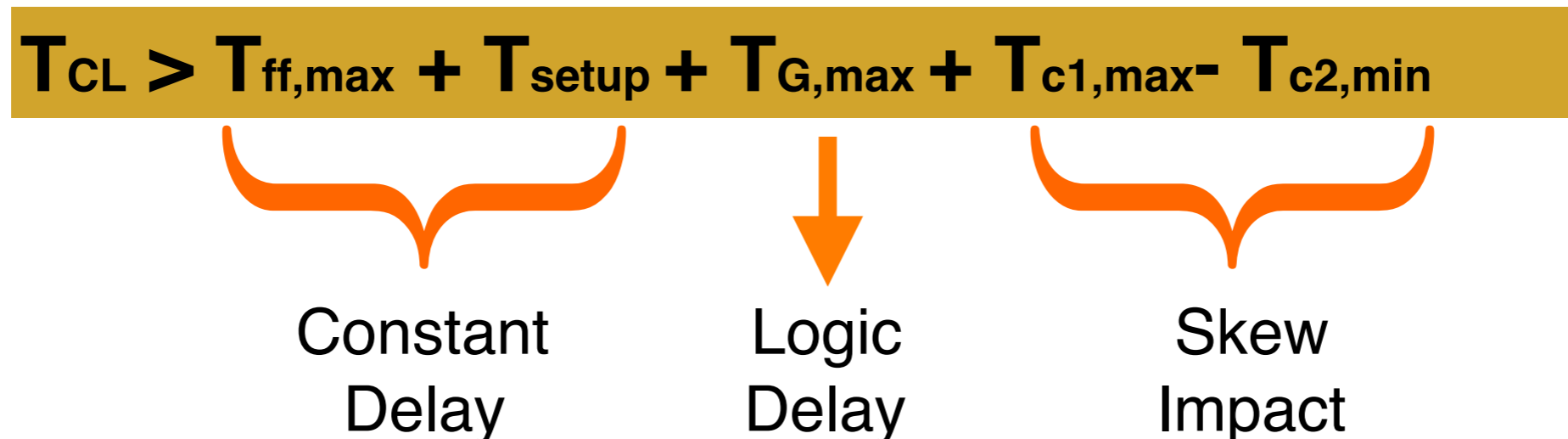
Signal arrives must be valid before next clock

$$T_{CLK} + T_{c2,min} - T_{setup}$$



Why Care Clock Skew?

- $T_{\text{slow}} = T_{c1,\text{max}} + T_{\text{ff,max}} + T_{G,\text{max}}$
- $T_{\text{required}} = T_{\text{CLK}} + T_{c2,\text{min}} - T_{\text{setup}}$
- Since $T_{\text{slow}} < T_{\text{required}} \Rightarrow$



EX. B2-2

Question: Given

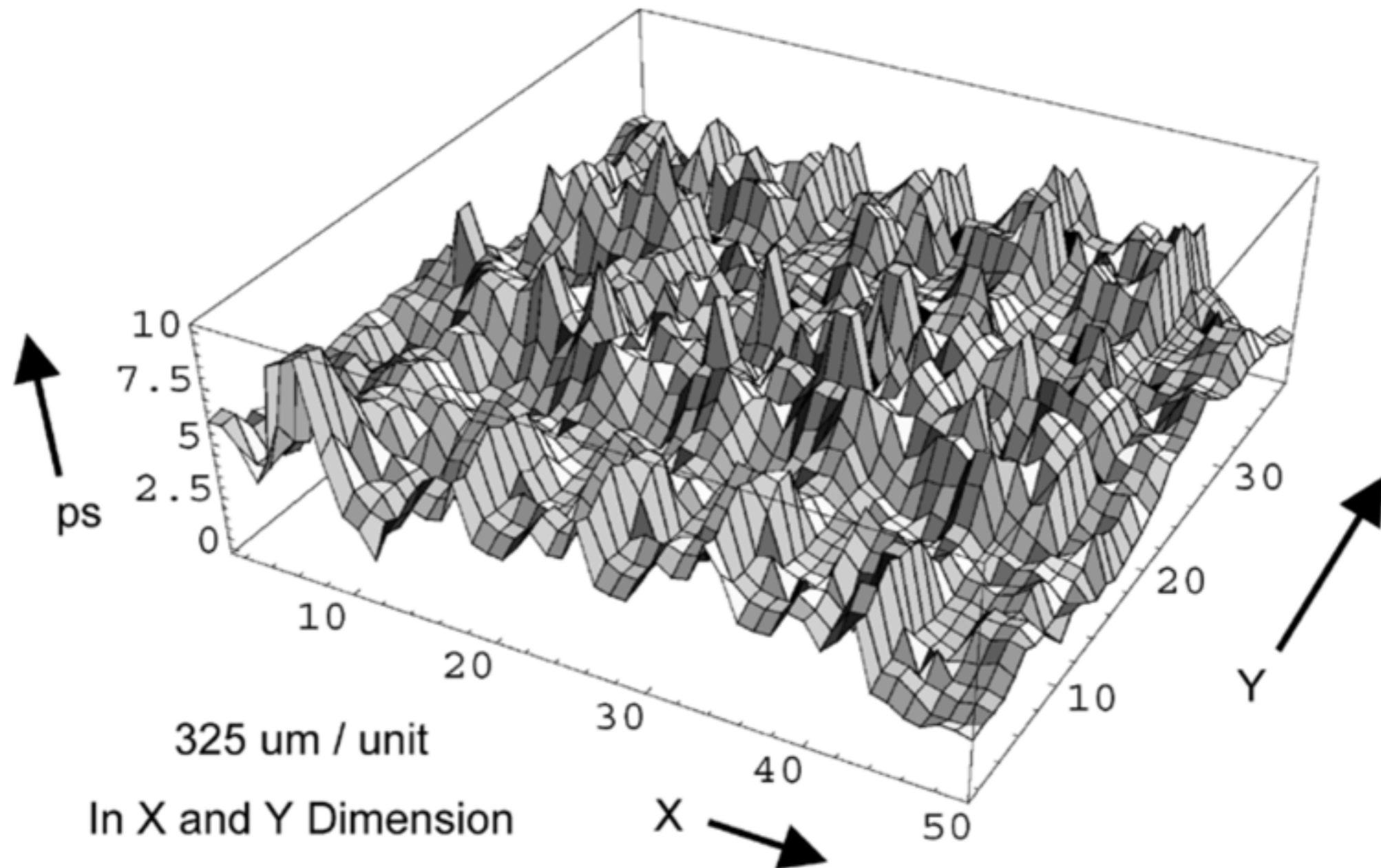
- $T_{ff,max} = 7ns;$
- $T_{G,max} = 5ns;$
- $T_{setup} = 4ns;$
- $T_{CLK} = 40MHz;$

What's the biggest time skew allowed?

Answer:

$$\begin{aligned} \text{max skew} &\leq T_{CLK} - (T_{ff,max} + T_{G,max} + T_{setup}) \\ &= 25ns - 7ns - 5ns - 4ns = 9ns \end{aligned}$$

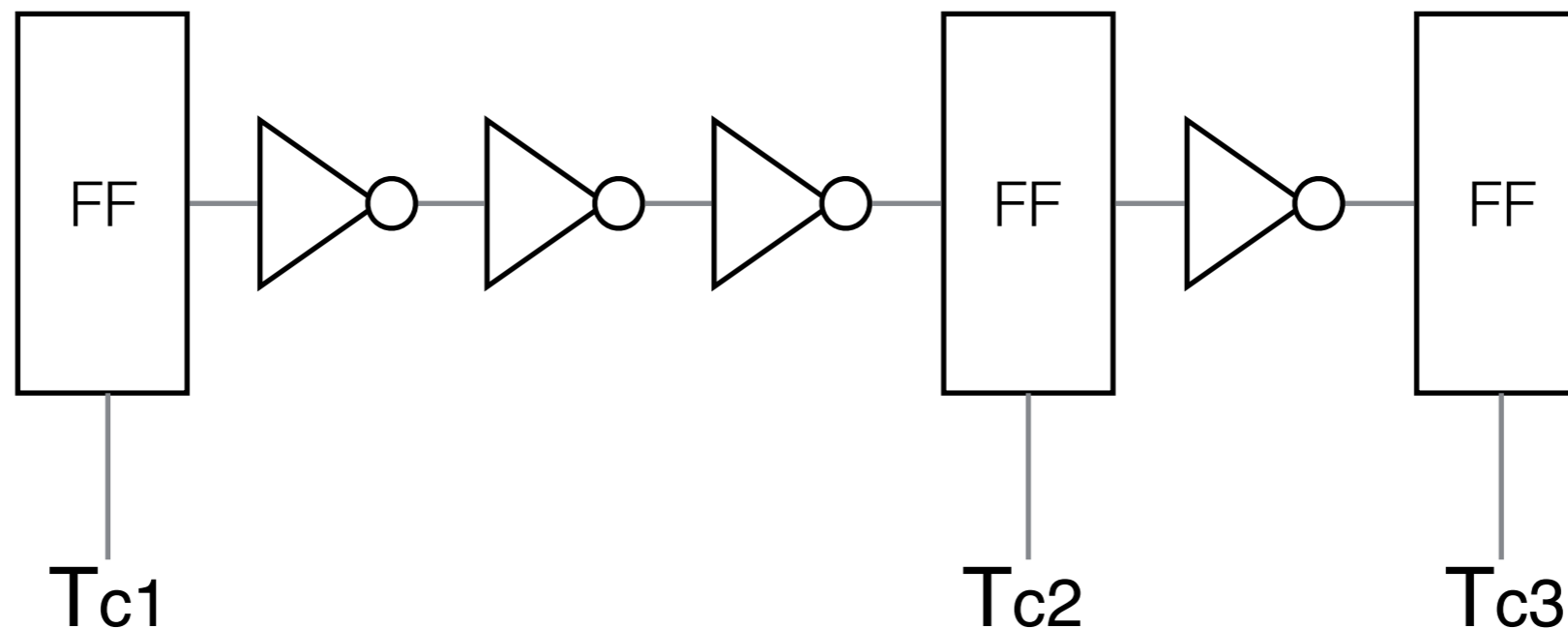
Clock Skew Distribution



[Pham et al, JSSC'2006]

EX. Skew Optimization

- Instead of Zero-Skew, take advantage of Skew.
- **Question:** Given $T_{G,max}=6ns$, $T_{ff,max}=10ns$, $T_{setup}=2ns$, what's the minimal T_{CLK} ?
 - ♦ The delay from T_{CLK} to the clock input CK1 of the flip flop (FF) is T_{c1} .
 - ♦ The delay from T_{CLK} to the clock input CK2 of the flip flop (FF) is T_{c2} .
 - ♦ The delay from T_{CLK} to the clock input CK3 of the flip flop (FF) is $T_{c3} = 0$.



EX. Skew Optimization

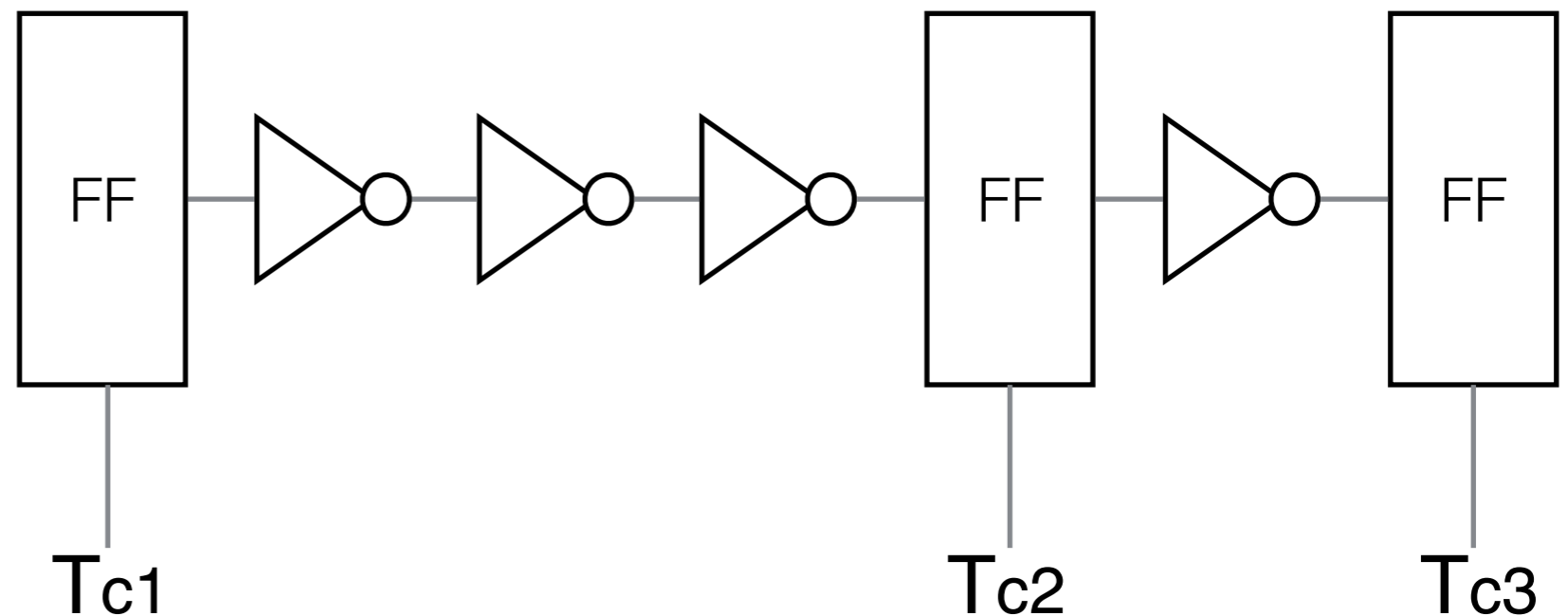
- **Answer:**

$$\left\{ \begin{array}{l} T_{CLK1} \geq T_{ff} + T_{setup} + 3 * T_G + (TC1 - TC2) = 30 + (TC1 - TC2) \\ T_{CLK2} \geq T_{ff} + T_{setup} + T_G + (TC2 - TC3) = 18 + (TC2 - TC3) \end{array} \right.$$

When TCLK is minimum $\Rightarrow T_{CLK1} = T_{CLK2}$

Since $TC3=0$, **Set** $TC1 = 0$, $TC2 = 6$,

$\Rightarrow T_{CLK} = 24$.



Thank You :-)