08. PCB — Summary

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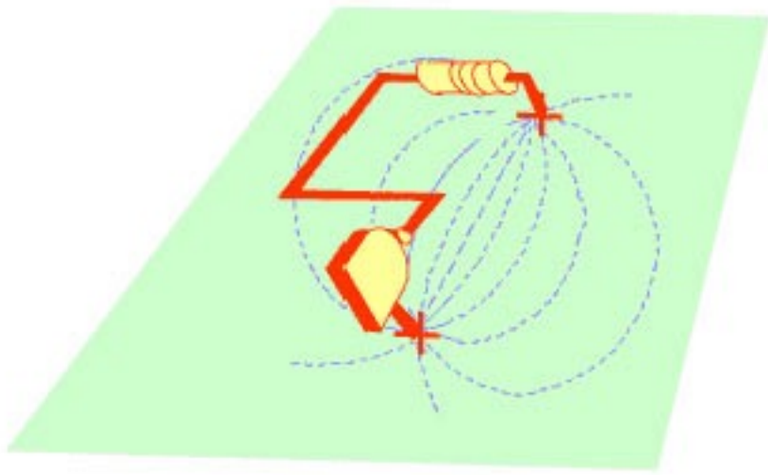
Reference:

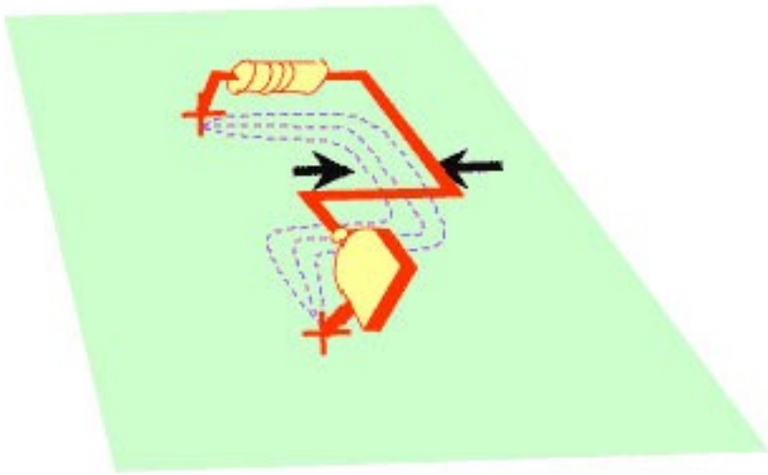
- Chapter 5 of Ground Planes and Layer Stacking
- **High speed digital design**
- by Johnson and Graham

Current Path

- At low speed: => Follow Least Resistance
- At high speed: Follow Least Inductance



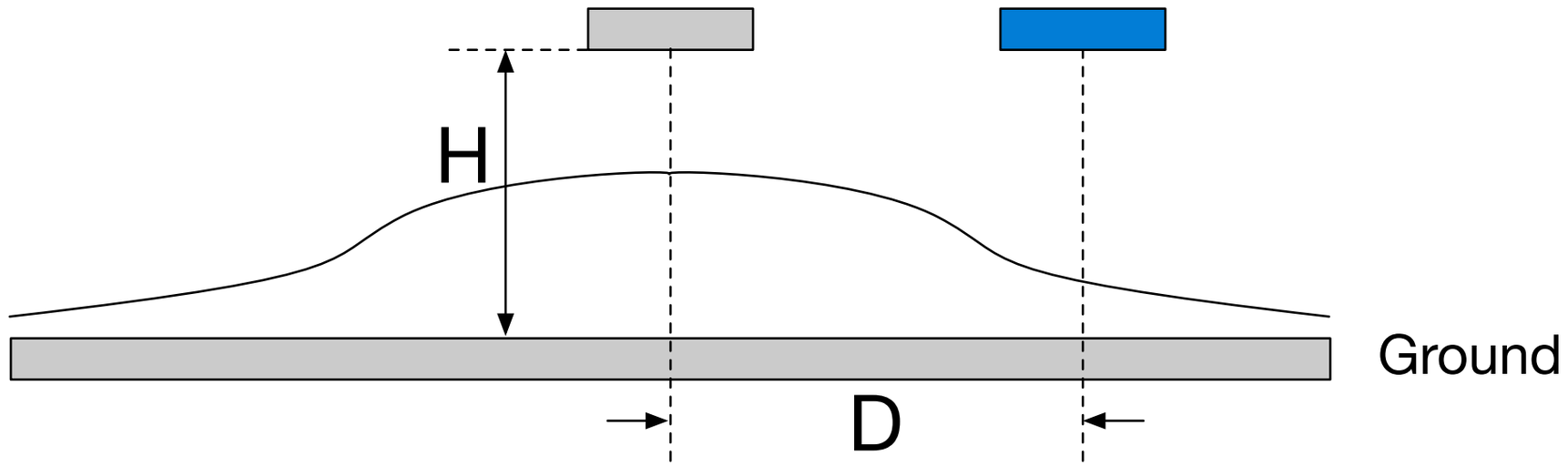
At low speeds, current flows the path of least resistance



At high speeds, current flows the path of least inductance

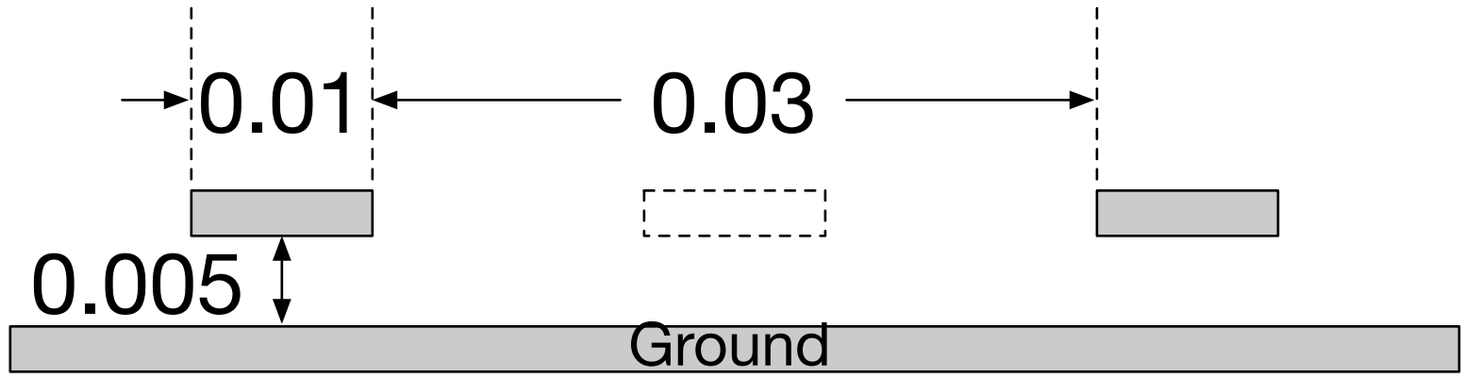
Crosstalk in Solid Ground Planes

- Crosstalk $\simeq \frac{K}{1+(D/H)^2}$
  - K <= rise time & length of trace
  - Faster rise time, higher K



Ex. Guard Trace Calculations

- Question: what's the estimated crosstalk?

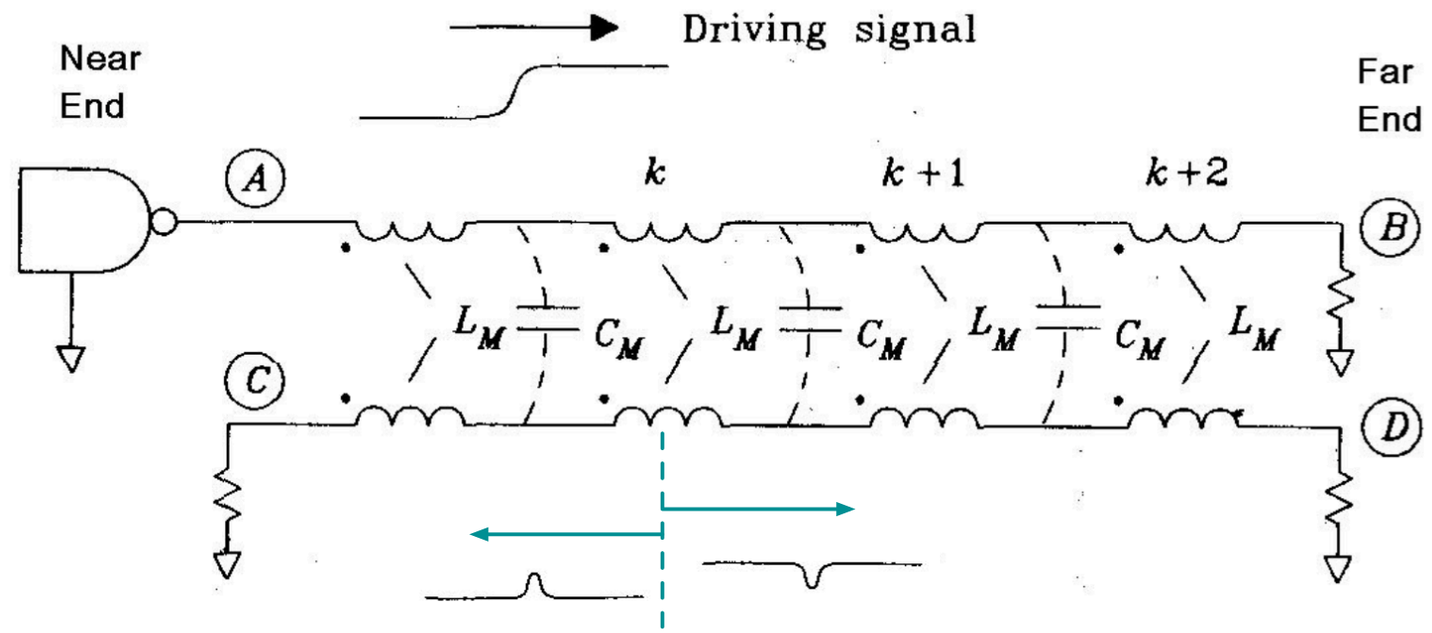


- Answer:

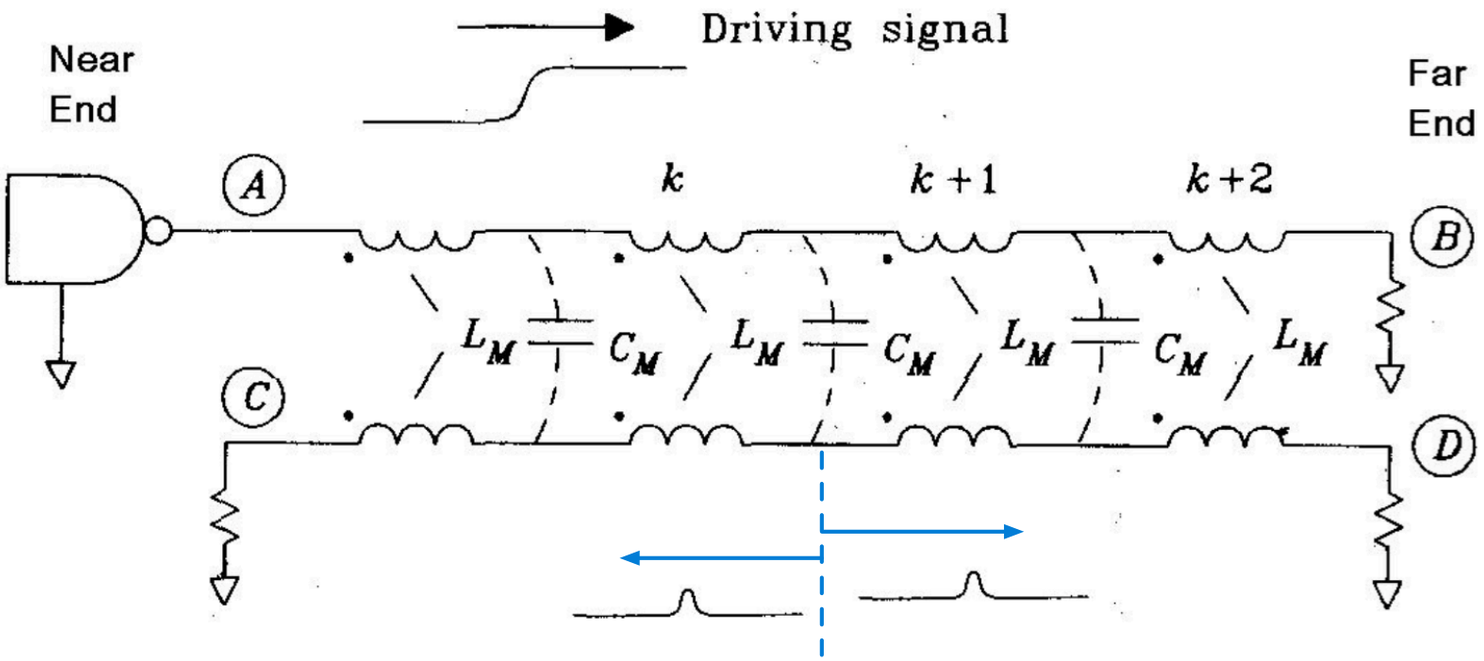
since K < 1, crosstalk < $\frac{1}{1+(D/H)^2} = \frac{1}{1+8^2} = 0.015$

- In general, reduce crosstalk to 1-3% is good enough

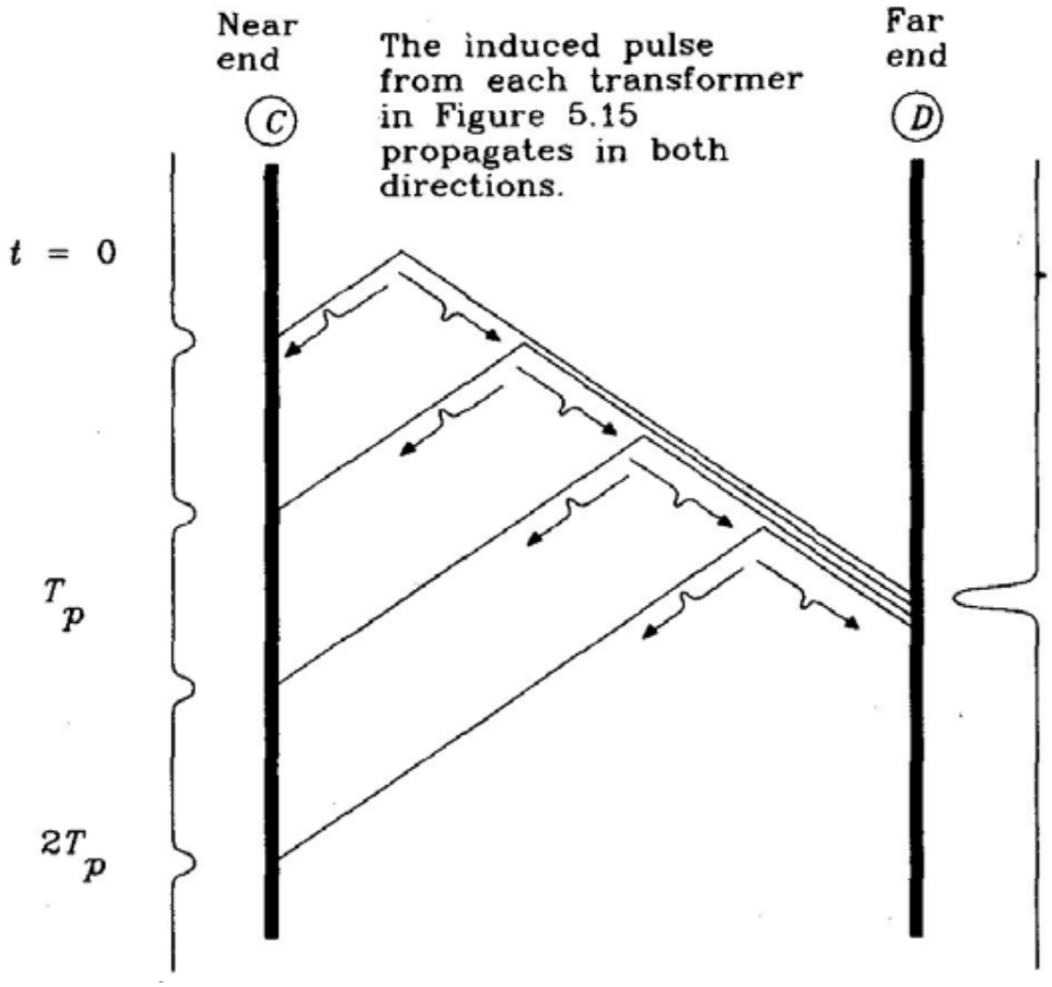
- Inductive Coupling Mechanism

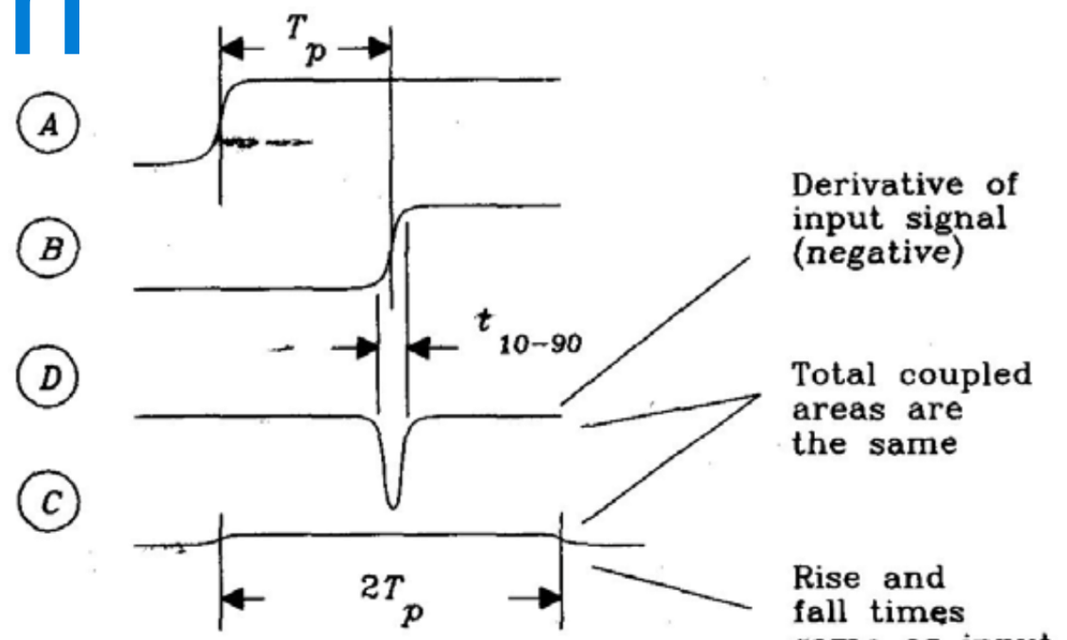


- Capacitance Coupling Mechanism

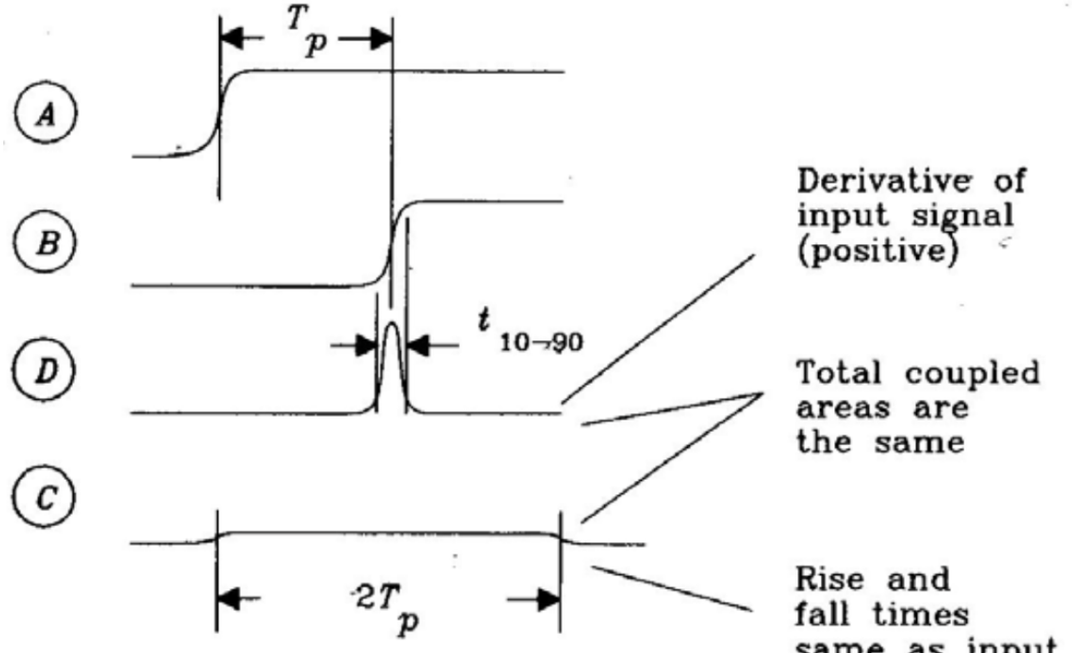


Reflection Diagram





Inductive coupling has opposite polarities in the forward and reverse directions



Capacitive coupling has the same polarities in the forward and reverse directions.

Combining Mutual Inductive & Capacitive Coupling

- Generally, over a solid ground plane, inductive and capacitive crosstalk voltages are roughly equal
- Over slotted, hatched or imperfect ground plane
  - Inductive component is much larger
  - Forward cross talk is large & negative